Intel® E7500/E7501/E7505 Chipset

Thermal Design Guide

For the Intel® E7500/E7501/E7505 Chipset Memory Controller Hub (MCH)

December 2002
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<thead>
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<th>Revision Number</th>
<th>Description</th>
<th>Date</th>
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<tr>
<td>-001</td>
<td>Initial Release as an Intel® E7500 chipset specific document</td>
<td>February 2002</td>
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<tr>
<td>-002</td>
<td>• Added Intel® E7505 chipset specific information and re-titled document</td>
<td>November 2002</td>
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<tr>
<td></td>
<td>• Removed 90°C Angle Attach Die Temperature Measurement Methodology</td>
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<td></td>
<td>• Updated Supplier Contact Information</td>
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<tr>
<td></td>
<td>• All reference to $T_{die-hs}$ changed to $T_{case}$</td>
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<tr>
<td>-003</td>
<td>• Added Intel® E7501 chipset specific information and re-titled document</td>
<td>December 2002</td>
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<td>• Updated E7500/E7505 chipset MCH thermal specifications</td>
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Introduction

As the complexity of computer systems increase, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are:

- To specify the operating limits of the Intel® E7500/E7501/E7505 chipset MCH components.
- To describe a reference thermal solution that meets the thermal specifications of the Intel® E7500/E7501/E7505 chipset MCH components.

Properly designed solutions provide adequate cooling to maintain the E7500/E7501/E7505 chipset MCH die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the E7500/E7501/E7505 chipset MCH die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the E7500/E7501/E7505 chipset MCH components only. For thermal design information on other chipset components, refer to the respective component datasheet. For the P64H2, refer to the Intel® PCI-64 Hub 2 (P64H2) Thermal Design Guidelines. For the ICH3-S, refer to the Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet. For the ICH4, refer to the Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet.

Note: Unless otherwise specified, the term “MCH” refers to all the E7500/E7501/E7505 chipset MCHs.
1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. Figure 1 illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1. Thermal Design Process

- **Step 1: Thermal Simulation**
  - Thermal Models
  - Thermal Model Users Guide

- **Step 2: Heatsink Selection**
  - Thermal Reference
  - Mechanical Reference

- **Step 3: Thermal Validation**
  - Thermal Testing Software
  - Software Users Guide
1.2 Definition of Terms

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
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<tbody>
<tr>
<td>BGA</td>
<td>Ball Grid Array. A package type defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.</td>
</tr>
<tr>
<td>Intel® ICH3-S / Intel® ICH4</td>
<td>I/O Controller Hub. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA-100, and other legacy functions.</td>
</tr>
<tr>
<td>MCH</td>
<td>Memory Controller Hub. The chipset component that contains the processor interface, the memory interface, and the hub interfaces.</td>
</tr>
<tr>
<td>FC-BGA</td>
<td>Flip Chip Ball Grid Array. A package type defined by a resin-fiber substrate where a die is mounted using an underfilled C4 (controlled collapse chip connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. The device arrives at the customer with solder balls attached. This is the packaging technology used for the MCH.</td>
</tr>
<tr>
<td>Intel® P64H2</td>
<td>Bus Controller Hub. The chipset component that interfaces the PCI-X buses.</td>
</tr>
<tr>
<td>T\text{_case}</td>
<td>Maximum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power. Thermal solutions should be designed to dissipate this target power level.</td>
</tr>
</tbody>
</table>
## 1.3 Reference Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Document Number/Location</th>
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<tbody>
<tr>
<td>Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet</td>
<td><a href="http://developer.intel.com/design/chipssets/e7501/datashts/251927.htm">http://developer.intel.com/design/chipssets/e7501/datashts/251927.htm</a></td>
</tr>
<tr>
<td>Intel® E7505 Chipset Memory Controller Hub (MCH) Datasheet</td>
<td><a href="http://developer.intel.com/design/chipssets/e7505/datashts/251932.htm">http://developer.intel.com/design/chipssets/e7505/datashts/251932.htm</a></td>
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<td>Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet</td>
<td><a href="http://developer.intel.com/design/chipssets/e7505/datashts/290733.htm">http://developer.intel.com/design/chipssets/e7505/datashts/290733.htm</a></td>
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<tr>
<td>Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet</td>
<td><a href="http://developer.intel.com/design/chipssets/e7500/datashts/290732.htm">http://developer.intel.com/design/chipssets/e7500/datashts/290732.htm</a></td>
</tr>
<tr>
<td>Thermal Design Suggestions for various form factors</td>
<td><a href="http://www.formfactors.org">http://www.formfactors.org</a></td>
</tr>
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</table>

**NOTE:** Contact your Intel Field Sales representative for further reference information.
The E7500 and E7501 chipsets consist of three individual components: the chipset memory controller hub (MCH), 82870P2 P64H2, and 82801CA ICH3-S. The E7505 chipset includes the chipset memory controller hub (MCH), 82870P2 P64H2, and the 82801DB ICH4. The E7500/E7501/E7505 chipset MCH components use a 42.5 mm, 6-layer FC-BGA package (see Figure 2 and Figure 3). For information on the P64H2 package, refer to the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal and Mechanical Design Guidelines and the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet. For information on the ICH3-S package, refer to the Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet. For information on the ICH4 package, refer to the Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet.

NOTES:
1. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
2. All dimensions and tolerances conform to ANSI Y14.5M–1982.
Figure 3. MCH Package Dimensions (Top View)

NOTES:
1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M–1982.
3 Thermal Simulation

Intel provides thermal simulation models of the MCH and associated user’s guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool “FLOTHERM®” (version 3.1 or higher) by Flomerics, Inc. Contact your Intel Field Sales representative to order the thermal models and user’s guides.
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4 Thermal Specifications

4.1 Case Temperature and Thermal Design Power

For TDP specifications, see Table 1 for the E7500 chipset MCH, Table 2 for the E7501 chipset MCH, and Table 3 for the E7505 chipset MCH. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers plan for one or more heatsinks when using the E7500/E7501/E7505 chipset.

4.2 Die Temperature

To ensure proper operation and reliability of the MCH, the die temperatures must be at or below the values specified in Table 1, Table 2, and Table 3. System and/or component level thermal solutions are required to maintain die temperatures below the maximum temperature specification. Refer to Chapter 5 for guidelines on accurately measuring package die temperatures.

Table 1. Intel® E7500 Chipset MCH Thermal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum</th>
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<tbody>
<tr>
<td>$T_{\text{case}}$</td>
<td>102 °C</td>
</tr>
<tr>
<td>TDP$_{\text{dual channel}}$</td>
<td>7.5 W</td>
</tr>
</tbody>
</table>

Table 2. Intel® E7501 Chipset MCH Thermal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{case}}$</td>
<td>105 °C</td>
</tr>
<tr>
<td>TDP$_{\text{dual channel}}$</td>
<td>8.5 W</td>
</tr>
<tr>
<td>TDP$_{\text{single channel}}$</td>
<td>7.8 W</td>
</tr>
</tbody>
</table>

Table 3. Intel® E7505 Chipset MCH Thermal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum</th>
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</thead>
<tbody>
<tr>
<td>$T_{\text{case}}$</td>
<td>105 °C</td>
</tr>
<tr>
<td>TDP$_{\text{dual channel}}$</td>
<td>6.5 W</td>
</tr>
<tr>
<td>TDP$_{\text{single channel}}$</td>
<td>5.1 W</td>
</tr>
</tbody>
</table>
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5 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the MCH package die temperature. Section 5.1 provides guidelines on how to accurately measure the MCH die temperatures. Section 5.2 contains information on running an application program that will emulate anticipated maximum thermal design power. The flowchart in Figure 6 offers guidelines for thermal performance and evaluation.

5.1 Die Temperature Measurements

To ensure functionality and reliability, the $T_{\text{case}}$ of the MCH must be maintained at or below the maximum temperature specifications as noted in Table 1, Table 2, and Table 3. The surface temperature at the geometric center of the die corresponds to $T_{\text{case}}$. Measuring $T_{\text{case}}$ requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heatsink base (if a heatsink is used). To maximum measurement accuracy, only the 0° degree thermocouple attach approach is recommended for thermocouple attach.

5.1.1 0° Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot, from the centered hole to one edge of the heatsink. The slot should be in the direction parallel to the heatsink fins (see Figure 5).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using high thermal conductivity cement. During this step, make sure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. It is critical that the thermocouple bead makes contact with the die (see Figure 4).
6. Attach heatsink assembly to the MCH, and route thermocouple wire out through the milled slot.
Figure 4. 0° Angle Attach Methodology (Top View)

![Diagram of 0° Angle Attach Methodology](angle_attach_1)

**NOTE:** Not to scale.

Figure 5. 0° Angle Attach Heatsink Modifications

![Diagram of Heatsink Modifications](Angle_Attach_Heatsink_Mod)

1.3 mm (0.05 in.)
(0.5 mm (0.02 in.) Depth)

3.3 mm (0.13 in.) Diameter
(1.5 mm (0.06 in.) Depth)

**NOTE:** Not to scale.
5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the thermal design power on an E7500/E7501/E7505 chipset MCH when used in conjunction with Intel® Xeon™ processor with 512-KB L2 cache or Intel® Xeon™ processor with 533 MHz system bus. The combination of the Xeon processor(s) and the higher bandwidth capability of the E7500/E7501/E7505 chipsets enable new levels of system performance. To assess the thermal performance of the chipset MCH thermal solution under “worst-case realistic application” conditions, Intel has developed a software utility that operates the chipset at near worst-case power dissipation.

The utility has been developed solely for testing customer thermal solutions at near the thermal design power. Figure 6 shows a decision flowchart for determining thermal solution needs. Real future applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, refer to each component’s datasheet for the ICC (Max Power Supply Current) specification. Contact your Intel Field Sales representative to obtain a copy of this software.

Figure 6. Thermal Solution Decision Flowchart
6 Reference Thermal Solutions

Intel has developed a reference thermal solution designed to meet the cooling needs of the E7500/E7501/E7505 chipset MCH at worst-case conditions. This chapter describes the overall requirements for the reference thermal solution, including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need thermal solutions, depending on specific system local-ambient operating conditions. For information on the P64H2 thermal solutions, refer to the Intel® 82870P2 PCI-64 Hub 2 (P64H2) Thermal Design Guidelines. For the ICH3-S, refer to thermal specification in the Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet. For the ICH4, refer to thermal specification in the Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet.

6.1 Operating Environment

The reference thermal solution was designed assuming a maximum local-ambient temperature of 50 °C. The minimum recommended airflow velocity at the heatsink is 200 lfm (linear feet per minute). The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35 °C external-ambient temperature at sea level. (External-ambient refers to the environment external to the system.)

6.2 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the E7500/E7501/E7505 chipset MCH thermal solution are shown in Figure 7.

When using heatsinks that extend beyond the MCH reference heatsink envelope shown in Figure 7, any motherboard components placed between the heatsink and motherboard cannot exceed 2.286 mm (0.090 in.) in height.
Figure 7. Reference Heatsink Volumetric Envelope for the MCH

NOTE: Not to scale.
6.3 Thermal Solution Assembly

The reference thermal solution for the E7500/E7501/E7505 MCH is a passive extruded heatsink with thermal and mechanical interfaces. It is attached using a clip with each end hooked through an anchor soldered to the board. Figure 8 shows the reference thermal solution assembly and associated components.

Figure 9 and Figure 10 show alternate views of the reference solution. Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

Figure 8. Reference Thermal Solution Assembly
Figure 9. Reference Thermal Solution Assembly (Side View)

Figure 10. Reference Thermal Solution (Top View)
6.3.1 Heatsink Orientations

To enhance the efficiency of the reference thermal solution, it is important for the designer to orient the fins properly with respect to the mean airflow direction. Simulation and experimental evidence have shown that the MCH heatsink thermal performance is enhanced when the fins are aligned with the mean airflow direction (Figure 11). Aligning the heatsink 45 degrees relative to the airflow is acceptable but delivers reduced thermal performance.

**Figure 11. Preferred Heatsink Orientation**
6.3.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the E7500/E7501/E7505 chipset MCH components. Figure 12 shows the heatsink profile. This document does not provide tolerance information. Check with your heatsink supplier for specific tolerances. Appendix A lists suppliers for the extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available, including the tall heatsink shown in Figure 13. Contact your heatsink supplier for information on alternate heatsinks.

**Figure 12. Extruded Heatsink Profile**

![Extr_Heatsink_Profile](image1)

**NOTE:** Not to scale.

**Figure 13. Alternate Tall Heatsink Profile**

![Alt_Extr_Heatsink_Profile](image2)

**NOTE:** Not to scale.
6.3.3 **Mechanical Interface Material**

Intel recommends the use of a mechanical interface material to avoid cracking of the exposed die under loading. The interface material reduces mechanical loads experienced by the die. The reference thermal solution uses a picture frame gasket of 0.813 mm (0.032 in.) thick Poron® foam. The foam gasket is a two-piece design with diagonal cuts at two corners as shown in Figure 14. A one-piece gasket design may be used instead without any impact to mechanical performance.

![Figure 14. Heatsink Mechanical Gasket, Optional Two-Piece](image)

**NOTE:** Not to scale.

6.3.4 **Thermal Interface Material**

A thermal interface material provides improved conductivity between the die and heatsink. The reference thermal solution uses Chomerics’ T-710, 0.127 mm (0.005 in.) thick, 25.4 mm x 25.4 mm (1.0 in. x 1.0 in.) square.

6.3.5 **Heatsink Clip**

The reference solution uses a wire clip with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See Figure 18 in Appendix B for a mechanical drawing of the clip.
6.3.6 Clip Retention Anchors

For E7500/E7501/E7505 chipset-based platforms that have very limited board space, a clip retention anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45-degree bent leads to increase the anchor attach reliability over time. See Appendix A for the part number and supplier information.

6.3.7 Board Level Component Keep-Out Dimensions

The locations of hole patterns and keep-out zones for the reference thermal solution are shown in Figure 15 and Figure 16.

Figure 15. Heatsink Retention Mechanism Layout

NOTES:
1. Dimensions are in inches.
2. Not to scale.
Figure 16. Retention Mechanism Component Keep-Out Zones

NOTES:
1. Dimensions are in inches.
2. Not to scale.
6.4 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 4.

Table 4. Reliability Guidelines

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Profile</th>
<th>Pass/Fail Criteria</th>
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<tbody>
<tr>
<td>Mechanical Shock</td>
<td>50 g, board level, 11 msec, 3 shocks/axis</td>
<td>Visual Check and Electrical Functional Test</td>
</tr>
<tr>
<td>Random Vibration</td>
<td>7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz</td>
<td>Visual Check and Electrical Functional Test</td>
</tr>
<tr>
<td>Temperature Life</td>
<td>85 °C, 2000 hours total, checkpoints at 168, 500,</td>
<td>Visual Check</td>
</tr>
<tr>
<td></td>
<td>1000, and 2000 hours</td>
<td></td>
</tr>
<tr>
<td>Thermal Cycling</td>
<td>-5 °C to +70 °C, 500 cycles</td>
<td>Visual Check</td>
</tr>
<tr>
<td>Humidity</td>
<td>85% relative humidity, 55 °C, 1000 hours</td>
<td>Visual Check</td>
</tr>
</tbody>
</table>

NOTES:
1. It is recommended that the above tests be performed on a sample size of at least 12 assemblies from 3 lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.
Note: These vendors/devices are listed by Intel as a convenience to Intel’s general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

Table 5. Complete Thermal Solution Kits

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier</th>
<th>Contact Information</th>
</tr>
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<tbody>
<tr>
<td>Pin Fin Heatsink Kit</td>
<td>A69225-001</td>
<td>CCI/ACK</td>
<td>Harry Lin 714-739-5797</td>
</tr>
<tr>
<td>(31gm, 42 x 42 x 23 mm)</td>
<td></td>
<td></td>
<td><a href="mailto:hlinack@aol.com">hlinack@aol.com</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Monica Chih 866-2-29952666x131</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>Foxconn</td>
<td>Bob Hall 503-693-3509 x235</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
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<tr>
<td>Alternate Pin Fin Heatsink Kit</td>
<td>A69225-002</td>
<td>CCI/ACK</td>
<td>Harry Lin 714-739-5797</td>
</tr>
<tr>
<td>(43gm, 42 x 42 x 35 mm)</td>
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<td></td>
<td><a href="mailto:hlinack@aol.com">hlinack@aol.com</a></td>
</tr>
<tr>
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<td></td>
<td></td>
<td><a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
</tr>
</tbody>
</table>

Table 6. Extruded Heatsinks

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Fin Heatsink Kit</td>
<td>A20930-001</td>
<td>CCI/ACK</td>
<td>Harry Lin 714-739-5797</td>
</tr>
<tr>
<td>(31gm, 42 x 42 x 23 mm)</td>
<td></td>
<td></td>
<td><a href="mailto:hlinack@aol.com">hlinack@aol.com</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Monica Chih 866-2-29952666x131</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Foxconn</td>
<td>Bob Hall 503-693-3509 x235</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
</tr>
</tbody>
</table>
Appendix A: Thermal Solution Component Suppliers

| Alternate Pin Fin Heatsink Kit (43gm, 42 x 42 x 35 mm) | A13506-001 | CCI/ACK | Harry Lin  
714-739-5797  
hlinack@aol.com  
Monica Chih  
866-2-29952666x131  
monica_chih@ccic.com.tw | Foxconn | Bob Hall  
503-693-3509x235  
bhall@foxconn.com |

Table 7. Interface Materials

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier (Part Number)</th>
<th>Contact Information</th>
</tr>
</thead>
</table>
| Thermal Interface (T-710) | — | Chomerics (69-12-22315-T710) | Todd Sousa  
360- 606-8171  
tsousa@parker.com |
| Mechanical Interface (Poron*) | A69141-001 | Boyd | Rhoda Kennedy  
503-972-3170  
rkennedy@boydcorp.com |
|  |
|  |
|  |

Table 8. Attach Hardware

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier</th>
<th>Contact Information</th>
</tr>
</thead>
</table>
| Heatsink Attach Clip | A69230-001 | CCI/ACK | Harry Lin  
714-739-5797  
hlinack@aol.com  
Monica Chih  
866-2-29952666x131  
monica_chih@ccic.com.tw |
|  |
| Solder-Down Anchor | A13494-005 | Foxconn | Julia Jiang  
408-919-6178  
juilaj@foxconn.com |

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.
Appendix B: Mechanical Drawings

This appendix contains the following drawings:

- MCH Heatsink Assembly (See Figure 17)
- MCH Heatsink Clip (See Figure 18)
Figure 17. MCH Heatsink Assembly

NOTES: UNLESS OTHERWISE SPECIFIED
1. ITEM IDENTIFICATION NUMBER IS AX9225-00X.
2. INTEL PROCUREMENT SPECIFICATION 402160 SHALL APPLY.
3. ELECTRONIC DATA FOR THIS FILE EXISTS.
4. HATCH ITEM NUMBER, VENDOR IDENTIFICATION NUMBER AND
   DATE CODE APPROXIMATELY WHERE SHOWN.
5. NOMINALLY CENTER INTERFACE PAD (ITEM 4) AND
   GASKET (ITEM 3) ALONG CENTER LINES AS SHOWN.
6. SHIP ASSEMBLY COMPLETE WITH MEX CLIP
   LOCATED AS SHOWN.
7. TABLE BELOW CONTROLS THE ASSEMBLY PARTS LIST.

1  CH4161-001 HEAT SINK BASE
2  CH4161-002 HEAT SINK RETAINING CLIP
3  CH4156-001 HEAT SINK, FIN FIN, 14kg
4  CH4156-002 HEAT SINK, FIN FIN, 15kg

PARTS LIST

Intel® E7500/E7501/E7505 Chipset MCH Thermal Design Guide 34
Figure 18. MCH Heatsink Clip

NOTES:

1. ITEM IDENTIFICATION NUMBER IS A69230-001.
2. INSIDE BEND RADIUS TO BE .061 UNLESS OTHERWISE SPECIFIED.
3. PART SHALL BE DegREASED, WASHED, AND FREE OF OIL AND/OR DIRT MARKS.
4. INTEL PROCUREMENT SPECIFICATION A02160 SHALL APPLY.
5. ELECTRONIC DATA FOR THIS FILE EXISTS.
6. BREAK ALL SHARP EDGES, REMOVE ALL BURRS.