IDF2012
INTEL DEVELOPER FORUM

Embedded Technology Continuum for Academia

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Embedded Products Engineering Manager, Intel Corporation
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Market Development Manager, Intel Corporation

ACAS001

Sponsors of Tomorrow.

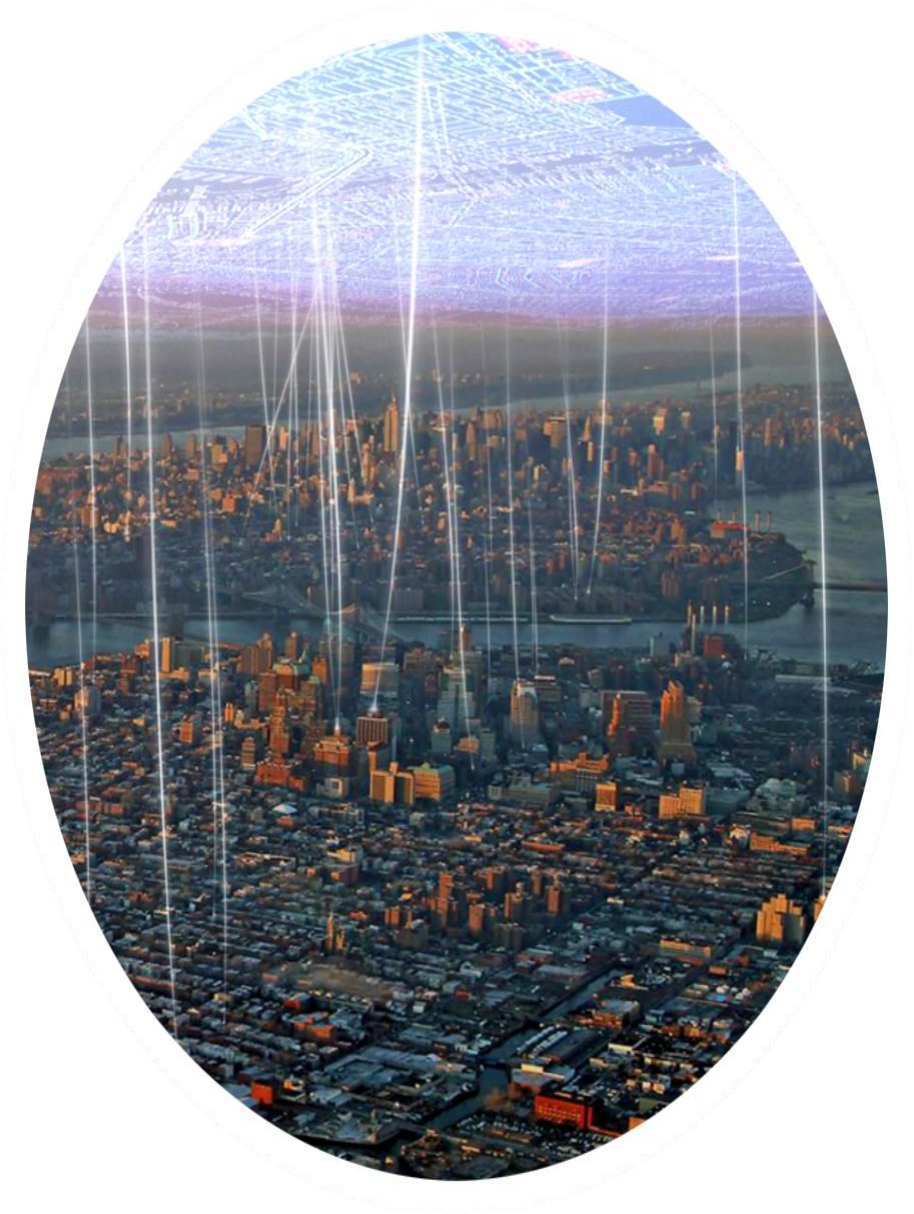
Agenda

- Intel in Embedded
- Embedded Curriculum 2012 Programs
- Call to Action

Intel in Embedded

Intelligent Solutions

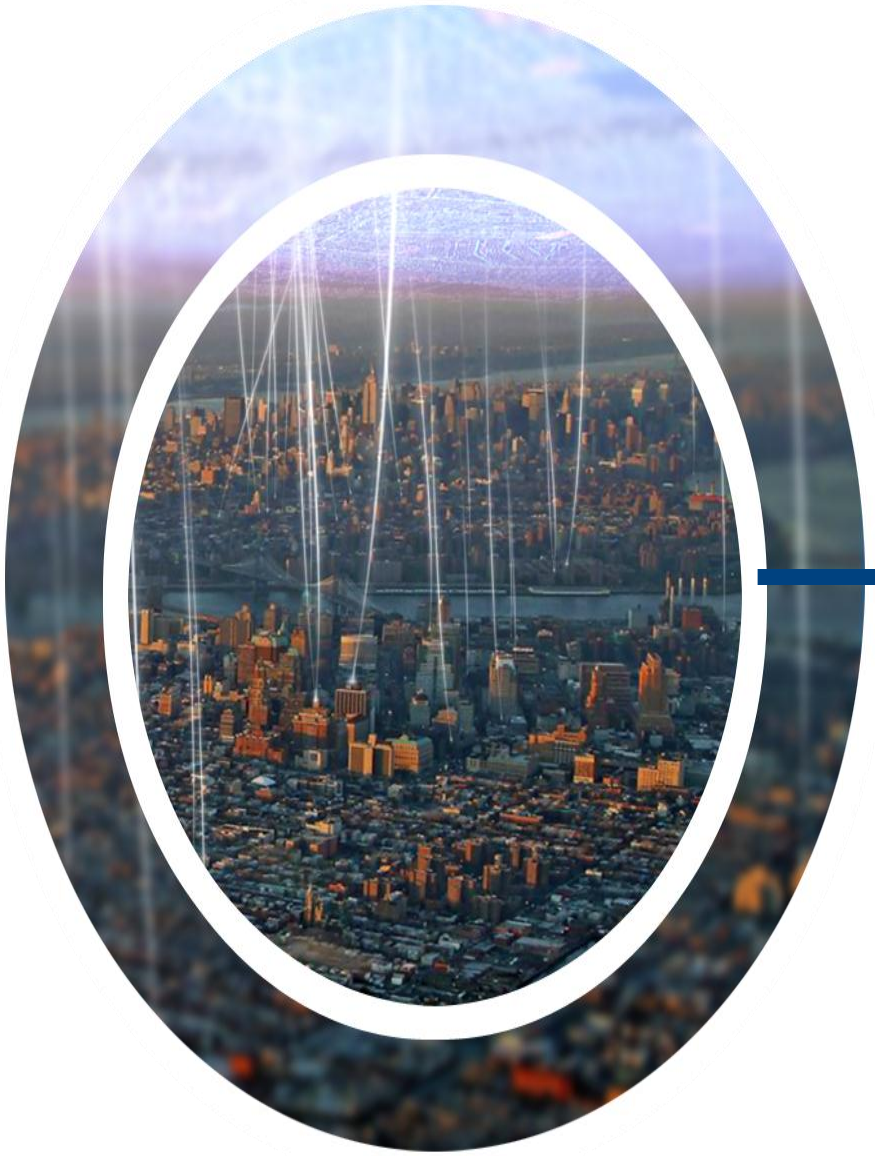
Building a Continuum of Computing Experiences



15 Billion

CONNECTED DEVICES

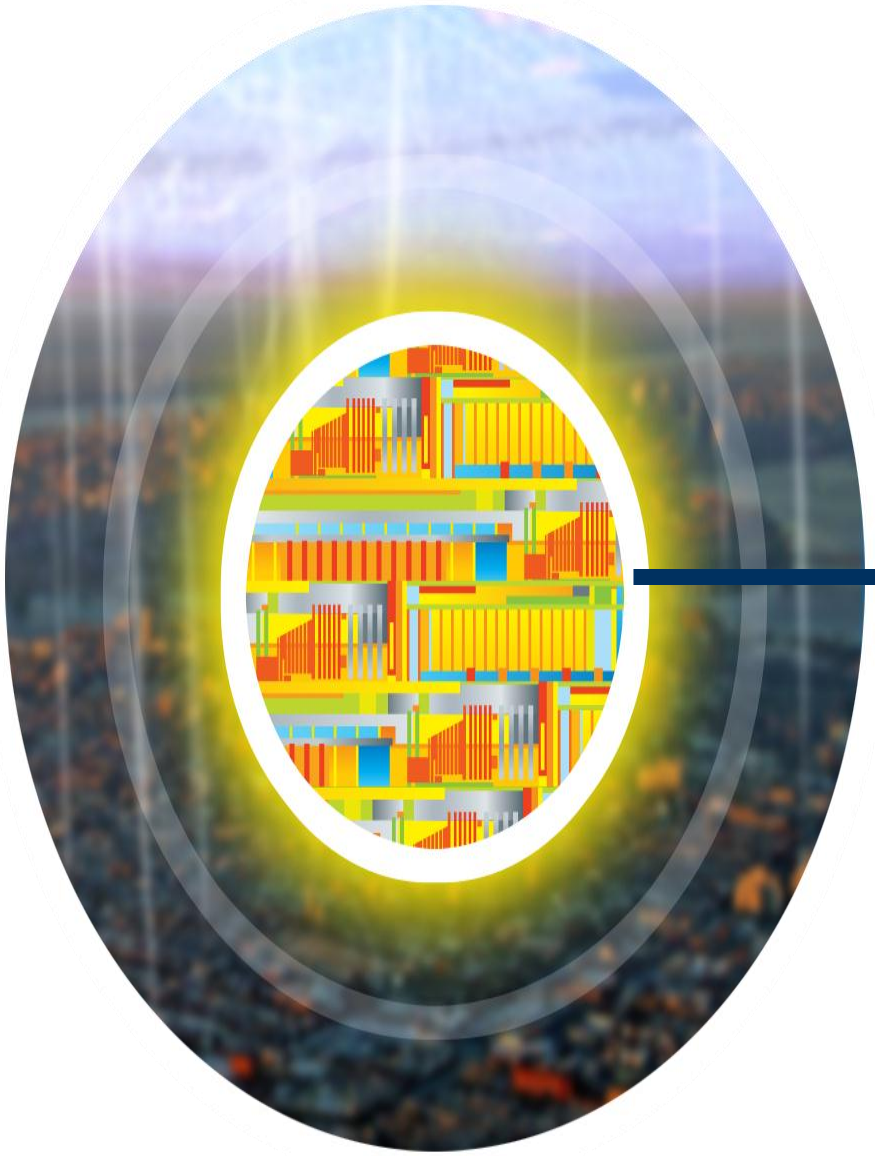
PCs, servers, tablets all the way down to tire pressure sensors



4 Billion

INTELLIGENT SYSTEMS

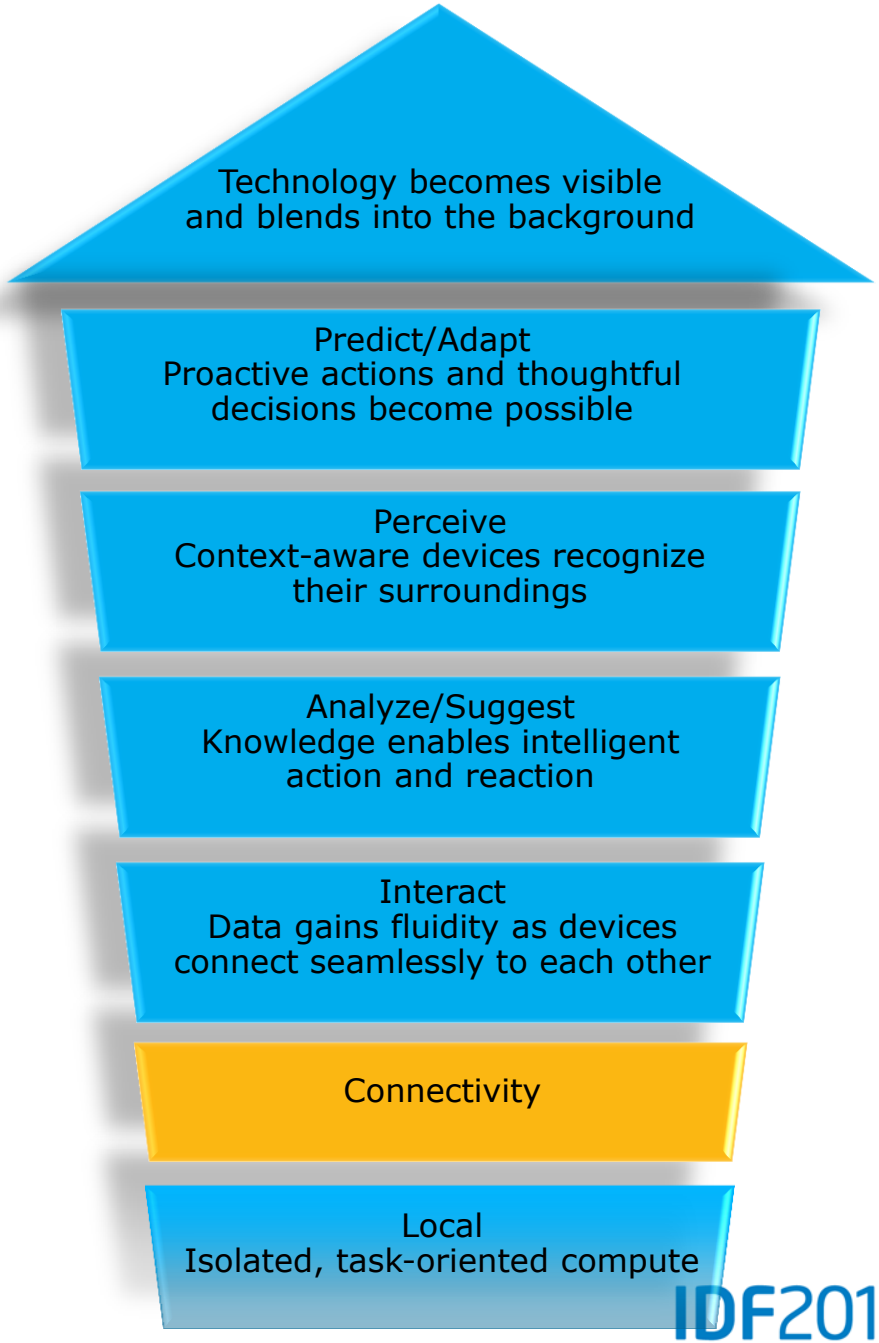
32 bit processing power including PCs, tablets and smart phones



1 Billion

EMBEDDED
INTELLIGENT
SYSTEMS

The Evolution of INTELLIGENT DEVICES

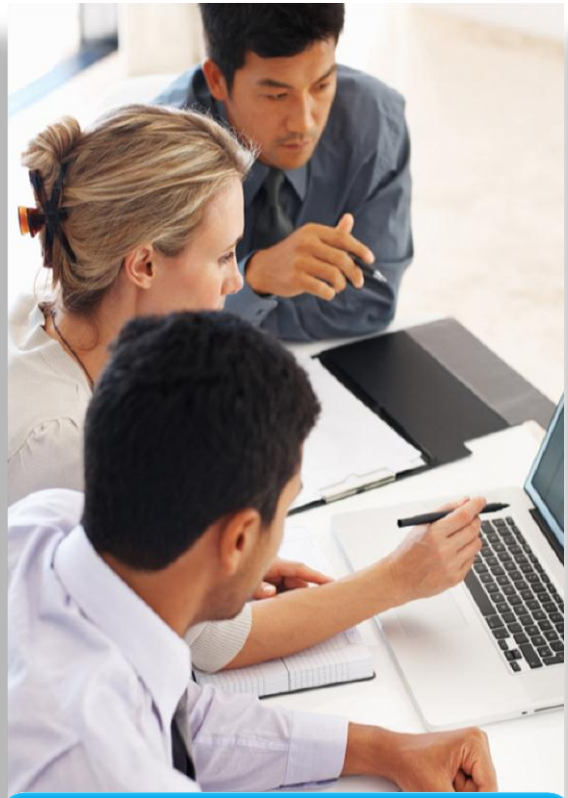


The Evolution of INTELLIGENT DEVICES

Greater Insights

Contextual Analysis

Data Output



Connectivity | Security | Manageability

PERFORMANCE

EVOLVING ARCHITECTURE

Competencies

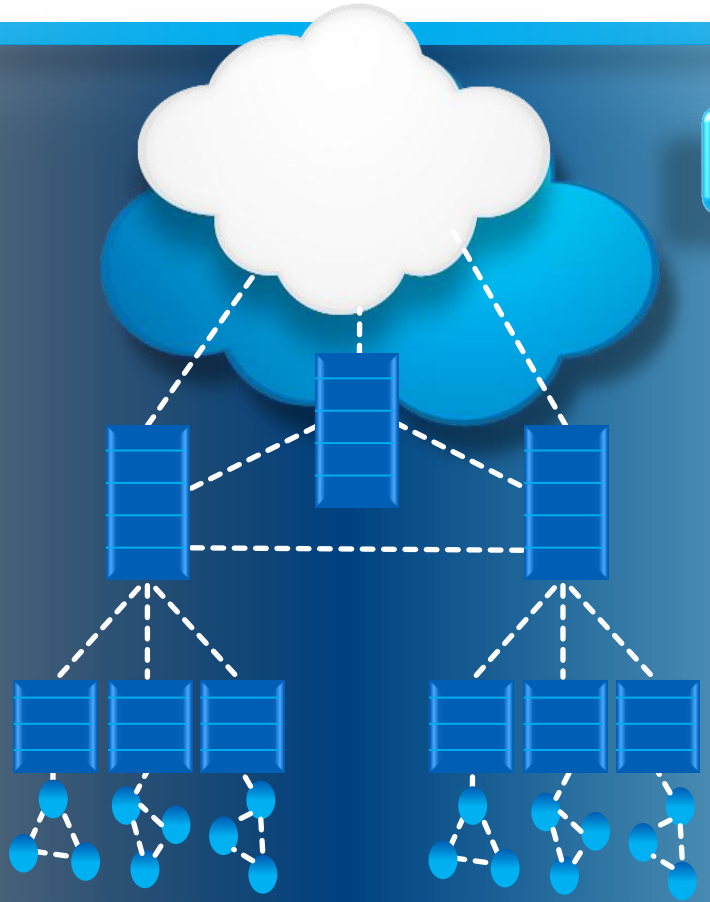
Big Data Analytics

Real Time Analytics

Operating Systems

Sector Workloads

Silicon



Opportunities

Services

Systems

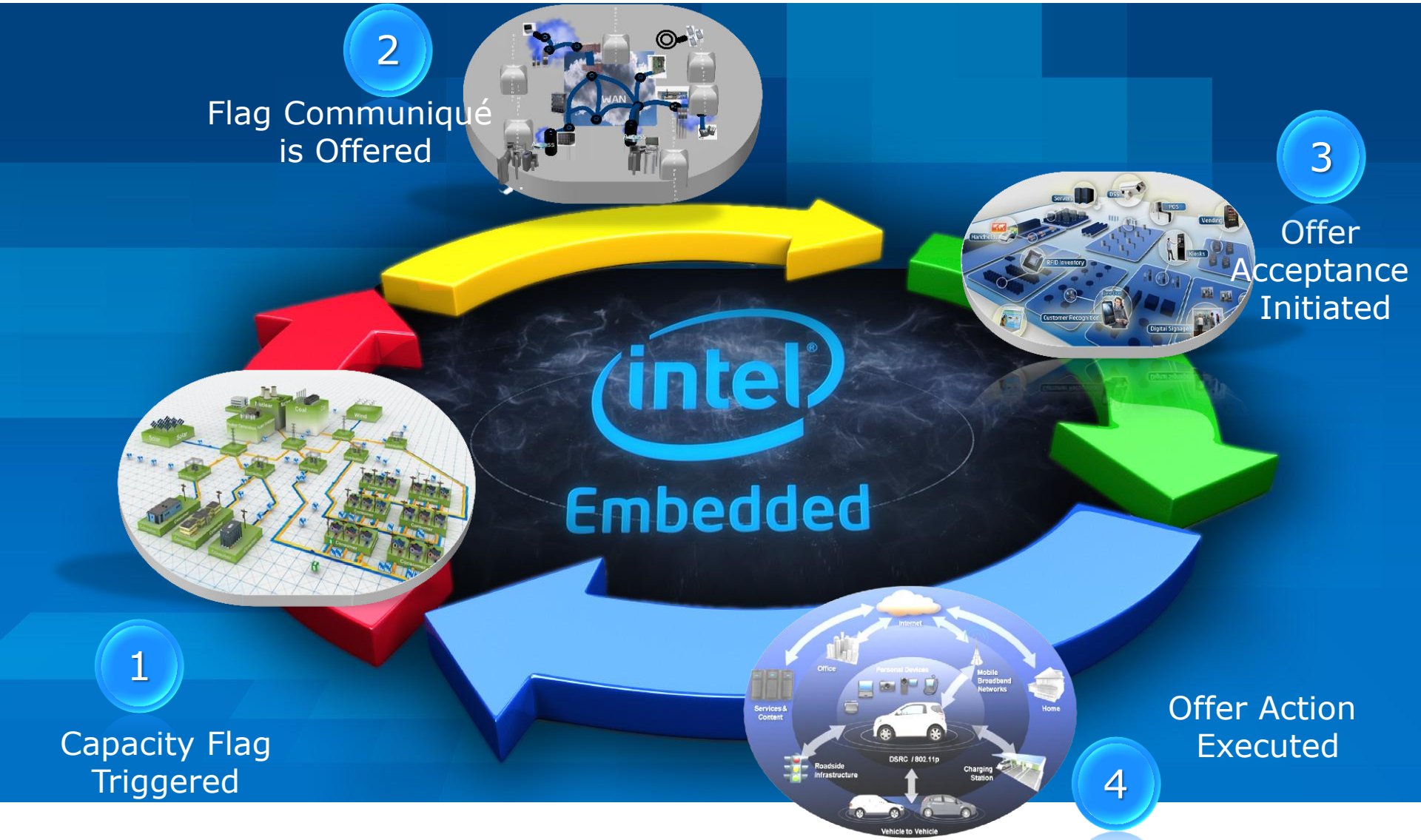
Software

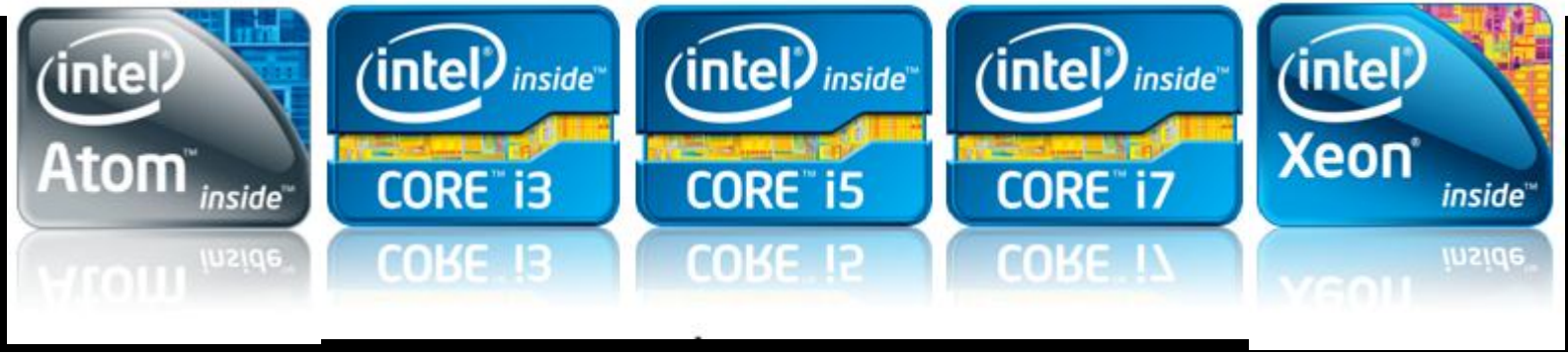
Compute

Sensors

Analytics and Sensing Provide New Opportunity

Delivering Everyday Experiences





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Embedded Curriculum 2012 Program

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Mission and Strategies

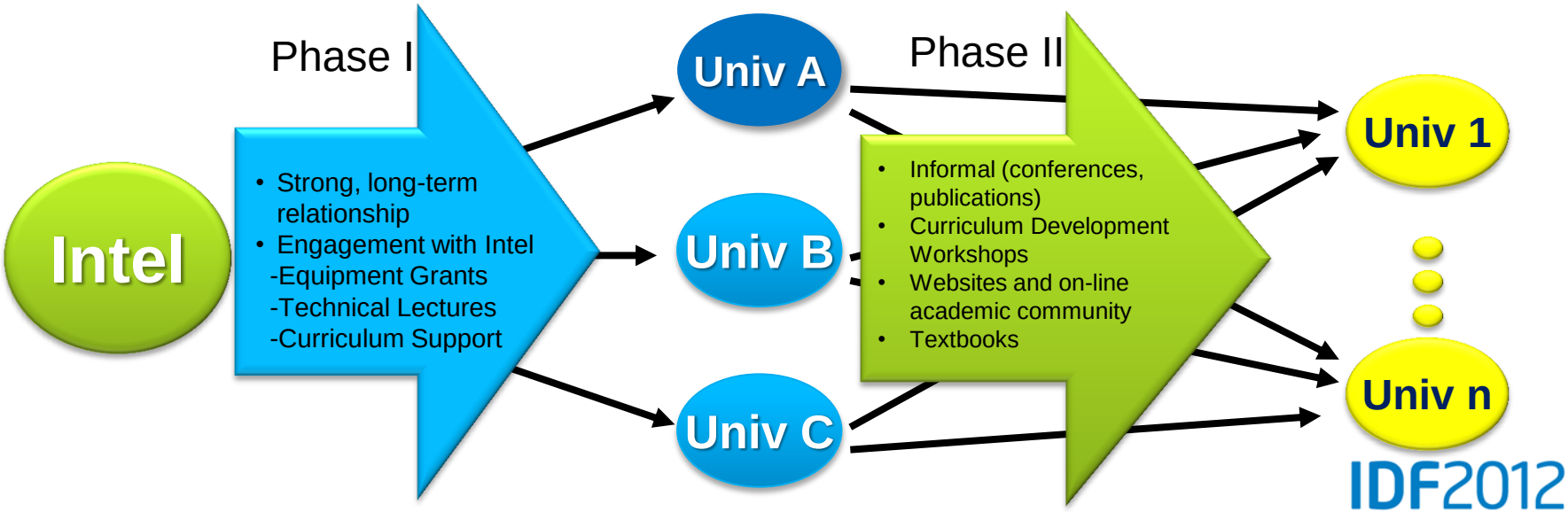
Mission: Prepare the next generation workforce with the latest embedded technology utilized by industry today.

- Strategies:
  - Partner with professors to enhance curriculum with Intel® Atom™ processor hardware and update relevant content
  - Support student contests worldwide to give students hands-on learning experience with Intel Atom processor hardware
  - Support authors as they write texts highlighting Intel Atom processor in the embedded curriculum

Overview of Curriculum Program

Partner with leading universities to utilize the latest technology in the Embedded Courses

- Intel provides hardware and technical support to Professors to update their courses
- Professors provide their knowledge in integrating Intel Architecture into the classroom
- Professors share their curriculum as open source tools to other professors – Intel includes on Curriculum Exchange



Embedded University Web Page

Intel launched the Intel ® Embedded University Program web pages

http://edc.intel.com/training/embedded-university/

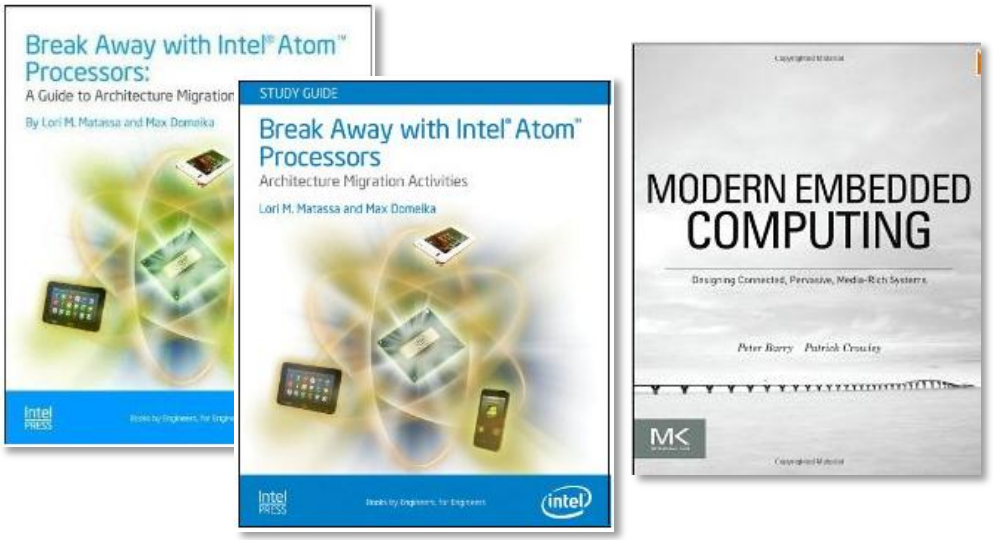
One stop to learn about Intel's embedded support efforts for universities

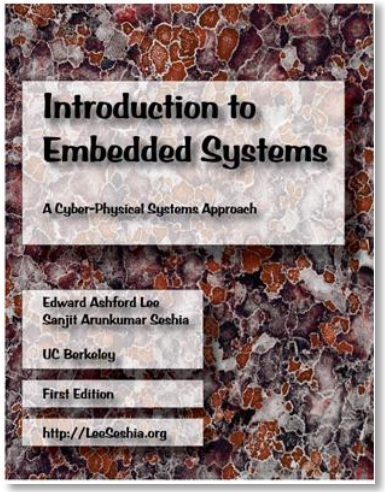
Texts Supporting Embedded Curriculum

- **Intel: Break Away Intel® Atom™ Processors: A Guide to Architecture Migration and Study Guide**
  - **Lori Matassa and Max Domeika**
- **Intel and WA U: Modern Embedded Computing: Designing Connected, Pervasive, Media-Rich Systems**
  - **Peter Barry and Patrick Crowley**
- **UC Berkeley: Introduction to Embedded Systems: A Cyber-Physical Systems Approach**
  - **Edward Lee and Sanjit Seshia**
- **LeeSeshia.org**

Coming

- **Intel® Atom™ Processors based "Embedded System Theory and Development"**
  - **Prof. Guozhi Xu, Prof. Letian Jiang and Dr. Rendong Ying from Shanghai Jiaotong University**
- **India, Russia**

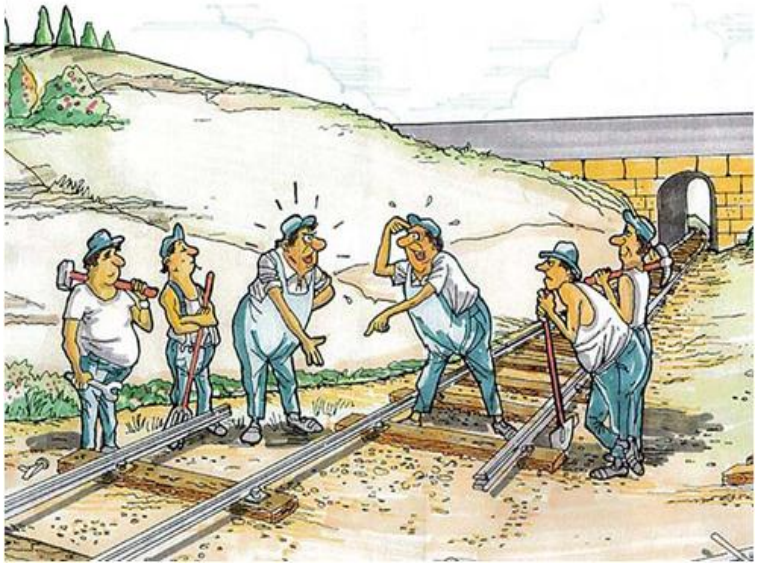




University Research Office

Mission: To influence the strategic directions of Intel and its ecosystem through focused, long-range, interdisciplinary university research programs.

- Embedded Computing
  - Funded Research Programs
    - On-die communication fabrics
    - Biosensors for everyday life
    - Heterogeneous computing
    - Resilient computing
  - Programs in Pipeline
    - Net zero power IA platforms
    - MEMS based sensors
    - Wide area sensor network



University Research Office

- Geo-specific Expansion Strategies:
  - Grassroots development of research program goals
    - Partner with local Intel groups, identify geo expertise
    - Explore co-funding opportunities
    - Build focused research agenda
  - Program structure & size follow from nature of goals
    - Priority given to multidisciplinary challenges
- Research Exploration with Intel Labs China
    - Networking and communication
      - Cloud radio access networks
      - Macro base stations
    - Security

Student Contests Around the World

China - Intel Cup Embedded System Design Contest (ESDC)

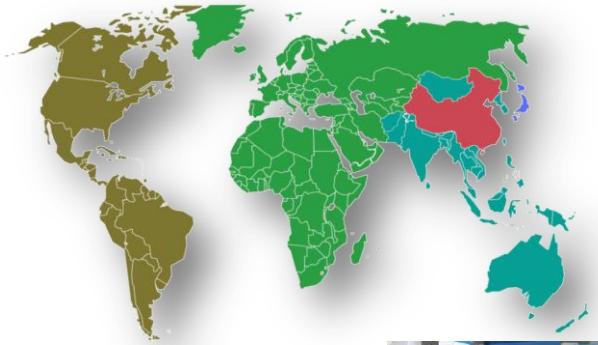
- ***India – Intel India Embedded Challenge 2012***
- ***Mexico – Tech de Monterrey "IMT Design Challenge"***
- ***Malaysia – Innovate Malaysia: Intel Track***
- ***USA - Cornell Cup USA Presented by Intel***
- ***Taiwan – 2012 Embedded System Design Contest***

嵌入梦想 芯动未来
2012 英特尔杯大学生电子设计竞赛
嵌入式系统专题邀请赛
2012 Intel Cup Undergraduate Electronic Design Contest
- Embedded System Design Invitational Contest

2012 Milestone
10 years anniversary
Kick-off in Mar 2012

2012 Coverage
162 teams from 72 universities of 12 countries/ regions

2012 More Innovations on intelligent systems



Nurturing innovation
Innovate Malaysia
Design Competition 2012

Intel® India
Embedded Challenge 2012

CORNELL CUP USA
Presented by intel

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Accomplishments to Date

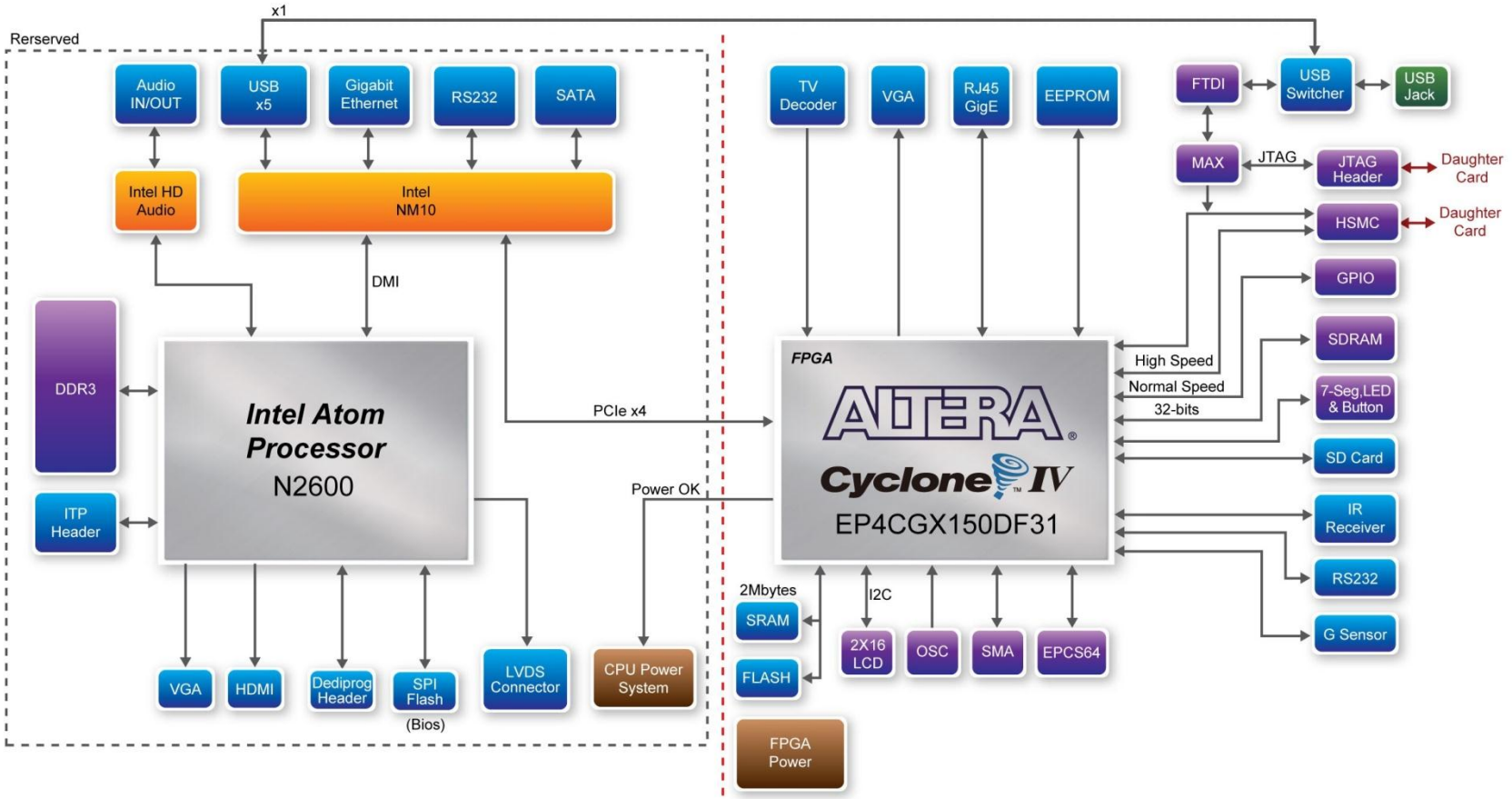
- Over 180 Universities engaged in the program WW
  - 225+ courses updated to include IA
  - 30k students enrolled annually
- Workshops providing Train the Trainer Focus
  - 225+ professors engaged
  - China, Malaysia
- Student Contests
  - Undergraduate focused
  - Focused on skill set development
  - Creating innovation and new business opportunities

Plan for 2012 - 2013

Go Deep: Support at universities already in the program (top schools)

- Identify new courses and new professors at existing universities
- Explore new courses with existing professors
- Consider previous course hardware refresh through proposal process

2012-2013 Hardware Platform

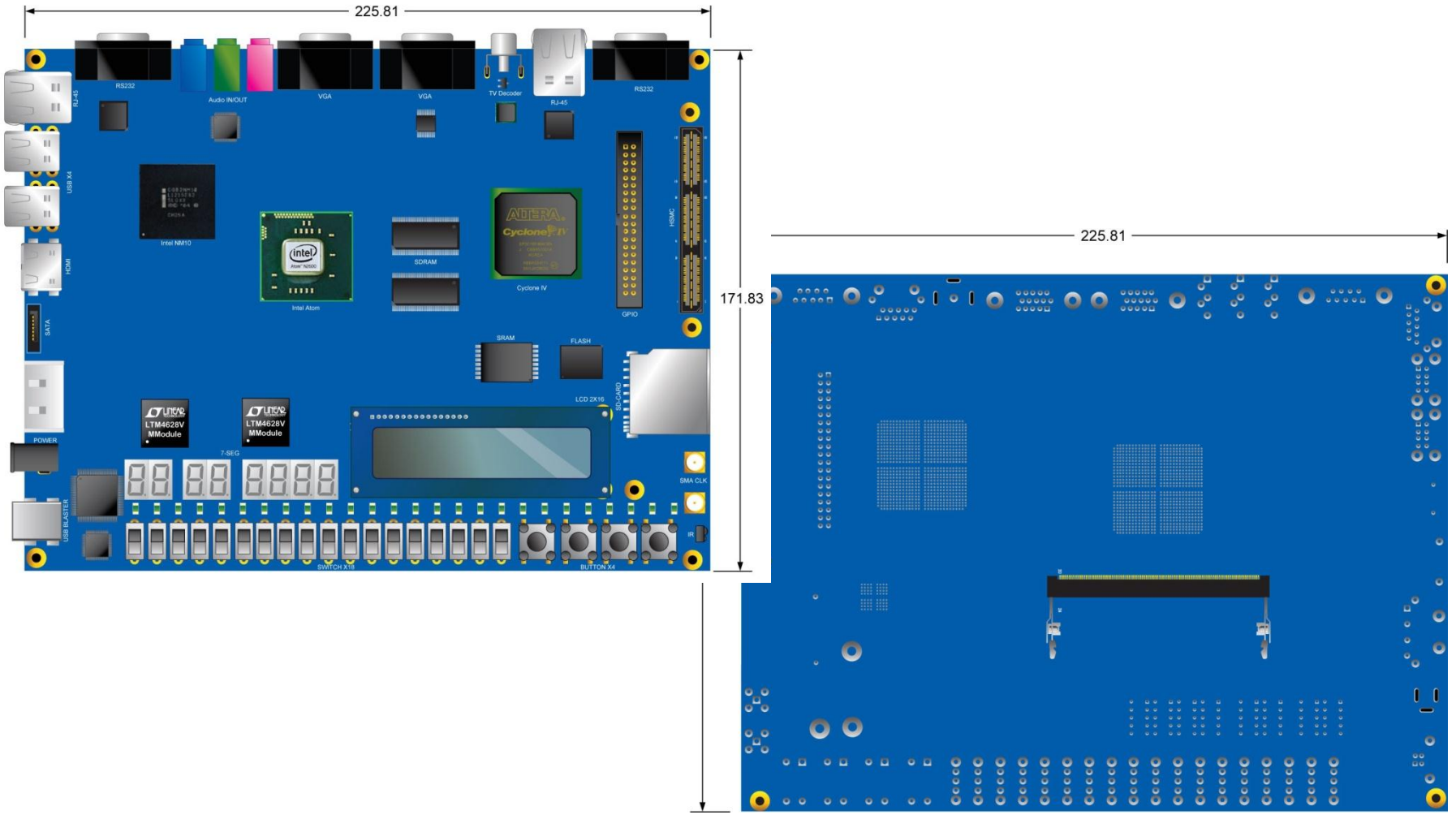


Platform Highlights

- Intel® Atom™ Processor N2600
  - Dual Core (4 logical cores)
  - 1.6GHz
  - 3.5W TDP
- Altera* Cyclone IV FPGA: EP4CGX150
- Standard PCI Express* Connection between Intel Atom and FPGA
- Ready for OpenCL* Compiler from Altera for hardware-software co-design and embedded system training
- Vendor can provide open market boards to universities directly

Altera Cyclone IV FPGA	EP4CGX150
Logic elements (LEs)	149,760
M9K memory blocks	720
Embedded memory (Kbits)	6,480
18-bit x 18-bit multipliers	360
PCIe hard IP block	1
Phase-locked loops (PLLs)	8
Transceiver I/Os	8
Maximum user I/Os	475
Maximum differential channels	216

Top/Bottom Layout View



Computer Science/Computer Engineering Curriculum Objectives

Hardware/Software	*Applications Environments*	*Hardware Interfaces*
Real Time Programming	Security and Secure Applications	System-on-a-chip (SOC) interfaces
Endian Neutral Programming	Power Aware Applications	Communications components
Multi-Core/Multi-Threading	Networking Applications	Memory Technologies
Firmware	Embedded Software Development and Debug tools	Graphics and Video
Virtualization	Reliability and Serviceability, Safety and Certification	Power Management

Hardware Engineering Curriculum Objectives

Hardware Development	***Hardware/Software Partitioning***
Architecture Overview	Offload Architectures
Board/System Design	Creating Application Programming Interfaces (API)
Board/System Validation	Performance Characterization
Thermal Design and Validation	Hardware and Software Design
Hardware Debug Tools and Methodology	

Call to Action

SET THE COURSE

Interact and Collaborate

- Interact with key technical leaders from ISG and Intel Labs
- Collaborate and form partnerships
- Be the liaison and leader
- Work with us to define the Intelligent Systems Architecture

Q&A

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Risk Factors

The above statements and any others in this document that refer to plans and expectations for the first quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "plans," "believes," "seeks," "estimates," "may," "will," "should" and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel's actual results, and variances from Intel's current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company's expectations. Demand could be different from Intel's expectations due to factors including changes in business and economic conditions, including supply constraints and other disruptions affecting customers; customer acceptance of Intel's and competitors' products; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel's products; actions taken by Intel's competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel's response to such actions; and Intel's ability to respond quickly to technological developments and to incorporate new features into its products. Intel is in the process of transitioning to its next generation of products on 22nm process technology, and there could be execution and timing issues associated with these changes, including products defects and errata and lower than anticipated manufacturing yields. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; product mix and pricing; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. The majority of Intel's non-marketable equity investment portfolio balance is concentrated in companies in the flash memory market segment, and declines in this market segment or changes in management's plans with respect to Intel's investments in this market segment could result in significant impairment charges, impacting restructuring charges as well as gains/losses on equity investments and interest and other. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Expenses, particularly certain marketing and compensation expenses, as well as restructuring and asset impairment charges, vary depending on the level of demand for Intel's products and the level of revenue and profits. Intel's results could be affected by the timing of closing of acquisitions and divestitures. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust and other issues, such as the litigation and regulatory matters described in Intel's SEC reports. An unfavorable ruling could include monetary damages or an injunction prohibiting us from manufacturing or selling one or more products, precluding particular business practices, impacting Intel's ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel's results is included in Intel's SEC filings, including the report on Form 10-Q for the quarter ended Oct. 1, 2011.

Rev. 1/19/12

Backup Slides

Computer Science/Computer Engineering Curriculum Objectives

Hardware/Software	*Applications Environments*	*Hardware Interfaces*
Real Time Programming	Security and Secure Applications	System-on-a-chip (SOC) interfaces
Endian Neutral Programming	Power Aware Applications	Communications components
Multi-Core/Multi-Threading	Networking Applications	Memory Technologies
Firmware	Embedded Software Development and Debug tools	Graphics and Video
Virtualization	Reliability and Serviceability, Safety and Certification	Power Management

CS/CE Curriculum Objectives

Hardware/Software	***Applic Enviro***	
Real Time Programming	Security a Applic	
Endian Neutral Programming	Power Aware	
Multi-Core/Multi-Threading	Networking	
Firmware	Embedded Developmen to	
Virtualization	Reliability and Serviceability, Safety and Certification	Power Management

Real Time Programming

- Hard Real-Time, Soft Real-Time
- Run to completion/Pre-Emption
- Interrupt Service Routines, Priorities, Masking
- Interrupt Latency
- Direct Memory Access controllers
- Real Time Clock
- Interrupt sources
  - PCIe Message Signal Interrupt
  - Inter-processor interrupt
  - Advanced Programmable Interrupt Controller
  - Hardware arbitration

CS/CE Curriculum Objectives

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Endian Neutral Programming

- Code Portability
- Compile Time Controls
- Run Time Controls
- Network byte ordering
- Data Storage and Shared Memory
- Byte Swap Macros
- Data Transfer
- Data Types

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CS/CE Curriculum Objectives

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Multi-Core/Multi-Threading

- Elements of parallel programming and multi-threading
  - Data and Task parallelism
  - Inter-process communication and thread synchronizations
  - Re-Entrant and Thread Safe Programming
- Non-Uniform Memory Architecture Programming (NUMA)
- Programming with threading APIs
- Threading Building Blocks OpenMP
- Solutions to common parallel programming problems
- Debugging and testing multi-threaded applications
- Software development tools for multi-threading

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Firmware

- System initialization - Boot loaders/BIOS
- Firmware and Driver development
- ROM image
- Microcode
- Application Programming Interface (API)

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CS/CE Curriculum Objectives

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Virtualization

- Hypervisors
- CPU virtualization
- Memory virtualization
- Device emulation
- Interrupt delivery
- Network virtualization
- I/O Virtualization
- PCI-SIG I/O Virtualization (IOV)
- Single Root IOV (SR-IOV)

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CS/CE Curriculum Objectives

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Real Time Programming	Security a Applic	
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Security and Secure Applications

- Internet Protocol Security (IPsec)
- Secure Sockets Layer (SSL)
- Security Algorithms (DES, 3DES, AES, etc.)
- Cryptographic hash function (SHA-x, MD5, etc.)
- Private and Public-key encryption
- Applications
  - Statefull Firewall
  - Intrusion Detection/Prevention System
- Open source implementations (OpenSSL)

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CS/CE Curriculum Objectives

Hardware/Software	***Applic Enviro***	
Real Time Programming	Security a Applic	
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Power Aware Applications

- Dynamic Power Management (DPM)
- Profile of application over memory banks
- Power-aware scheduling
- Dynamic Voltage/Frequency Scaling (DVS)
- Shutting down unused peripherals
- System Sleep Modes

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CS/CE Curriculum Objectives

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Networking

- Network stack/OSI Model
- Wireless 3G/4G technolgoies
- TCP/IP Protocol
- IPV4/IPV6
- Bluetooth
- Ethernet/IEEE 802.x Specifications
- Routing protocols
- Proxy

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CS/CE Curriculum Objectives

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Embedded Software Development and Debug tools

- Cross Development Environments
- Assemblers/compiler/linkers
- Debuggers
- Software profiling tools
- Code coverage tools
- Open Source vs Proprietary tools
- JTAG debug
- Single Stepping
- Virtual memory mapping

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CS/CE Curriculum Objectives

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Reliability and Serviceability

- Parity or ECC protection
- Cyclic redundancy check checksums for data
- Lock-step to perform master-checker
- Avoid single point of failures
- Hot swapping of components
- Partitioning/domaining of computer components
- Computer clustering capability
- Virtual machines
- Temperature sensors
- Failover capability

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CS/CE Curriculum Objectives

System-on-a-chip (SOC) interfaces

- Memory interfaces
- Industry standards such as USB, Ethernet, USART, SPI, SATA, I2S/I2C, CAN
- I/O Interfaces such as PCI, PCI-X, PCI-Express
- Analog interfaces including ADCs and DACs.
- Voltage regulators and power management circuits

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		Hardware Interfaces
		System-on-a-chip (SOC) interfaces
		Communications components
		Memory Technologies
		Graphics and Video
Virtualization	Reliability and Serviceability, Safety and Certification	Power Management

CS/CE Curriculum Objectives

Communications components

- 10/100/1000 Ethernet
- 10G/40G Ethernet
- Bluetooth
- Zigbee
- WiFi
- WiMax
- Blu-Ray

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	cations nments	***Hardware Interfaces***
	nd Secure cations	System-on-a-chip (SOC) interfaces
	e Applications	Communications components
	Applications	Memory Technologies
	d Software t and Debug ols	Graphics and Video
Virtualization	Reliability and Serviceability, Safety and Certification	Power Management

CS/CE Curriculum Objectives

Memory Technologies

- DRAM (DDR, DDR2, DDR3, RDRAM, SDRAM)
- Flash
- SATA
- Solid State Drives (SSD)
- SD/MMC

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…cations …nments	***Hardware Interfaces***
…nd Secure …cations	System-on-a-chip (SOC) interfaces
… Applications	Communications components
… Applications	Memory Technologies
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CS/CE Curriculum Objectives

Graphics and Video

- Embedded 2D/3D Graphics
- Video Playback, Encode, Decode
- Graphics Processing Units (GPU)
- Media Accelerators
- Media Formats (H.264, MPEG2, MPEG4)
- Audio Formats
- DVD/BlueRay
- Graphics Quality Metrics

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	…cations …nments	***Hardware Interfaces***
	…nd Secure …cations	System-on-a-chip (SOC) interfaces
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CS/CE Curriculum Objectives

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		Applications	Memory Technologies
		d Software t and Debug ols	Graphics and Video
Virtualization	Reliability and Serviceability, Safety and Certification		Power Management

Power Management

- C-states
- Speedstep
- Measuring Power Consumption
- Thermal design power
- Thermal considerations
- Heat Sink technology
- Cooling

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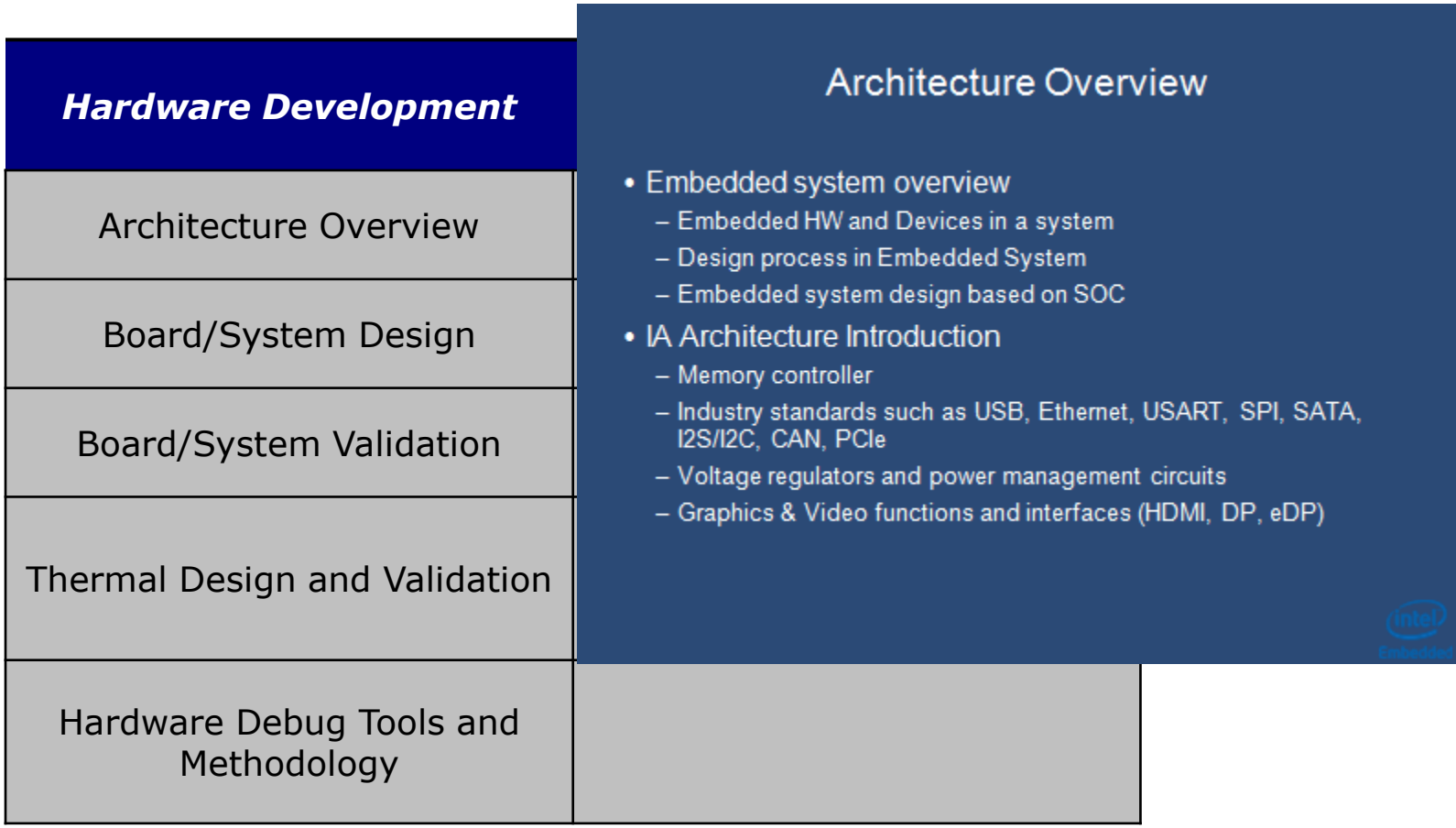
Hardware Curriculum Objectives

Hardware Development	***Hardware/Software Partitioning***
Architecture Overview	Offload Architectures
Board/System Design	Creating Application Programming Interfaces (API)
Board/System Validation	Performance Characterization
Thermal Design and Validation	Hardware and Software Design
Hardware Debug Tools and Methodology	

Hardware Curriculum Objectives



Hardware Curriculum Objectives

Hardware Development
Architecture Overview
Board/System Design
Board/System Validation
Thermal Design and Validation
Hardware Debug Tools and Methodology

Board/System Design

- Low power and power aware design
- Dynamic Power Management (DPM)
- Profile of application over memory banks
- Power-aware scheduling
- Dynamic Voltage/Frequency scaling (DVS)
- Shutting down unused peripherals
- System Sleep Modes
- Design documentation
- Schematic CaptureTools

Hardware Curriculum Objectives

Hardware Development
Architecture Overview
Board/System Design
Board/System Validation
Thermal Design and Validation
Hardware Debug Tools and Methodology

Board/System Validation

- Board Design
  - Board design flow and rules
  - Layout
  - Debug tools
- Board Validation
  - Validation flow
  - Basic function
  - Power deliver
  - Single integrity
  - Thermal
  - Compatibility
  - System level: vibration/shock

Hardware Curriculum Objectives

Hardware Development
Architecture Overview
Board/System Design
Board/System Validation
Thermal Design and Validation
Hardware Debug Tools and Methodology

Thermal Design and Validation

- Thermal Modeling
  - Power Estimation/Modeling
  - Performance Estimation/Modeling
  - Reliability Estimation/Modeling
- Primary/Secondary heat flow path
- Interconnect thermal characteristics
- I/O Pads to PCB thermal characteristics
- Airflow
- Component Placement
- Thermal Interface Material
- Thermal Validation techniques

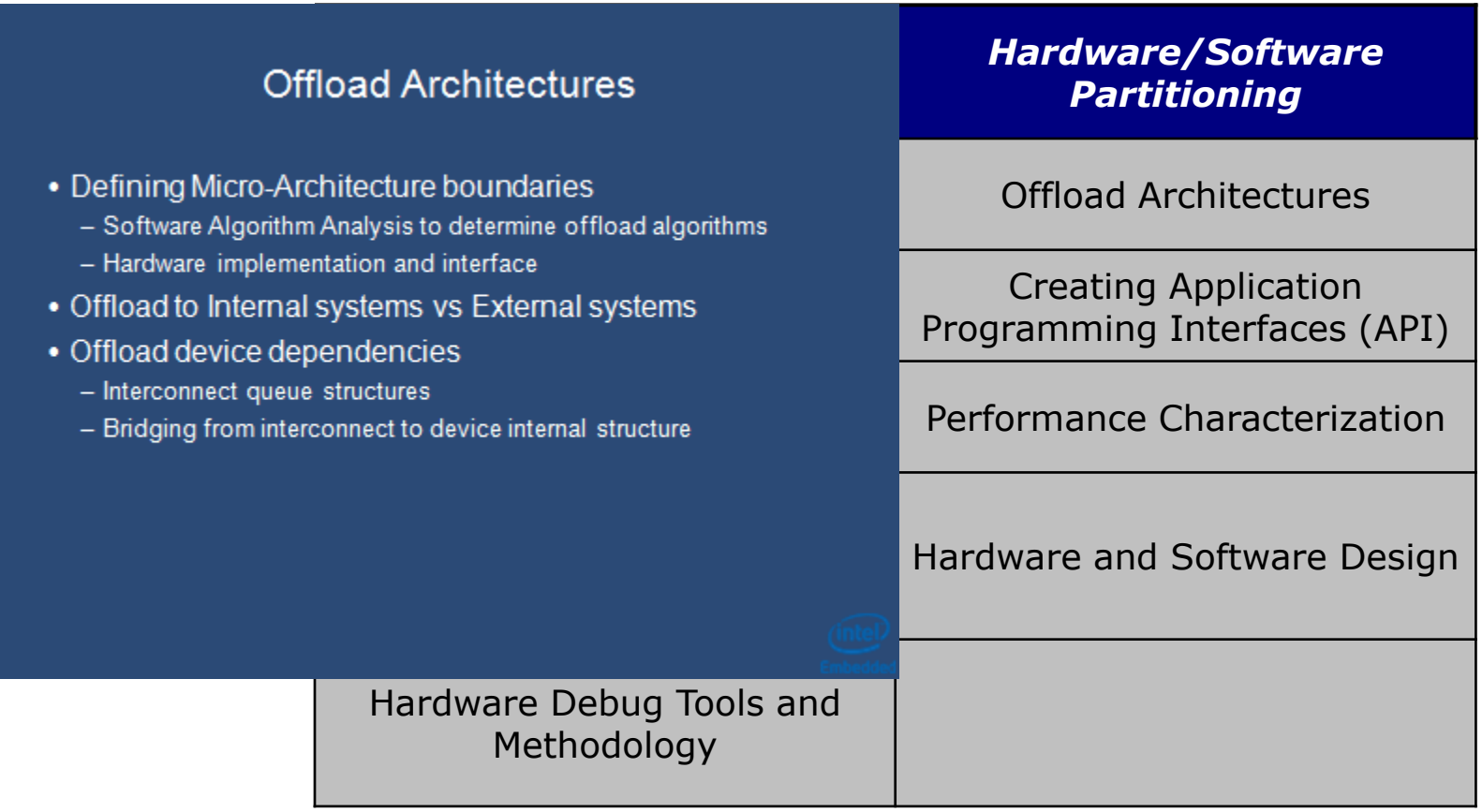
Hardware Curriculum Objectives

Hardware Development
Architecture Overview
Board/System Design
Board/System Validation
Thermal Design and Validation
Hardware Debug Tools and Methodology

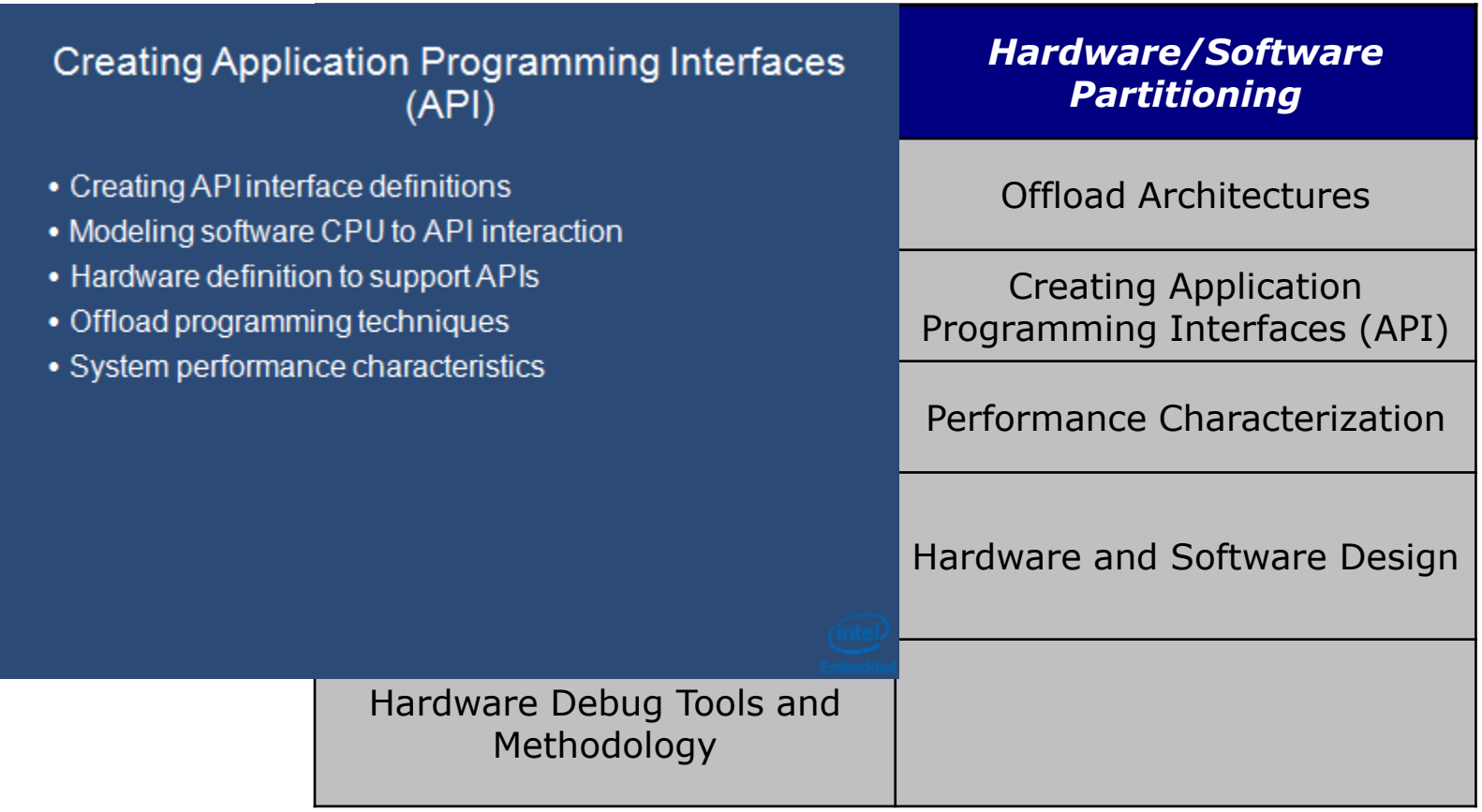
Hardware Debug Tools and Methodology

- Joint Test and Access Group (JTAG) IEEE Std. 1149.1-1990
- Design in technologies
  - Boundary Scan
  - TAP Controller Interface
  - XOR Chain
  - Voltage and Ground Rail Testing
- Test equipment: Logic analyzers, Oscilloscopes

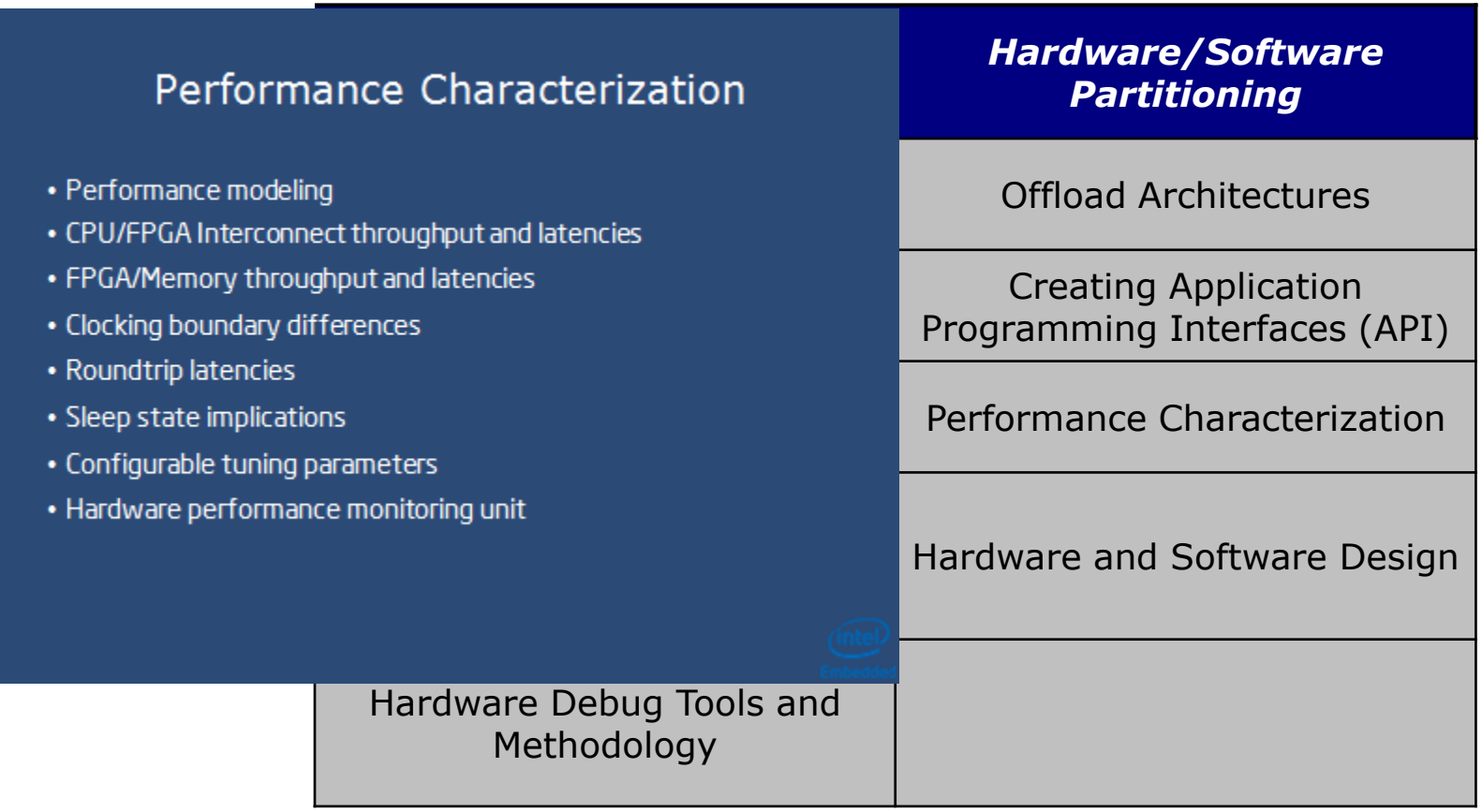
Hardware Curriculum Objectives



Hardware Curriculum Objectives



Hardware Curriculum Objectives



Hardware Curriculum Objectives