# Nios II Embedded Design Suite Release Notes

2015.06.17

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These release notes cover versions 13.1 through 15.0 of the Altera® Nios® II Embedded Design Suite (EDS). These release notes describe the revision history for the Nios II EDS.

For the most recent list of errata for the Nios II EDS, search the Knowledge Base under **Support** on the Altera website. You can use the Knowledge Base to search for errata based on the product version affected and other criteria.

**Related Information**

**Altera Knowledge Base**

## Product Revision History

The following table shows the revision history for the Nios II EDS.

**Table 1: Nios II Embedded Design Suite Revision History**

| Version | Date | Description |
|---|---|---|
| 15.0 | June 2015 | <ul><li>New MAX® 10 analog-to-digital converter (ADC) HAL driver</li><li>New Quad Serial Peripheral Interface (QSPI) HAL Driver</li><li>Enhancements to the MAX 10 ADC HAL Driver</li><li>HAL drivers for MAX 10 remote update IP core</li><li>Nios II GNU toolchain upgraded to v4.9.1, including support for new compiler options</li><li>Nios II Linux kernel and toolchain components have been accepted upstream</li></ul> |
| 14.1 | December 2014 | <ul><li>Introduces Nios II Gen2</li><li>The original Nios II processor is now called the Nios II Classic processor.</li><li>Upgrade to Eclipse® 4.3</li><li>New embedded IP support</li><li>Nios II toolchain improvements:<ul><li>Link Time Optimization enabled [-flto]</li><li>Upgrades: GCC v4.8.3, Newlib v1.18, GDB v7.7</li><li>Windows host compile/build time performance improvements</li></ul></li><li>64-bit support for all host tools</li><li>Nios II Gen2 support for MAX 10</li></ul> |

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| Version | Date | Description |
|---------|------|-------------|
|  |  | • `alt-file-convert` (BETA) tool added<br>• Quad serial configuration (EPCQ) BootLoader and EPCQ HAL Support<br>• Upgraded EPCQ Controller IP (x4, L support) |
| 14.0 | July 2014 | • Verified with Quartus II v14.0 software<br>• 32-bit host support removed<br>• Added support for Nios II Gen2 processor cores<br>• Resolved runtime stack checking issues<br>• Resolved compiler long jump support issue<br>• Resolved linking issue with newlib for Floating Point Hardware 2 |

For more information about Nios II EDS features, refer to the Nios II handbooks.

**Related Information**

- **Nios II Classic Processor Reference Handbook**
- **Nios II Classic Software Developer's Handbook**
- **Nios II Gen2 Processor Reference Handbook**
- **Nios II Gen2 Software Developer's Handbook**

## Nios II EDS v15.0 Updates

The v15.0 Nios II EDS includes the following new and enhanced features:

- New MAX 10 analog-to-digital converter (ADC) HAL driver
- New Queued Serial Peripheral Interface (QSPI) HAL Driver
- Enhancements to the MAX 10 ADC HAL Driver
- Nios II GNU toolchain upgraded to v4.9.1

  - Improved support for link time optimization (`-flto`)
  - More control over global pointer optimization using `-mgpopt=[none, local, global, data, all]`
  - Null pointer check (new in GNU v4.9.1) can be disabled with `--fno-delete-null-pointer-checks`
- Nios II Linux kernel and toolchain components have been accepted upstream

High-profile issues resolved:

- EPCQ HAL driver issues corrected
- Custom newlib generator fixed in Windows Nios II terminal
- stdin now working correctly on Windows

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# Nios II EDS v14.1 Updates

## Nios II Gen2 Processor Core

The last version of the Nios II is 14.0 and it is named Nios II Classic. Nios II versions after this build are called Nios II Gen2.

The Nios II Gen2 processors are binary compatible with the Nios II Classic processors, but have the following new features:

- Options for a 64-bit address range
- Optional peripheral memory region
- Faster and more deterministic arithmetic instructions

## New Embedded IPs for 14.1

The list of new IP includes:

- HPS Ethernet converter IPs - These allow you to assign the HPS Ethernet I/O pins to FPGA I/O pins and convert them from GMII format to RGMII or SGMII.

  **Note:** This is very helpful if you are pin limited by the HPS I/O.
- New device family-specific IP cores:

  - Arria 10 - TPIU trace IP. Trace is the ultimate tool in runtime software debug, much like Signaltap is for FPGA development. This IP enables developers to export the ARM® Cortex™-A9 trace debug signals to external pins so that trace debug modules like Lauterbach® or ARM Dstream, can be connected to the A10 SoC Cortex-A9.
  - Max 10 - New IPs that deliver Qsys compatible interfaces to the Max10 ADCs and user flash. These new IPs are used in the Max10 example designs.

The 14.1 release has new example designs that demonstrate:

- Max 10 sleep mode, for low power applications
- Analog I/O for developers that want to use the integrated ADCs
- Dual configuration capability from the Max 10 on-chip configuration flash memory

The Cyclone® V and ArriaV SoC golden system reference designs (GSRDs) have also been updated to support the 14.1 ACDS and SoC EDS releases, this means that they will automatically include the SoC software fixes in 14.1 like the PLL workaround in the preloader.

## 64-Bit Host Support Enhanced

In this release, 64-bit capability was added to the following tools:

- 64-bit nios2-gdb-server
- 64-bit nios2-flash-programmer
- 64-bit nios2-terminal

**Note:** Within ACDS, at least two GDB servers and two flash programmers are shipped.

## Upgrades to the Eclipse Environment

The Eclipse environment has been upgraded to version 4.3 to bring the benefits of the newer environment to the Nios II development suite.

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There are command line option differences between GCC v4.8.3 and the previously supported version. If you have an existing project created with a previous version, you need to update your makefiles or regenerate your board support package (BSP).

The Free Software Foundation provides the downloads available under **GCC Download** and full GCC release notes are available under **GCC Releases**.

**Related Information**

[http://gcc.gnu.org/](http://gcc.gnu.org/)

## Upgrades to the Nios II GNU Toolchain

The following tools have been upgraded:

- GCC to version 4.8.3
    - Link time optimization (`[flto]`) enabled
- GDB to version 7.7
- newlib to version 1.18

The build environment on the windows host platform has been optimized to give faster build times. For example, building the basic webserver application now takes one-third of the time it used to.

## Additional Support for Max10

In this release, there is added support for Max10 through the addition of memory initialization and bootload support for the user flash memory.

There is a beta version of a new file conversion utility, called alt-file-convert, that makes it easier to get your data into the correct format for loading into flash.

## Upgrades to the EPCQ IP Peripheral

HAL software and bootloader support for the upgraded EPCQ soft IP peripheral has been added.

The EPCQ IP core has been upgraded to add support for x4 mode and L devices, giving faster access to the EPCQ device from Nios or other FPGA based masters.

# Nios II EDS v14.0 Updates

## 64-Bit Host Support

The Nios II Software Build Tools (SBT) v14.0 only supports 64-bit host systems.

**Note:** 32-bit hosts are no longer supported.

The following Nios II utilities have been moved to the Quartus II product:

- **nios2-gdb-server**
- **nios2-flash-programmer**
- **nios2-terminal**

## Run-time Stack Checking

In earlier versions of the Nios II EDS, if run-time stack checking was enabled, the Nios II system could become unresponsive. This issue is resolved in v14.0.

## Long Jump Support

In earlier versions of the Nios II EDS, the compiler did not correctly support long jumps (outside a 256-MB address range). This issue is resolved in v14.0.

## Floating Point Hardware 2 Support

To fully support Floating Point Hardware 2, you must recompile the newlib C library. In the Nios II EDS v13.1, the linker failed to link the recompiled C library with the application. This issue is resolved in v14.0.

## Qsys Bridge Support

Starting with v14.0, the Nios II EDS supports the Address Span Extender and IRQ Bridge cores.

## Nios II Gen2 Processor Support

### The Nios II Gen2 Processor Core

In v14.0, the Nios II processor core includes a preview implementation of the Nios II Gen2 processor core, supporting Altera's latest device families. The Nios II Gen2 processor core delivers size and performance similar to the original Nios II processor, and is compatible with Nios II Classic processor code at the binary level.

The tool flow and HAL include options to support Nios II Gen2 features. The workflow for generating BSPs and building software is the same, but BSPs generated for the Nios II Classic processor must be regenerated.

### HAL Support for the Nios II Gen2 Processor

The Nios II Hardware Abstraction Layer (HAL) is extended to support the following Nios II Gen2 features:

- A 32-bit address range
- Peripheral (uncached) memory regions
- ECC protection on data cache and TCMs in the Nios II/f core

### Nios II Gen2 Processor and MAX 10 FPGA Support

#### Nios II Gen2 Processor Cores and MAX 10 FPGA Support

MAX 10 FPGA devices are supported by the Nios II Gen2 processor, but not by the Nios II Classic processor. To implement a Nios II system on a MAX 10 device, you must use the Nios II Gen2 processor core.

The Altera On-chip Flash memory component, introduced in 14.0, enables Avalon-MM access to on-chip MAX 10 user flash memory. With this component, the Nios II boot copier can copy code to RAM from the MAX 10 user flash memory.

**Tool Support for the MAX 10 FPGA**

The HAL adds basic driver support for the MAX 10 analog to digital (A/D) converter.

The Altera device programming utilities are updated to support programming the MAX 10 user flash memory.

## What's New in v14.0a10: the Nios II Gen2 Processor and Arria 10 FPGA Support

Arria 10 FPGA devices are supported by the Nios II Gen2 processor, but not by the classic Nios II processor. To implement a Nios II system on an Arria 10 device, you must use the Nios II Gen2 processor core.

# Nios II EDS v13.1 Updates

## GCC Upgraded to 4.7.3

In v13.1, the Nios II Software Build Tools (SBT) have been updated to support the v4.7.3 version of GCC.

There are command line option differences between GCC v4.7.3 and the previously supported version. If you have an existing project created with a previous version, you need to update your makefiles or regenerate your board support package (BSP).

**Note:** GCC v4.7.3 adds several new warnings and messages. If you used the `-Werror` command-line option in the previous version, you might see unexpected errors generated by the new warnings.

For details about the Nios II GCC 4.7.3 implementation, refer to **Nios II GNU toolchain upgrade from GCC 4.1.2 to GCC 4.7.3** in the Altera **Knowledge Base**.

The Free Software Foundation provides a guide to porting to GCC 4.7, documenting common issues. This guide can be found on **GCC, the GNU Compiler Collection**, under **Porting to GCC 4.7**. Full GCC release notes are available under **GCC Releases**.

**Related Information**

- **Altera Knowledge Base**
- **http://gcc.gnu.org/**

## Enhanced Floating Point Custom Instruction Support

In v13.1, Qsys adds an option to select a new floating point custom instruction set component, Floating Point Hardware 2.

To take advantage of software support for the Floating Point Hardware 2 instructions, include **altera_nios_custom_instr_floating_point_2.h**, which forces GCC to call newlib math functions (rather than GCC built-in math functions). Altera recommends that you recompile newlib with for optimum performance.

**Note:** Do not use the `-mcustom -fpu-cfg` command-line option for GCC. This option does not support the Floating Point Hardware 2 instructions.

The Nios II software build tools (SBT) add individual `-mcustom` commands to the makefile to support the Floating Point Hardware 2 custom instructions.

## ECC Support

Starting in v13.1, the Nios II Processor parameter editor lets you enable ECC protection for the RAMs in the processor core and the instruction cache.

By default, ECC is not enabled on reset. Therefore, software must enable ECC protection. Software can also inject ECC errors into RAM data bits to support testing of the ECC exception handler and event bus.

The Nios II Hardware Abstraction Layer (HAL) is extended to support ECC initialization and exception handling.

## Universal Boot Copier

In v13.1, the Nios II boot copier is upgraded to support more types of flash devices.

The upgraded boot copier is called the universal boot copier.

The Nios II boot copier copies the application binaries from flash devices to volatile memory. The flash memory is laid out with the FPGA image at the lowest memory address, followed by the Nios II application binary images.

In previous product releases, the FPGA image size was fixed for each device family. However, for devices in the Cyclone V, Stratix V, and Arria V families, the image size varies depending on the following variables:

- Flash type: Quad-output (EPCQ) or single-output (EPCS) Enhanced Programmable Configuration device
- Flash device capacity: 128 or 256 Mbits
- Compression
- Serial peripheral interface (SPI) configuration: ×1 or ×4
- Device layout: single or cascaded

It is difficult for the boot copier to identify the current combination so that it can use the appropriate image size, and any algorithm might fail to support future configurations.

To solve this problem, a header is added to the FPGA image to specify the image size. By using the image size from the header, the universal boot copier can work with any flash configuration in current or future devices.

The **sof2flash** utility is updated to support the universal boot copier.

This change does not impact to the ability of the FPGA control block to automatically program the FPGA image at power-on.

# Known Issues and Errata

The following list contains known issues and errata, if any:

- There is a minor difference in the Nios II Gen2 processor cache behavior that might affect developers who choose to leverage the non-standard cache behavior of the classic processors in their applications.

**Related Information**

**Altera Knowledge Base**
For more information about known issues and errata and how to work around them, search the Altera Knowledge Base.