Nios II Performance Benchmarks

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Performance Benchmarks Overview

This datasheet lists the performance and logic element (LE) usage for the Nios® II Classic and Nios II Gen2 soft processor, and peripherals. Nios II is configurable and designed for implementation in Altera® FPGAs. The following Nios II processors cores were used for these benchmarks:

- Nios II/f—The Nios II/f "fast" processor is designed for high performance while presenting the most configuration options which are unavailable in the other Nios II processors.
- Nios II/s—The Nios II/s "standard" processor is designed for small size while maintaining moderate performance.(1)
- Nios II/e—The Nios II/e "economy" processor is designed for the smallest possible processor size while providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

Note: Results may vary slightly depending on the version of the Quartus® II software, the version of the Nios II processor, and the target device. Also, any changes to the system logic design might change the performance and LE usage. All results are generated using Qsys-based designs;

The *f_{max} for Nios II Classic/Gen2 Processor System (MHz)* and *MIPS for Nios II Classic/Gen2 Processor System* tables list the f_{max} and millions of instructions per second (MIPS®) for a system with the following components:

- Nios II processor with JTAG debug module
- JTAG UART
- 64 KB On-chip memory
- Avalon® Memory-Mapped (Avalon-MM) pipeline bridge
- Timer

The MIPS reports were obtained using the MIPS* (*Dhrystones 2.1 benchmark). You can download the Dhrystones 2.1 benchmark software from the Nios II Embedded Processor Design Examples page on the Altera website. For more information about the Dhrystones 2.1 benchmark software, refer to the readme.txt file which is included in the Dhrystones 2.1 benchmark design example.

The Fast design example illustrates a system that has all the components listed. You can download the Fast design example from the Nios II Embedded Processor Design Examples webpage. For more information about the Fast design example, refer to the readme.txt file which is included in the Fast design example.

(1) This core is only available on the Nios II Classic soft processor.

Related Information

Nios II Embedded Processor Design Examples

Nios II Classic Performance Benchmarks

Table 1: f_{max} for Nios II Classic Processor System (MHz)

Device Family	Device used	Nios II/f[2]	Nios II/s[2]	Nios II/e[2]
Stratix® V	5SGXEA7N2F45C1	340	310	390
Stratix IV	EP4S100G5H40I1	240	230	300
Cyclone V	5CGXFC7D6F31C6	180	140	200
Cyclone IV	EP4CGX30CF19C6	160	120	170
Arria® V GZ	5AGZME7K2F40C3	280	260	350
Arria V	5AGXFB5K4F40I3	170	180	250
Arria II GX	EP2AGX260FF35I3	170	170	300

Table 2: MIPS for Nios II Classic Processor System

Device Family	Nios II/f[2][3]	Nios II/s[2][3]	Nios II/e[2][3]
Stratix V	396	192	56
Stratix IV	271	147	42
Cyclone V	203	96	32
Cyclone IV GX	170	77	26
Arria V GZ	305	160	51
Arria V	203	115	38
Arria II GX	192	109	47

Table 3: MIPS/MHz ratio for Nios II Classic Processor System on Various Device Families

Device Family	Nios II/F	Nios II/S	Nios II/E
Stratix V	1.13	0.64	0.15
Stratix IV	1.13	0.64	0.15
Cyclone V	1.13	0.64	0.15
Cyclone IV GX	1.13	0.64	0.15
Arria V GZ	1.13	0.64	0.15
Arria V	1.13	0.64	0.15
Arria II GX	1.13	0.64	0.15

(2) Results were generated using push button Analysis, Synthesis and Fitter settings in the Quartus II software.
(3) All the MIPS results are based on estimations.

The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. These results represent typical results. Your results may vary.

Table 4: LE Usage for Nios II Classic Processor Cores and Peripherals - Stratix V and Stratix IV devices

Processor Core / Peripheral	Stratix V (ALMs)	Stratix IV (ALUTs)
Nios II/f[4]	751	1104
Nios II/s[5]	485	795
Nios II/e[6]	268	463
Nios II JTAG debug module	120	170
UART	61	93
JTAG UART	59	113
RAM Controller	2681[7]	3643
Timer	69	93

Table 5: LE Usage for Nios II Classic Processor Cores and Peripherals - Cyclone V and Cyclone IV GX

Processor Core / Peripheral	Cyclone V (ALMs)	Cyclone IV GX (ALUTs)
Nios II/f[4]	806	2276
Nios II/s[5]	568	1582
Nios II/e[6]	289	714
Nios II JTAG debug module	115	348
UART	55	142
JTAG UART	59	161
RAM Controller	2404[7]	442
Timer	56	139

Table 6: LE Usage for Nios II Classic Processor Cores and Peripherals - Arria V GZ, Arria V, and Arria II GX devices

Processor Core / Peripheral	Arria V GZ (ALMs)	Arria V (ALMs)	Arria II (ALUTs)
Nios II/f[4]	758	785	1115
Nios II/s[5]	484	494	799
Nios II/e[6]	267	291	483

(4) The Nios II/f processor used has 512-byte instruction, 512-byte data caches, and hardware multiplier.
(5) The Nios II/s processor used has 512-bytes instruction, hardware multiplier and no data caches.
(6) The Nios II/e processor used has no instruction or data caches, and no hardware multiplier.
(7) The RAM controller for this device is based on DDR3 SDRAM Controller with UniPHY.

Processor Core / Peripheral	Arria V GZ (ALMs)	Arria V (ALMs)	Arria II (ALUTs)
Nios II JTAG debug module	116	117	171
UART	55	55	98
JTAG UART	59	58	113
RAM Controller	2551(7)	2411	292
Timer	57	57	89

Additional performance benchmarking information for the Nios II processor can be found at the following links:

For more information about the Nios II interrupt latency performance, refer to the *Exception Handling* chapter of the *Nios II Classic Software Developer's Handbook*.

For more information about the Nios II floating-point custom instruction performance, refer to the *Using Nios II Floating-Point Custom Instructions Tutorial*.

For more information about the Nios II networking applications performance, refer to *AN440: Accelerating Nios II Networking Applications*.

Related Information

- **AN-440: Accelerating Nios II Networking Applications**
- **Using Nios II Floating-Point Custom Instructions Tutorial**
- **Exception Handling (Classic)**

Nios II Gen2 Performance Benchmarks

Table 7: f_{max} for Nios II Gen2 Processor System (MHz)

Device Family	Device used	Nios II/f(2)	Nios II/e(2)
Stratix V	5SGXEA7N2F45C1	350	420
Stratix IV	EP4S100G5H40I1	240	270
Cyclone V	5CGXFC7D6F31C6	170	200
Cyclone IV	EP4CGX30CF19C6	150	160
Arria V GZ	5AGZME7K2F40C3	280	360
Arria V	5AGXFB5K4F40I3	200	240
Arria II GX	EP2AGX260FF35I3	220	300
Arria 10	10AX115U3F45I2LG	270	330
Max 10	10M50DFF672I6G	130	150

Table 8: MIPS for Nios II Gen2 Processor System

Device Family	Nios II/f[2][3]	Nios II/e[2][3]
Stratix V	384	62
Stratix IV	260	44
Cyclone V	181	30
Cyclone IV GX	181	26
Arria V GZ	316	56
Arria V	215	36
Arria II GX	249	47

Table 9: MIPS/MHz ratio for Nios II Gen2 Processor System on Various Device Families

Device Family	Nios II/F	Nios II/E
Stratix V	1.13	0.15
Stratix IV	1.13	0.15
Cyclone V	1.13	0.15
Cyclone IV GX	1.13	0.15
Arria V GZ	1.13	0.15
Arria V	1.13	0.15
Arria II GX	1.13	0.15

The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. These results represent typical results. Your results may vary.

Table 10: LE Usage for Nios II Gen2 Processor Cores and Peripherals - Stratix V and Stratix IV devices

Processor Core / Peripheral	Stratix V (ALMs)	Stratix IV (ALUTs)
Nios II/f[8]	723	1133
Nios II/e[9]	295	524
Nios II JTAG debug module	128	165
UART	62	96
JTAG UART	58	115
RAM Controller	2575[7]	3653
Timer	68	92

[8] The Nios II Gen2/f processor used has 512-byte instruction, 512-byte data caches and hardware multiplier.
[9] The Nios II Gen2/e processor used has no instruction or data caches, and no hardware multiplier.

Table 11: LE Usage for Nios II Gen2 Processor Cores and Peripherals - Cyclone V and Cyclone IV GX devices

Processor Core / Peripheral	Cyclone V (ALMs)	Cyclone IV GX
Nios II/f[8]	810	2291
Nios II/e[9]	311	768
Nios II JTAG debug module	125	351
UART	57	141
JTAG UART	58	162
RAM Controller	2414[7]	423
Timer	55	138

Table 12: LE Usage for Nios II Gen2 Processor Cores and Peripherals - Arria V GZ, Arria V and Arria II devices

Processor Core / Peripheral	Arria V GZ (ALMs)	Arria V (ALMs)	Arria II (ALUTs)
Nios II/f[8]	745	796	1219
Nios II/e[9]	294	314	514
Nios II JTAG debug module	122	124	170
UART	56	56	93
JTAG UART	58	58	115
RAM Controller	2542[7]	2414	322
Timer	56	55	95

Table 13: LE Usage for Nios II Gen2 Processor Cores and Peripherals - Arria 10, MAX 10

Processor Core / Peripheral	Arria 10 (ALMs)	MAX 10 (logic cells)
Nios II/f[8]	804	2275
Nios II/e[9]	287	788
Nios II JTAG debug module	111	366
UART	55	141
JTAG UART	58	162
RAM Controller	178[7]	423
Timer	57	142

Additional performance benchmarking information for the Nios II processor can be found at the following links:

For more information about the Nios II interrupt latency performance, refer to the *Exception Handling* chapter of the *Nios II Gen2 Software Developer's Handbook*.

For more information about the Nios II floating-point custom instruction performance, refer to the *Using Nios II Floating-Point Custom Instructions Tutorial*.

For more information about the Nios II networking applications performance, refer to *AN440: Accelerating Nios II Networking Applications*.

Related Information

- **AN-440: Accelerating Nios II Networking Applications**
- **Using Nios II Floating-Point Custom Instructions Tutorial**
- **Exception Handling (Gen2)**

Document Revision History

Data	Version	Changes
July 2015	2015.07.06	Updated f_{max} for Nios II Gen2 Processor System (MHz): Arria 10 and MAX 10
June 2015	2015.06.18	Updated values for the following tables: • f_{max} for Nios II Classic Processor System (MHz) • LE Usage for Nios II Classic Processor Cores and Peripherals - Stratix V and Stratix IV devices • LE Usage for Nios II Classic Processor Cores and Peripherals - Cyclone V and Cyclone IV GX • LE Usage for Nios II Classic Processor Cores and Peripherals - Arria V GZ, Arria V, and Arria II GX devices • f_{max} for Nios II Gen2 Processor System (MHz) • LE Usage for Nios II Gen2 Processor Cores and Peripherals - Stratix V and Stratix IV devices • LE Usage for Nios II Gen2 Processor Cores and Peripherals - Cyclone V and Cyclone IV GX devices • LE Usage for Nios II Gen2 Processor Cores and Peripherals - Arria V GZ, Arria V and Arria II devices • LE Usage for Nios II Gen2 Processor Cores and Peripherals - Arria 10, MAX 10

Data	Version	Changes
February 2015	2015.02.25	Updated values for the following tables: • f_{max} for Nios II Classic Processor System (MHz) • MIPS for Nios II Classic Processor System • f_{max} for Nios II Gen2 Processor System (MHz) • MIPS for Nios II Gen2 Processor System • LE Usage for Nios II Classic Processor Cores and Peripherals - Stratix V and Stratix IV devices • LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Stratix V and Stratix IV devices • LE Usage for Nios II Classic Processor Cores and Peripherals - Cyclone V and Cyclone IV GX • LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Cyclone V and Cyclone IV GX devices • LE Usage for Nios II Classic Processor Cores and Peripherals - Arria V GZ, Arria V, and Arria II GX devices • LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Arria V GZ, Arria V and Arria II devices.

Data	Version	Changes
August 2014	11.0	• Updated data and device families in Table 1: fmax for Nios II Processor System (MHz) • Updated data and device families in Table 2: MIPS for Nios II Processor System • Added Table 3: fmax for Nios II Gen 2 Processor System (MHz) • Added Table 4: MIPS for Nios II Gen 2 Processor System (MHz) • Updated data and device families for Table 5: MIPS/MHz Ratio for Nios II and Nios II Gen 2 Processor System on various Device Families • Updated data and device families for Table 6: LE Usage for Nios II Processor Cores and Peripherals - Stratix V and Stratix IV devices • Added Table 7:LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Stratix V and Stratix IV Devices • Updated data for Table 8: LE Usage for Nios II Processor Cores and Peripherals - Cyclone V and Cyclone IV GX • Added Table 9: LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Cyclone V and Cyclone IV GX devices • Updated data for Table 10: LE Usage for Nios II Processor Cores and Peripherals - Arria V GZ, Arria V, and Arria II GX devices. • Added Table 11:LE Usage for Nios II Processor Cores and Peripherals - Arria V GZ, Arria V and Arria II devices.

Data	Version	Changes
Novemeber 2013	10.0	• Removed information for devices that Altera no longer supports: Arria, Cyclone, Cyclone II, Stratix, Stratix II, and all HardCopy series. • Updated performance and LE usage for Arria II GX, Arria V, Arria V GZ, Stratix IV, and Stratix V devices with the Quartus II version 13.1 software. • Added performance and LE usage for Cyclone V devices with the Quartus II version 13.1 software.
July 2013	9.0	• Measured performance and LE usage for Stratix V and Arria V devices with the Quartus II version 13.0 software • Updated new information for Stratix V and Arria V devices. • Added new information for Arria V GZ devices. • Removed information for Cyclone V devices.
December 2012	8.0	• Measured performance and LE usage with the Quartus II version 12.1 software and the Nios II version 12.1 processor. • Added new information for Cyclone V and Arria V devices. • Updated all tables with new data.
June 2011	7.0	• Measured performance and LE usage with the Quartus II version 11.0 software and the Nios II version 11.0 processor. • Updated all tables with new data.

Data	Version	Changes
July 2010	6.0	• Measured performance and LE usage with the Quartus II version 13.0 software and the Nios II version 10.0 processor. • Rearranged the logic element usage for Nios II processor cores and peripherals for HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix from table 5 to table 6. • Added new information for Stratix V device. • Updated all tables with new data.
February 2010	5.0	• Measured performance and LE usage with the Quartus II version 9.1 software and the Nios II version 9.1 processor. • Added new information for the Cyclone III LS, Cyclone IV GX, and HardCopy IV devices. • Updated information for Arria II GX devices. • Updated Table 1, Table 2, Table 3, Table 5, and Table 6 with new data.
June 2009	4.0	• Measured performance and LE usage with the Quartus II version 9.0 SP1 software and the Nios II version 9.0 SP1 processor. • Added information for the HardCopy III, Arria II GX, and Arria GX devices. • Updated Tables 1 and 2 with new data. • Added Table 6.

Data	Version	Changes
July 2008	3.0	• Measured performance and LE usage with the Quartus II version 8.0 software and the Nios II version 8.0 processor. • Added information for the Stratix IV device. • Added links for additional information on Nios II benchmark performance. • Updated Tables 1, 2, 4 and 5 with new data. • Added Table 3.
August 2007	2.0	• Measured performance and LE usage with the Quartus II version 6.1 software and the Nios II version 6.1 processor. • Added information for the Stratix III, HardCopy II, and Cyclone III devices. • Updated Tables 1, 2, and 3 with new data.
October 2004	1.0	Initial release