Altera IP

Release Notes

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RN-IP
2015.06.30

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Contents

Altera IP Release Notes 1

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These release notes include versions 15.0, 14.1, 14.0 Arria® 10 Edition, 14.0, 13.1 Arria 10 Edition, and 13.1 of Altera® IP cores, including the Altera MegaCore IP Library IP and other IP cores.

Related Information

- **Introduction to Altera IP Cores**
- **Altera Software Installation and Licensing**

Errata

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

For full information on errata and the versions affected by errata, refer to the Knowledge Base page of the Altera website.

Related Information

Altera Knowledge Base

1G/10GbE and Backplane Ethernet 10GBASE-KR PHY Revision History

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1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP Core v14.0 Revision History

Table 2-1: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- Altera Transceiver PHY IP Core User Guide
- Errata for 1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP core in the Knowledge Base
- Introduction to Altera IP Cores

1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP Core v13.1 Revision History

Table 2-2: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- Altera Transceiver PHY IP Core User Guide
- Errata for 1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP core in the Knowledge Base
- Introduction to Altera IP Cores

10-Gbps Ethernet (10GbE) MAC Revision History

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10-Gbps Ethernet (10GbE) MAC v15.0

Table 3-1: v15.0 May 2015

Description	Impact
Added new TX and RX registers, `vlandet_dis`, in the frame decoder for the option to disable VLAN or stacked VLAN tag detection. To disable the detection of VLAN/SVLAN type frame (length type field = 0x8100), set the register to 1.	This new register is available when you upgrade the IP core to v15.0

Related Information

- Introduction to Altera IP Cores
- 10-Gbps Ethernet (10GbE) MAC MegaCore Function User Guide
- Errata for 10-Gbps Ethernet (10GbE) MAC MegaCore Function in the Knowledge Base

10-Gbps Ethernet (10GbE) MAC v14.0

Table 3-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for clause 66 of IEEE 802.3—synthesis option.	This change is optional. If you do not upgrade your IP core, it does not have this new feature.

Related Information

- Introduction to Altera IP Cores
- 10-Gbps Ethernet (10GbE) MAC MegaCore Function User Guide
- Errata for 10-Gbps Ethernet (10GbE) MAC MegaCore Function in the Knowledge Base

10-Gbps Ethernet (10GbE) MAC v13.1

Table 3-3: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • HardCopy IV GX • Stratix II GX	-
Removed 1G/10GbE MAC and 10M-10GbE MAC with IEEE 1588v2 design examples from the directory.	-
The 10GbE MAC with 10GBASE-R PHY and IEEE 1588v2 configuration supports only Arria V GT device with speed grade 3_H3.	-
Increased the width for path delay interface signals such as `tx_path_delay_10g_data` (16 bits), `tx_path_delay_1g_data` (22 bits), `rx_path_delay_10g_data` (16 bits), and `rx_path_delay_1g_data` (22 bits)	-

Related Information

- **Introduction to Altera IP Cores**
- **10-Gbps Ethernet (10GbE) MAC MegaCore Function User Guide**
- **Errata for 10-Gbps Ethernet (10GbE) MAC MegaCore Function in the Knowledge Base**

10GBASE-R PHY IP Core Revision History

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10GBASE-R PHY IP Core v14.1 Revision History

Table 4-1: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-

Related Information

- Altera Transceiver PHY IP Core User Guide
- Errata for 10GBASE-R PHY in the Knowledge Base
- Introduction to Altera IP Cores

10GBASE-R PHY IP Core v14.0 Revision History

Table 4-2: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added OpenCore Plus evaluation feature support for IEEE 1588 Precision Time Protocol.	-

Related Information

- Altera Transceiver PHY IP Core User Guide
- Errata for 10GBASE-R PHY in the Knowledge Base
- Introduction to Altera IP Cores

10GBASE-R PHY IP Core v13.1 Revision History

Table 4-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Errata for 10GBASE-R PHY in the Knowledge Base**
- **Introduction to Altera IP Cores**

40- and 100-Gbps Ethernet MAC and PHY IP Core Revision History

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40- and 100-Gbps Ethernet MAC and PHY IP Core v14.1

Table 5-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1		

Related Information

- 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base

40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0 Update 2

Table 5-2: Version 14.0 Update 2 September 2014

Description	Impact	Notes
Fixed an issue in which incoming runt Ethernet packets of size one byte to eight bytes caused the 40GbE IP core to hang instead of handling the error.	If you upgrade to version 14.0 Update 2 of the Quartus II software, you must upgrade your 40-100GbE IP core to incorporate this fix. The fix has no effect on 100GbE IP cores, which did not have the issue. However, the previous versions of the 40-100GbE IP core require upgrade with the Quartus II software.	

Related Information

- 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base

40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0

Table 5-3: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	Upgrading your IP core for this change is optional.	
Added OpenCore Plus support for 40GBASE-KR4 variations.	Upgrading your IP core for this change is optional.	

Related Information

- **Introduction to Altera IP Cores**
- **40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide**
- **Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base**

40- and 100-Gbps Ethernet MAC and PHY IP Core v13.1

Table 5-4: Version 13.1 November 2013

Description	Impact	Notes
Added 40GBASE-KR4 option with FEC and with auto-negotiation and link training mode options.		
Added Synchronous Ethernet clock support option in Stratix V devices. The option separates the TX PLL and RX CDR input reference clocks (`tx_ref_clk` and `rx_ref_clk` signals replace `ref_clk` for these variations) and exposes the RX recovered clock.		
Exposed link fault signals `remote_fault_status` and `local_fault_status` in duplex variations.		
Exposed PHY status signals `tx_lanes_stable` and `lanes_deskewed` in MAC&PHY variations.		
Updated and simplified the example design and testbench. The testbench stimulus is simpler and the user no longer needs to configure the DUT with a specific name and clock rate.		

Related Information

- **40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide**
- **Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base**

40- and 100-Gbps Ethernet MAC and PHY IP Core v13.0

Table 5-5: Version 13.0 May 2013

Description	Impact	Notes
Added preamble pass-through option.		
Added transmitter average inter-packet gap (IPG) adjustment option.		

Related Information

- 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base

40- and 100-Gbps Ethernet MAC and PHY IP Core v12.1

Table 5-6: Version 12.1 November 2012

Description	Impact	Notes
Verified with the Quartus II software v12.1.		

Related Information

- 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base

50G Interlaken IP Core Revision History

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50G Interlaken IP Core v15.0

Table 6-1: Version 15.0 May 2015

Description	Impact	Notes
Added new **TX scrambler seed** parameter.	This feature adds support for modification of the TX scrambler seed for Arria 10 variations. If your design includes multiple IP cores, you should ensure they have different TX scrambler seed values. Previously this functionality was not available for Arria 10 variations. In addition, starting in the IP core version 15.0, you must refrain from modifying the RTL parameter `SCRAM_CONST` in Stratix V and Arria V GZ variations, and use the new parameter in the Parameter Editor instead.	

Related Information

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

50G Interlaken IP Core v14.1

Table 6-2: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	IYou must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Information

- **50G Interlaken MegaCore Function User Guide**
- **Errata for 50G Interlaken IP core in the Knowledge Base**

50G Interlaken IP Core v14.0 Arria 10 Edition

Table 6-3: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition.		

Related Information

- **50G Interlaken MegaCore Function User Guide**
- **Errata for 50G Interlaken IP core in the Knowledge Base**

50G Interlaken IP Core v14.0

Table 6-4: Version 14.0 June 2014

Description	Impact	Notes
New required frequency for input clock signals `tx_usr_clk` and `rx_usr_clk` is 250 MHz, and the two clocks must be driven at the same frequency. If you provide a clock with a different frequency, it must be in the range of 200 MHz to 300 MHz, and you must modify the new hidden (RTL) parameter `TX_USR_CLK_MHZ` to the new value in the files **<*instance_name*>/ilk_core_50g.sv** for synthesis and **<*instance_name*>_sim/ilk_core_50g.sv** for simulation.		
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.		

Description	Impact	Notes
Improved resource utilization by 20% and latency by 55%.		

Related Information

- **Introduction to Altera IP Cores**
- **50G Interlaken MegaCore Function User Guide**
- **Errata for 50G Interlaken IP core in the Knowledge Base**

50G Interlaken IP Core v13.1 Arria 10 Edition

Table 6-5: Version 13.1 Arria 10 Edition December 2013

Description	Impact	Notes
Added support for Arria 10 devices. IP core variations that target an Arria 10 device have additional interfaces and design requirements.		

Table 6-6: 50G Interlaken IP Core Signal Changes

Signals added or modified in version 13.1 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_serial_clk	New interface to external TX PLL. Relevant for Arria 10 variations only.
—	tx_pll_locked	
—	tx_pll_powerdown	
—	tx_cal_busy	
—	reconfig_clk	New Arria 10 transceiver reconfiguration interface. Relevant for Arria 10 variations only.
—	reconfig_reset	
—	reconfig_read	
—	reconfig_write	
—	reconfig_address[12:0]	
—	reconfig_readdata[31:0]	
—	reconfig_waitrequest	
—	reconfig_writedata[31:0]	

Old Signal Name	New Signal Name	Notes
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V and Stratix V variations. This interface is present only in Arria V and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Information

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

50G Interlaken IP Core v13.1

Table 6-7: Version 13.1 November 2013

Description	Impact	Notes
Verified in the Quartus II software v13.1.		

Related Information

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

50G Interlaken IP Core v13.0

Table 6-8: Version 13.0 May 2013

Description	Impact	Notes
Initial release.		

Related Information

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

100G Interlaken IP Core Revision History

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100G Interlaken IP Core v15.0

Table 7-1: Version 15.0 May 2015

Description	Impact	Notes
Added new **TX scrambler seed** parameter.	This feature adds support for modification of the TX scrambler seed for Arria 10 variations. If your design includes multiple IP cores, you should ensure they have different TX scrambler seed values. Previously this functionality was not available for Arria 10 variations. In addition, starting in the IP core version 15.0, you must refrain from modifying the RTL parameter `SCRAM_CONST` in Stratix V and Arria V GZ variations, and use the new parameter in the Parameter Editor instead.	

Related Information

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

100G Interlaken IP Core v14.1

Table 7-2: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Information

- **100G Interlaken MegaCore Function User Guide**
- **Errata for 100G Interlaken IP core in the Knowledge Base**

100G Interlaken IP Core v14.0 Arria 10 Edition

Table 7-3: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition.		

Related Information

- **100G Interlaken MegaCore Function User Guide**
- **Errata for 100G Interlaken IP core in the Knowledge Base**

100G Interlaken IP Core v14.0

Table 7-4: Version 14.0 June 2014

Description	Impact	Notes
Removed `mm_clk_locked` input signal.	Port change.	
Removed hidden parameter `CNTR_BITS` from top level RTL files.		
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.		

Related Information

- **Introduction to Altera IP Cores**

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

100G Interlaken IP Core v13.1 Arria 10 Edition

Table 7-5: Version 13.1 Arria 10 Edition December 2013

Description	Impact	Notes
Added support for Arria 10 devices. IP core variations that target an Arria 10 device have additional interfaces and design requirements.		

Table 7-6: 100G Interlaken IP Core Signal Changes

Signals added or modified in version 13.1 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_serial_clk	New interface to external TX PLL. Relevant for Arria 10 variations only.
—	tx_pll_locked	
—	tx_pll_powerdown	
—	tx_cal_busy	
—	reconfig_clk	New Arria 10 transceiver reconfiguration interface. Relevant for Arria 10 variations only.
—	reconfig_reset	
—	reconfig_read	
—	reconfig_write	
—	reconfig_address[13:0] or reconfig_address[14:0]	
—	reconfig_readdata[31:0]	
—	reconfig_waitrequest	
—	reconfig_writedata[31:0]	
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V and Stratix V variations. This interface is present only in Arria V and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Information

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

100G Interlaken IP Core v13.1

Table 7-7: Version 13.1 November 2013

Description	Impact	Notes
Added optional ECC feature on M20K blocks in Stratix V devices.		
Added bit error injection testing feature to check CRC24 error detection.		
Changed implementation of single segment mode: • Changed parameter name from **Received data format** to **Data format**. • If you select Single segment mode, the IP core can no longer handle incoming dual segment traffic on the TX client data interface.		
Added four new parameters to optionally include advanced error reporting and handling, Stratix V M20K block ECC feature, diagnostic features, and in-band flow control functionality. Excluding the features improves resource utilization.		
Changed the behavior of the management interface during read operations. The IP core asserts the `mm_rddata_valid` signal two `mm_clk` cycles after the `mm_read` signal is asserted, instead of one `mm_clk` cycle as in previous versions of the IP core.		

Related Information

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

100G Interlaken IP Core v13.0

Table 7-8: Version 13.0 May 2013

Description	Impact	Notes
Added dual segment mode.		
Added packet mode option in parameter editor.		
Improved error handling.		
Added PRBS capability.		
Added CRC-32 error injection capability.		

Related Information

- 100G Interlaken MegaCore Function User Guide

- **Errata for 100G Interlaken IP core in the Knowledge Base**

Arria V GZ Hard IP for PCI Express IP Core Revision History

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Arria V GZ Hard IP for PCI Express IP Core v15.0

Table 8-1: v15.0 May 2015

Description	Impact
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

Related Information

- Introduction to Altera IP Cores
- Arria V GZ Avalon-ST Interface for PCIe Solutions User Guide
- Arria V GZ Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Arria V GZ Hard IP for PCI Express in the Knowledge Base

Arria V GZ Hard IP for PCI Express IP Core v14.1

Table 8-2: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- Introduction to Altera IP Cores
- Arria V GZ Avalon-ST Interface for PCIe Solutions User Guide
- Arria V GZ Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Arria V GZ Hard IP for PCI Express in the Knowledge Base

Arria V GZ Hard IP for PCI Express IP Core v14.0

Table 8-3: v14.0 June 2014

Description	Impact
Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core): • Revised programming model and optimized the performance of the Descriptor Controller. • Added support for either 128- or 256-bit interface to the Application Layer. • Added support for 64-bit addressing, making address translation unnecessary. • Added support for optional bursting RX Master for BAR2. • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. • Due to the many changes, the support level has reverted to preliminary.	The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to the 14.0 version. Altera will no longer support the 13.1 version

Description	Impact
Made the following changes to the Avalon-MM Arria V GZ Hard IP for PCI Express IP core : • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. • Added support for 64-bit addressing, making address translation unnecessary. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM. • Increased CRA address to 14 bits from 12 bits.	All of these new features are optional. If you choose to include an optional feature that changes the port signature of your IP core, you must regenerate your design and connect the signals.
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*	

Related Information

- **Introduction to Altera IP Cores**
- **Arria V GZ Avalon-ST Interface for PCIe Solutions User Guide**
- **Arria V GZ Avalon-MM Interface for PCIe Solutions User Guide**
- **V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide**
- **Errata for Arria V GZ Hard IP for PCI Express in the Knowledge Base**

Arria V GZ Hard IP for PCI Express IP Core v13.1

Table 8-4: v13.1 November 2013

Description	Impact
Support for Avalon-MM 256-Bit Hard IP for PCI Express Gen3 ×8 with DMA is final.	-
Support for Gen2 CvP is removed.	

Related Information

- **Introduction to Altera IP Cores**
- **Arria V GZ Avalon-ST Interface for PCIe Solutions User Guide**
- **Arria V GZ Avalon-MM Interface for PCIe Solutions User Guide**

- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Arria V GZ Hard IP for PCI Express in the Knowledge Base

Arria V Hard IP for PCI Express IP Core Revision History

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Arria V Hard IP for PCI Express IP Core v15.0

Table 9-1: v15.0 May 2015

Description	Impact
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

Related Information

- Introduction to Altera IP Cores
- Arria V Avalon-ST Interface for PCIe Solutions User Guide
- Arria V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Arria V Hard IP for PCI Express in the Knowledge Base

Arria V Hard IP for PCI Express IP Core v14.1

Table 9-2: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- **Introduction to Altera IP Cores**
- **Arria V Avalon-ST Interface for PCIe Solutions User Guide**
- **Arria V Avalon-MM Interface for PCIe Solutions User Guide**
- **V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide**
- **Errata for Arria V Hard IP for PCI Express in the Knowledge Base**

Arria V Hard IP for PCI Express IP Core v14.0

Table 9-3: v14.0 June 2014

Description	Impact
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Upgraded Arria V Hard IP for PCI Express IP core to support the new IP Catalog.	-
Added support for new, V-Series PCIe with Avalon-MM DMA Interface IP Core.	-
Arria V Avalon-MM Hard IP for PCI Express IP core. : • Added access to selected Configuration Space and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals.	All of these new features are optional. If you include either the hard IP status bus or status extension bus in you design, you must regenerate your design and connect the new bus

Related Information

- **Introduction to Altera IP Cores**
- **Arria V Avalon-ST Interface for PCIe Solutions User Guide**
- **Arria V Avalon-MM Interface for PCIe Solutions User Guide**

- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Arria V Hard IP for PCI Express in the Knowledge Base

Arria V Hard IP for PCI Express IP Core v13.1

Table 9-4: v13.1 November 2013

Description	Impact
Added support for Gen2 Configuration via Protocol (CvP) using an **.ini** file. Contact your sales representative for more information.	-

Related Information

- Introduction to Altera IP Cores
- Arria V Avalon-ST Interface for PCIe Solutions User Guide
- Arria V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Arria V Hard IP for PCI Express in the Knowledge Base

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Revision History 10

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Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v15.0.1 Revision History

Table 10-1: v15.0.1 June 2015

Description	Impact
Verified in Quartus II software v15.0.1	-
Made the following improvements to the link training (LT) algorithm: • Support for manual VGA tuning • Added option to skip link partner VOD (main tap) adjustment during LT • Added option to enable decision feedback equalization (DFE) at the end of LT • General algorithm improvements for stability	-

Table 10-2: 10GBASE-KR IP Core Register Definition Changes v15.0.1

Register definitions added or modified in version 15.0.1 for word address 0x4D0.

Bit	RW	Old Register Name	New Register Name	Description
2	RW	`quick_mode`	Reserved	Reserved
3	RW	`pass_one`	Reserved	Reserved

Bit	RW	Old Register Name	New Register Name	Description
18	RW	Ctle_depth	VOD Training Enable	Defines whether or not to skip adjustment of the link partner's VOD (main tap) during link training. The following values are defined: • 1 = Exercise VOD (main tap) adjustment during link training • 0 = Skip VOD (main tap) adjustment during link training The default value is 0.
19	RW	Ctle_depth	Bypass DFE	Defines whether or not Decision Feedback Equalization (DFE) is enabled at the end of link training. The following values are defined: • 1 = Bypass continuous adaptive DFE at the end of link training • 0 = Enable continuous adaptive DFE at the end of link training The default value for simulation is 1. The default value for hardware is 0.
21:20	RW	rx_ctle_mode	rx_ctle_vga_mode	Defines the point at which to enable the RX CTLE in the adaptation algorithm. The following values are defined: • 00 = never, the RX CTLE isn't enabled or adjusted • 01 = trigger CTLE/VGA before starting TX-EQ • 10 = trigger CTLE/VGA after finishing TX-EQ • 11 = trigger CTLE/VGA, both before starting, and after finishing TX-EQ The default value is 00. **Note:** These bits are only effective when 0x4D0[22] is set to 0.

Bit	RW	Old Register Name	New Register Name	Description
22	RW	Reserved	adp_ctle_vga_mode	Defines whether or not CTLE/VGA adaptation is in adaptive or manual mode. The following values are defined: • 1 = Manual CTLE/VGA mode. Link training algorithm sets fixed CTLE and VGA values as specified in bits 0x4D0[28:24] and 0x4D0[31:29], respectively. • 0 = adaptive CTLE mode. Bits in 0x4D0[21:20] are effective only when this bit is set to 0. The default value is 1.
28:24	RW	Reserved	Manual CTLE	Defines the CTLE value used by the link training algorithm when in manual CTLE mode. These bits are only effective when 0x4D0[22] is set to 1. The default value is 1.
31:29	RW	max_post_step[2:0]	Manual VGA	Defines the VGA value used by the link training algorithm when in manual VGA mode. These bits are only effective when 0x4D0[22] is set to 1. The default value is 4.

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Errata for 10GBASE-R PHY in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v15.0 Revision History

Table 10-3: v15.0 May 2015

Description	Impact
When adaptation is enabled, the 10GBASE-KR link training may not finish in the required 500 ms. This results in a Link Training Failure. When this occurs, equalization may not be trained optimally for the link.	You can disable adaptation and use a fixed CTLE value during link training. This is done by setting 0x4D0[22:20] to 4, and

Description	Impact
	0x4D0[28:24] to the desired CTLE value.
The 10GBASE-KR register, 0x4d2[0] Link Trained – Receiver status, is read incorrectly as 0 when testing on HW. It will be read back correctly during simulation.	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v14.1 Revision History

Table 10-4: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v14.0 Revision History

Table 10-5: v14.0 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Description	Impact
Removed the following parameters from the **Link Training** tab: • **Enable daisy chain mode**. • **Enable microprocessor interface**.	-
Changed the default values of the following PMA parameters under the **Link Training** tab: • **VMAXRULE** • **VMINRULE** • **VODMINRULE** • **VPOSTRULE** • **VPRERULE** • **PREMAINVAL** • **INITMAINVAL** • **INITPOSTVAL** • **INITPREVAL**	-
Changed Avalon Memory-Mapped (AVMM) clock frequency from 125 MHz to 161 MHz to support NIOS II. The AVMM slave interface provides access to the IP core registers.	-
IEEE 1588 Precision Time Protocols are not supported in backplane applications.	-
Link Training takes more time in simulation as NIOS command processing is slower.	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v13.1 Revision History

Table 10-6: v13.1 December 2013

Description	Impact
Initial release	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 External Memory Interface IP Revision History 11

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Arria 10 External Memory Interface IP 15.0

Table 11-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0	-

Related Information

- External Memory Interface Handbook
- Errata for Arria 10 External Memory Interface IP in the Knowledge Base

Arria 10 External Memory Interface IP 14.1

Table 11-2: v14.1 December 2014

Description	Impact
Several new features are added in v14.1: • Support for the QDR-IV memory protocol. • Ping Pong PHY support for DDR3 and DDR4. • Compact pin placement for x4 groups for DDR3 and DDR4. • Simulation, compilation, and timing closure support for DDR4 RDIMMs. • Compilation and timing closure support for DDR3 RDIMMs, and LRDIMMs, and DDR4 LRDIMMs. • Half-rate controller and PHY support for quarter-rate DDR3 and DDR4 interfaces.	-

Description	Impact
DDR3 and DDR4 interfaces with x4 groups are now generated with two DQS groups per I/O lane. In previous releases, interfaces with x4 groups required one I/O lane per DQS group, causing inefficient I/O pin usage. (For devices with a name prefixed with 10AX090, 10AX115, 10AT090, or 10AT115, x4 support is available only for ES2 and newer silicon revisions. For other devices, x4 support is available for all silicon revisions including ES.)	v14.1 allows more compact pin placement.
For quarter-rate DDR3 and DDR4 interfaces using hard memory controller, the hard memory controller and the PHY can now run at half-rate (that is, at 2x the frequency of user clock domain). This feature is enabled automatically for interfaces and FPGA devices that can support it. In previous releases, the hard memory controller and the PHY always ran at quarter-rate for quarter-rate interfaces.	Running at half-rate allows better efficiency and improved latency.
In PHY-only mode for multi-rank interfaces, new signals `afi_rrank` and `afi_wrank` have been introduced for shadow register selection.	Shadow registers now are supported for Arria 10.
DDR4 3DS / ChipID is not supported by Arria 10. The option to use it has been removed.	Option is no longer available.

Related Information

External Memory Interface Handbook

Arria 10 External Memory Interface IP 14.0 Arria 10 Edition

Table 11-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for QDR II/II+/II+ Xtreme and RLDRAM 3.	-
Added I/O and Diagnostics Settings tab to the parameter editor for DDR3 and DDR4.	-
Added optional signal `mem_alert_n` , which is enabled by default for DDR4. This port is used to enable address and command deskew for calibration.	-
Added support for PHY-only mode for DDR3 and DDR4.	-
Added error correction code (ECC) and memory-mapped configuration and status register (MMR) support for DDR3 and DDR4.	-

Related Information

External Memory Interface Handbook

Arria 10 External Memory Interface IP 13.0 Arria 10 Edition

Table 11-4: v13.0 Arria 10 Edition December 2013

Description	Impact
Initial release.	-

Related Information

External Memory Interface Handbook

Arria 10 FPLL IP Core Revision History 12

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Arria 10 FPLL IP Core Revision History v15.0 Revision History

Table 12-1: v15.0 May 2015

Description	Impact
Changed the following GUI warning: Warning (10858): Verilog HDL warning at altera_xcvr_fpll_a10.sv(487): object pll_extfb_wire used but never assigned. This compile warning resulted from a dangling net left behind when the CGB master was not generated (enabled). Tied off the `pll_extfb_wire` signal when the CGB master is not generated to drive it.	-
Added an **Advanced Parameters** tab that displays the following values: • C counters (0 to 3) • L, M and N counters • K fractional division • VCO frequency	-
Truncated the return vco frequency (MHz) to six digits after the decimal point.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 FPLL IP Core Revision History v14.1 Revision History

Table 12-2: v14.1 December 2014

Description	Impact
Changed the default FPLL Mode to Transceiver TX PLL.	-
FPLL does not allow the bandwidth setting of "high" in fractional mode.	
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for Transceiver IP Cores in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 FPLL IP Core Revision History v14.0 Revision History

Table 12-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Changed the FPLL Parameter Editor graphic user interface (GUI) to show the available FPLL modes. You can use the FPLL in the following three modes: • Core • Cascade Source • Transceiver	-

Description	Impact
Removed the option for automatic bandwidth setting. The following bandwidth settings are available: • Low • Medium • High	-
Enhanced user warnings and information messages.	-
The fPLL IP in 13.1 Arria 10 edition, allowed simultaneous selection of FPLL to be used in core and transceiver PLL modes. However, in the FPLL IP in 14.0 Arria 10 edition, only one mode (transceiver PLL or core PLL) can be selected at a time. If you have selected both (transceiver PLL and core PLL) modes in 13.1 Arria 10 edition, then FPLL IP will fail automatic upgrade for 14.0 Arria 10 edition. In this case, you will have to manually upgrade the FPLL IP after selecting one legal FPLL usage mode.	-
The **Master Clock Generation Block** tab in IP Parameter Editor is not visible when "Core" is selected as the FPLL mode. The **Master Clock Generation Block** tab appears only when "Transceiver" is selected as the FPLL mode.	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for Transceiver IP Cores in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 FPLL IP Core Revision History v13.1 Revision History

Table 12-4: v13.1 Arria 10 Edition

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for Transceiver IP Cores in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 Hard IP for PCI Express IP Core Revision History 13

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Arria 10 Hard IP for PCI Express IP Core v15.0

Table 13-1: 15.0 May 2015

Description	Impact
Added **Enable Altera Debug Master Endpoint (ADME)** parameter to support optional Native PHY register programming with the Altera System Console.	If you turn on this option, you can use the Altera System Console for enhanced debugging.
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.
In IP core variations with the Avalon-MM interface, added support for dynamically generated Qsys example designs that reflect the parameters that you selected in the Parameter Editor. This feature was new in the IP core v14.1 with the Avalon-ST interface, and is now provided also with the Avalon-MM interface.	If you choose the Avalon-MM interface and click the Example Design button, the Quartus II software generates an example design that matches the current parameter settings, for most IP core variations,

Description	Impact
In IP core variations with the Avalon-MM or Avalon-MM DMA interface, added **Enable Hard IP Status Bus when using the AVMM interface** parameter. This parameter makes visible or hides the link status signals, ECC error signals, TX and RX parity error signals, completion header and data signals, and currentspeed signal.	Refer to the Arria 10 HIP for PCI Express Signal Changes v15.0 table.
The IP core no longer generates with a Synopsys Design Constraints file (**.sdc**) that includes a derive_pll_clocks constraint. Instead, in compliance with Arria 10 design requirements, the user must add the timing constraint macro `derive_pll_clocks -create_base_clocks` to a top-level **.sdc** file.	User must add this constraint in a top-level Synopsys Design Constraints file. This constraint was previously included in the IP core SDC file.

Table 13-2: Arria 10 HIP for PCI Express Signal Changes v15.0

Signals added or modified in version 15.0.

Signal Name	New Behavior
`derr_cor_ext_rcv`	The presence or absence of these signals is now controlled by the new **Enable Hard IP Status Bus when using the AVMM interface** parameter. If the parameter is turned on, the signals are included. If the parameter is turned off, the signals are not available.
`derr_cor_ext_rpl`	
`derr_rpl`	
`dlup`	
`dlup_exit`	
`ev128ns`	
`ev1us`	
`hotrst_exit`	
`int_status[3:0]`	
`l2_exit`	
`lane_act[3:0]`	
`ltssmstate[4:0]`	
`rx_par_err`	
`tx_par_err[1:0]`	
`cfg_par_err`	
`ko_cpl_spc_header[7:0]`	
`ko_cpl_spc_data[11:0]`	
`currentspeed[1:0]`	

Related Information

- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface**

- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface**
- **Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base**

Arria 10 Hard IP for PCI Express IP Core v14.1

Table 13-3: 14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.
Added support for Single-Root I/O Virtualization (SR-IOV) interface.	If you choose to use the SR-IOV interface, you will need to redesign your Application Layer.
Added support for dynamically generated Qsys example designs that reflects the parameters that you selected in the Parameter Editor.	If you choose the Avalon-ST interface, the automatically generated testbench has the parameters that you specified.
Added support for Configuration Space Bypass Mode when using the Avalon-ST interface.	If you choose to use Configuration Space Bypass Mode, you will need to redesign your Application Layer.
Added Quartus II compilation support for the Avalon-MM with DMA interface.	You can now compile for the Avalon-MM with DMA interface and download the Programmer Object File **.pof** to a development board.
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	If you generate your IP core outside a Quartus II project, you must ensure that you specify a device for your Arria 10 IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface**
- **Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base**

Arria 10 Hard IP for PCI Express IP Core v14.0 Arria 10 Edition

Table 13-4: v14.0 Arria 10 Edition August 2014

Description	Impact
Changed the PIPE interface to 32 bits for all data rates.	This change requires you to recompile your v13.1 variant in 14.0a10 release
Added simulation log file, **altpcie_monitor_<*dev*>_dlhip_tlp_file_log.log** in your simulation directory. Generation of the log file requires the following simulation file, **<*install_dir*>altera/altera_pcie/altera_pcie_a10_hip/altpcie_monitor_a10_dlhip_sim.sv**, that was not present in earlier releases of the Quartus II software.	
Added option to enable 62.5 MHz application clock for Gen1 x1 data rate.	If you choose this option, you must regenerate your IP core.
Added third interface option, Avalon-MM with DMA, that includes a high performance DMA. If you choose this option, you must regenerate your IP core.	
Added option to integrate the Descriptor Controller in the variant for the Avalon-MM with DMA interface.	-

Related Information

- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface**
- **Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base**

Arria 10 Hard IP for PCI Express IP Core v13.1 Arria 10 Edition

Table 13-5: v13.1 Arria 10 Edition December 2013

Description	Impact
Initial release.	-

Related Information

- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface**
- **Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface**
- **Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base**

Arria 10 Transceiver ATX PLL IP Core Revision History 14

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Arria 10 Transceiver ATX PLL IP Core v15.0 Revision History

Table 14-1: v15.0 May 2015

Description	Impact
Added an **Advanced Parameters** tab that displays the following values: • C counters (0 to 3) • L, M and N counters • K fractional division • VCO frequency	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver ATX PLL IP Core v14.1 Revision History

Table 14-2: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1.	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver ATX PLL IP Core v14.0 Revision History

Table 14-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for fractional mode. Fractional mode provides support for a wider range of output frequencies than integer mode. This feature is available under the **Output Frequency** tab.	-
Added support for Embedded Debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Added the following presets for GT and GX modes: • **GT 25781.25 Mbps Single Channel** • **GX 2500 Mbps Bonded** • **GX 2500 Mbps Single Channel** • **GX 2500 Mbps xN Non-Bonded**	-
Changed the documentation link in IP Parameter Editor to refer to the *Arria 10 Transceiver PHY User Guide*.	-
Enhanced user warnings and information messages.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver ATX PLL IP Core v13.1 Revision History

Table 14-4: v13.1 Arria 10 Edition December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver CMU PLL IP Core Revision History 15

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Arria 10 Transceiver CMU PLL IP Core v15.0 Revision History

Table 15-1: v15.0 May 2015

Description	Impact
Removed the `hip_cal_done` port to avoid a fitter failure. Previously, this port was available when dynamic reconfiguration was enabled.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver CMU PLL IP Core v14.1 Revision History

Table 15-2: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- Arria 10 Transceiver PHY User Guide

- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver CMU PLL IP Core v14.0 Revision History

Table 15-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Added preset **GX 2500 Mbps Single Channel** for GX mode.	-
Changed the IP core to expose the `pll_cal_busy` port to the top level.	-
Changed the documentation link in IP Parameter Editor to refer to the *Arria 10 Transceiver PHY User Guide*.	-
Enhanced user warnings and information messages.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver CMU PLL IP Core v13.1 Revision History

Table 15-4: v13.1 Arria 10 Edition December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Arria 10 Transceiver Native PHY IP Core Revision History 16

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Arria 10 Transceiver Native PHY IP Core v15.0 Revision History

Table 16-1: 15.0 May 2015

Description	Impact
Changed bit settings.	You must upgrade any IPs generated prior to Quartus II software v15.0.
Added the following warning message to the GUI: "**Enable dynamic reconfiguration** should be enabled when **Enable datapath and interface reconfiguration** is enabled". This message appears when dynamic reconfiguration is disabled while datapath reconfiguration is enabled.	-

Description	Impact
Updated tooltips and added information messages for the parameters in the table below **Note:** Information messages are displayed only if the parameter is enabled.	-

Table 16-2: Tool Tip and Information Message Updates

Parameter	Tool Tip Update	Information Message
tx_pma_clkout	Enables the optional tx_pma_clkout output clock. This is the parallel clock from the TX PMA. This port is not to be used to clock the data interface.	The tx_pma_clkout port is not to be used to clock the data interface.
rx_pma_clkout	Enables the optional rx_pma_clkout output clock. This is the recovered parallel clock from the RX CDR. This port is not to be used to clock the data interface.	The rx_pma_clkout port is not to be used to clock the data interface.
tx_pma_div_clkout	Enables the optional tx_pma_div_clkout output clock. This port should not be used for register mode data transfers.	The tx_pma_div_clkout port should not be used for register mode data transfers.
rx_pma_div_clkout	Enables the optional rx_pma_div_clkout output clock. This port should not be used for register mode data transfers.	The rx_pma_div_clkout port should not be used for register mode data transfers.

Description	Impact
Added the following information message to the GUI for `tx_std_bitslipboundarysel`: "The `tx_std_bitslipboundarysel` port must be enabled if Standard PCS TX bitslip capability is desired." This message is displayed if TX bitslip is enabled and Std PCS is used.	-
Added warning messages for merging simplex IPs. The messages are displayed conditionally. For example, when embedded debug is enabled in a simplex design. The following are example messages: • If this TX Simplex Native PHY instance needs to be merged with an RX Simplex Native PHY instance or a CDR PLL IP instance, ensure that reconfiguration inputs of both the PHY instances are driven by the same source. • If this RX Simplex Native PHY instance needs to be merged with an TX Simplex Native PHY instance, ensure that reconfiguration inputs of both the PHY instances are driven by the same source. • This TX Simplex Native PHY instance cannot be merged with an RX Simplex Native PHY instance or a CDR PLL IP instance. • This RX Simplex Native PHY instance cannot be merged with a TX Simplex Native PHY instance.	-
Removed the **triggered** option from the **DFE adaptation mode** parameter. If an IP core is generated before 15.0 with the **triggered** option selected for **DFE adaptation mode**, automatic upgrade maps **triggered** to **continuous**. Also updated the tool tip for **DFE adaptation mode** accordingly.	-
Added options to enable/disable the `tx_pma_iqtxrx_clkout` and `rx_pma_iqtxrx_clkout` ports. The ports are targeted for cascading the RX/TX PMA output clocks to the input of a PLL.	-
Fixed the issue where the following parameter values were not setting properly if using Riveria: • `hssi_10g_tx_pcs_pseudo_seed_a` • `hssi_10g_tx_pcs_pseudo_seed_b` • `hssi_8g_rx_pcs_wa_pd_data` • `pma_tx_buf_xtx_path_pma_tx_divclk_hz` • `pma_rx_buf_xrx_path_pma_rx_divclk_hz` • `pma_tx_buf_xtx_path_tx_pll_clk_hz`	-

Description	Impact
When generating configuration files for RX-only configurations, the PHY incorrectly includes registers related to the TX CGB block. When generating configuration files for TX-only configurations, the PHY incorrectly includes registers related to the RX PMA adaptation blocks.	The RX/TX configuration file inadvertently contains configuration data for the complimentary simplex direction. This causes an issue when a TX and RX PHY are merged to the same location because streaming the configuration data to one side affects the other. Embedded streamer configurations are not affected as such and are not permitted in simplex configurations.

Arria 10 Transceiver Native PHY IP Core v14.1 Revision History

Table 16-3: 14.1 December 2014

Description	Impact
Added support for multiple silicon revisions supported for ACDS 14.1 version of the Quartus II software.	-
Added a new parameter for Interlaken protocol implementation called **Enable Interlaken TX random disparity bit**. When enabled, a random number is used as a disparity bit.	
Changed the option "Manual (PLD controlled)" to "Manual (FPGA fabric controlled)" for the **RX word aligner mode** parameter.	-
Changed the option "SATA" to "SATA/SAS" for **PMA configuration rules** parameter.	-
Changed the descriptions of parameters **CTLE adaptation mode** and **DFE adaptation mode**.	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Arria 10 Transceiver Native PHY IP Core v14.0 Revision History

Table 16-4: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for PCS-Direct mode. The PCS-Direct mode enables you to bypass all the internal PCS blocks.	-
Changed the maximum data rate supported by GT channels to 28300 Mbps.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Changed **Enable embedded JTAG AVMM Master** parameter to **Enable Altera Debug Master Endpoint** parameter.	-
Added the following parameters: • **PMA Configuration Rules**. • **Enable fast sync status reporting for deterministic latency SM** under the **Word Aligner and Bitslip** tab. Use this parameter for implementing CPRI (Auto) protocol.	-
Added Faster Register mode for PCS TX and RX FIFO.	-
Changed the parameter **Enable Reconfiguration between Standard and Enhanced PCS** to **Enable Datapath and Interface Reconfiguration**.	-
Changed the **one-time** option for CTLE and DFE adaptation mode to **Triggered** mode.	-
Removed **Enable tx_enh_fifo_cnt port** and **Enable rx_enh_fifo_cnt port** parameters from the IP **Parameter Editor**.	-
Removed the parameter **Device Speed Grade**selection.	-
Removed 62.5, 125, 200, and 250 values for PPM detector threshold.	-
Enhanced user warnings and information messages.	-

Description	Impact
Added the following presets: • 3G SDI NTSC • 3G SDI PAL • HD SDI NTSC • HD SDI PAL • Low Latency GT • SAS Gen1 • SAS Gen1.1 • SAS Gen2 • SATA Gen1 • SATA Gen2 • SATA Gen3 • SFI-S 64:64 4x11.3Gbps • SONET/SDH OC-12 • SONET/SDH OC-48 • SONET/SDH OC-96 • Serial Rapid IO 1.25Gbps	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for Transceiver IP Cores in the Knowledge Base**
- **Introduction to Altera IP Cores**

Arria 10 Transceiver Native PHY IP Core v13.1 Revision History

Table 16-5: v13.1 Arria 10 Edition

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for Transceiver IP Cores in the Knowledge Base**
- **Introduction to Altera IP Cores**

CIC IP Core Revision History 17

2015.06.30

RN-IP Subscribe Send Feedback

CIC IP Core v15.0

Table 17-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- CIC MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for CIC IP core in the Knowledge Base

CIC IP Core v14.1

Table 17-2: v14.1 December 2014

Description	Impact
Added final support for Arria 10 devices	-

Related Information

- CIC MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for CIC IP core in the Knowledge Base

CIC IP Core v14.0 Arria 10 Edition

Table 17-3: 14.0 Arria 10 Edition August 2014

Description	Impact
Added two new buses, `av_st_in_data` and `av_st_out_data`, which includes all Avalon-ST compilant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- **CIC MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for CIC IP core in the Knowledge Base**

CIC IP Core v14.0

Table 17-4: 14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices.	-
Added support for IP Catalog. For more information about IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **CIC MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for CIC IP core in the Knowledge Base**

CIC IP Core v13.1

Table 17-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-

Related Information

- CIC MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for CIC IP core in the Knowledge Base

CPRI IP Core Revision History 18

2015.06.30

RN-IP Subscribe Send Feedback

CPRI IP Core v14.1

Table 18-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1.		

Related Information

- CPRI MegaCore Function User Guide
- Errata for CPRI IP core in the Knowledge Base

CPRI IP Core v14.0

Table 18-2: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.		
Renamed **Include Vendor Specific Space (VSS) access through CPU interface** parameter to **Include all control word access through CPU interface** to better explain the function of the parameter. The parameter functionality remains as it was in the 13.1 and 13.0 releases.		

Related Information

- Introduction to Altera IP Cores
- CPRI MegaCore Function User Guide
- Errata for CPRI IP core in the Knowledge Base

CPRI IP Core v13.1

Table 18-3: Version 13.1 November 2013

Description	Impact	Notes
Removed support for HardCopy IV GX device family.		
Improved the demonstration testbench.		
Improved resource utilization.		

Related Information

- CPRI MegaCore Function User Guide
- Errata for CPRI IP core in the Knowledge Base

CPRI IP Core v13.0

Table 18-4: Version 13.0 May 2013

Description	Impact	Notes
Added new parameter for user control of inclusion or exclusion of software interface to full control words.		
Added new parameter for user control of inclusion or exclusion of round-trip delay calibration feature.		
Reduced resource utilization in 28-nm devices.		

Related Information

- CPRI MegaCore Function User Guide
- Errata for CPRI IP core in the Knowledge Base

Cyclone V Hard IP for PCI Express IP Core Revision History 19

2015.06.30

RN-IP Subscribe Send Feedback

Cyclone V Hard IP for PCI Express IP Core v15.0

Table 19-1: v15.0 May 2015

Description	Impact
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

Related Information

- Introduction to Altera IP Cores
- Cyclone V Avalon-ST Interface for PCIe Solutions User Guide
- Cyclone V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base

Cyclone V Hard IP for PCI Express IP Core v14.1

Table 19-2: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- Introduction to Altera IP Cores
- Cyclone V Avalon-ST Interface for PCIe Solutions User Guide
- Cyclone V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base

Cyclone V Hard IP for PCI Express IP Core v14.0

Table 19-3: v14.0 June 2014

Description	Impact
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for new V-Series PCIe with Avalon-MM DMA Interface IP Core.	-
Added the following features to the Cyclone V Avalon-MM Hard IP for PCI Express IP core: • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals.	All of these new features are optional. If you include either the hard IP status bus or status extension bus in you design, you must regenerate your design and connect the new bus.

Related Information

- Introduction to Altera IP Cores
- Cyclone V Avalon-ST Interface for PCIe Solutions User Guide
- Cyclone V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base

Cyclone V Hard IP for PCI Express IP Core v13.0 SP1

Table 19-4: v13.0 SP1 July 2013

Description	Impact
Verified in the Quartus II software v13.0 SP1.	-

Related Information

- Introduction to Altera IP Cores
- Cyclone V Avalon-ST Interface for PCIe Solutions User Guide
- Cyclone V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base

DDR2 and DDR3 SDRAM Controller with UniPHY Revision History 20

2015.06.30

RN-IP Subscribe Send Feedback

DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v15.0

Table 20-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0	-

Related Information

- External Memory Interface Handbook
- Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base

DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v14.1

Table 20-2: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-

Related Information

- External Memory Interface Handbook
- Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base

DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v14.0

Table 20-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Removed support for Cyclone III, Cyclone III LS, and Stratix III devices	-

Related Information

- **External Memory Interface Handbook**
- **Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base**

DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v13.1

Table 20-4: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-
Removed support for HardCopy III and HardCopy IV devices	-

Related Information

- **External Memory Interface Handbook**
- **Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base**

DisplayPort IP Core Revision History 21

2015.06.30

RN-IP Subscribe Send Feedback

DisplayPort IP Core v15.0

Table 21-1: v15.0 May 2015

Description	Impact
Added preliminary support for Arria 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated color support. • RGB—18, 24, 30, 36, or 48 bpp • YCbCr 4:4:4—24, 30, 36, or 48 bpp • YCbCr 4:2:2—16, 20, 24, or 32 bpp	
Added source-supported DPCD locations.	
Added new bits for `DPTX_TEST_80BIT_PATTERN` bits.	
Removed the Link Quality Generation register bits and combined these bits into the `DPTX_TX_CONTROL` register. • 0000 = Normal video • 0001 = Training pattern 1 • 0010 = Training pattern 2 • 0011 = Training pattern 3 • 0111 = Video idle pattern • 1001 = D10.2 test pattern (same as training pattern 1) • 1010 = Symbol error rate measurement pattern • 1011 = PRBS7 • 1100 = 80-bit custom pattern • 1101 = HBR2 compliance test pattern (CP2520 pattern 1)	
Added new sink-supported DPCD location bits: `TEST_REQUEST`, `TEST_LINK_RATE`, `TEST_LANE_COUNT`, `PHY_TEST_PATTERN`, and `TEST_80BIT_CUSTOM_PATTERN`.	
Added simulation testbench for Arria 10 devices.	

Related Information

- Introduction to Altera IP Cores
- DisplayPort IP Core User Guide
- Errata for DisplayPort IP Core in the Knowledge Base

DisplayPort IP Core v14.1

Table 21-2: v14.1 December 2014

Description	Impact
Added multi-stream support (MST, 1 to 4 source and sink streams). You can access this feature using these parameters: • **Support MST** • **Max stream count**	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for 4Kp60 resolution.	
Removed support for double reference clocks—162MHz and 270MHz —for transceiver clocking.	
Updated the design example with pixel clock recovery feature and 4Kp60 support.	
Added new signals.	
Added new source registers: • 0×00a0 (DPTX_MST_CONTROL1) • 0×00a2 (DPTX _MST_VCPTAB0) • 0×00a3 (DPTX _MST_VCPTAB • 0×00a3 (DPTX _MST_VCPTAB1) • 0×00a4 (DPTX _MST_VCPTAB2) • 0×00a5 (DPTX _MST_VCPTAB3) • 0×00a6 (DPTX _MST_VCPTAB4) • 0×00a7 (DPTX _MST_VCPTAB5) • 0×00a8 (DPTX _MST_VCPTAB6) • 0×00a9 (DPTX _MST_VCPTAB7) • 0×00aa (DPTX _MST_TAVG_TS)	
Added new sink registers: • 0×0006 (DPRX_BER_CNTI0) • 0×0007 (DPRX_BER_CNTI1) • 0×00a0 (DPRX_MST_CONTROL1) • 0×00a1 (DPRX_MST_STATUS1) • 0×00a2 (DPRX _MST_VCPTAB0) • 0×00a3 (DPRX _MST_VCPTAB1) • 0×00a4 (DPRX _MST_VCPTAB2) • 0×00a5 (DPRX _MST_VCPTAB3) • 0×00a6 (DPRX _MST_VCPTAB4) • 0×00a7 (DPRX _MST_VCPTAB5) • 0×00a8 (DPRX _MST_VCPTAB6) • 0×00a9 (DPRX _MST_VCPTAB7)	

Table 21-3: DisplayPort IP Core Signal Changes

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	clk_cal	Calibration clock for transceiver management interface
—	tx_link_rate_8bits	Main link rate expressed in multiples of 270Mbps
—	rx_link_rate_8bits	
—	txN_video_in (N=1,2,3)	TX signals for Stream 1, 2 and 3
—	txN_vid_clk (N=1,2,3)	
—	txN_audio (N=1,2,3)	
—	txN_audio_clk (N=1,2,3)	
—	txN_ss (N=1,2,3)	
—	txN_msa_conduit (N=1,2,3)	
—	rxN_video_out (N=1,2,3)	RX signals for Stream 1, 2 and 3
—	rxN_vid_clk (N=1,2,3)	
—	rxN_audio (N=1,2,3)	
—	rxN_ss (N=1,2,3)	
—	rxN_msa_conduit (N=1,2,3)	
—	rxN_stream (N=1,2,3)	
tx_xcvr_clkout	tx_ss_clk	—
rx_xcvr_clkout	rx_ss_clk	—

Related Information

- **Introduction to Altera IP Cores**
- **DisplayPort IP Core User Guide**
- **Errata for DisplayPort IP Core in the Knowledge Base**

DisplayPort IP Core v14.0

Table 21-4: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Description	Impact
Added PHY Presets for Arria V, Cyclone V, and Stratix V device families.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added single clock reference (135MHz) for source and sink.	
Removed Native PHY from the IP core.	-
Updated register map and API functions.	-

Related Information

- **Introduction to Altera IP Cores**
- **DisplayPort IP Core User Guide**
- **Errata for DisplayPort IP Core in the Knowledge Base**

DisplayPort IP Core v13.1

Table 21-5: v13.1 November 2013

Description	Impact
Added support for Cyclone V devices.	-
Added HBR2 support for Arria V devices.	-
Added dual and quad pixel mode support.	-
Added quad symbol (40-bit) transceiver data interface support.	-
Added fast link training support.	-
Enhanced hardware demonstration designs: • Arria V device hardware demonstration design now demonstrates HBR2 functionality. • Hardware demonstration designs now demonstrate fast link training. • Hardware demonstration designs are now available for the Arria V FPGA Starter Kit development board and the Cyclone V GT development board	-
Updated register map and API functions.	-

Related Information

- **Introduction to Altera IP Cores**
- **DisplayPort IP Core User Guide**
- **Errata for DisplayPort IP Core in the Knowledge Base**

FIR II IP Core Revision History 22

2015.06.30

RN-IP Subscribe Send Feedback

FIR II IP Core v15.0

Table 22-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- FIR II IP Core User Guide
- Introduction to Altera IP Cores
- Errata for FIR II IP core in the Knowledge Base

FIR II IP Core v14.1

Table 22-2: v14.1 December 2014

Description	Impact
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- FIR II IP Core User Guide
- Introduction to Altera IP Cores
- Errata for FIR II IP core in the Knowledge Base

FIR II IP Core v14.0 Arria 10 Edition

Table 22-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition	-

Related Information

- **FIR II IP Core User Guide**
- **Introduction to Altera IP Cores**
- **Errata for FIR II IP core in the Knowledge Base**

FIR II IP Core v14.0

Table 22-4: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Added support for IP Catalog. For more information about IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **FIR II IP Core User Guide**
- **Introduction to Altera IP Cores**
- **Errata for FIR II IP core in the Knowledge Base**

FIR II IP Core v13.1

Table 22-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Added full support for Arria V and Stratix V devices	-

Related Information

- **FIR II IP Core User Guide**
- **Introduction to Altera IP Cores**
- **Errata for FIR II IP core in the Knowledge Base**

FFT IP Core Revision History 23

2015.06.30

RN-IP Subscribe Send Feedback

FFT IP Core v15.0

Table 23-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- FFT MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for FFT IP core in the Knowledge Base

FFT IP Core v14.1

Table 23-2: v14.1 December 2014

Description	Impact
Added hard-ffloating point option for Arria 10 devices.	-

Related Information

- FFT MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for FFT IP core in the Knowledge Base

FFT IP Core v14.0 Arria 10 Edition

Table 23-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Added two new buses, `source_data` and `sink_data`, which includes all Avalon-ST compilant data signals, when you instantiate the IP core as part of a Qsys system.	-
Removed global clock enable signal, `clk_ena`	-

Related Information

- **FFT MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for FFT IP core in the Knowledge Base**

FFT IP Core v14.0

Table 23-4: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Added support for IP Catalog. For more information about IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **FFT MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for FFT IP core in the Knowledge Base**

FFT IP Core v13.1

Table 23-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Added full support for Arria V and Stratix V devices	-

Related Information

- **FFT MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for FFT IP core in the Knowledge Base**

HDMI IP Core Revision History 24

2015.06.30

RN-IP Subscribe Send Feedback

HDMI IP Core v15.0 Update 1

Table 24-1: v15.0 Update 1 June 2015

Description	Impact
Fixed the timing violation on the oversampling block in the Arria V HDMI 2.0 design.	Upgrade if you are using the Arria V HDMI 2.0 design.

Related Information

- Introduction to Altera IP Cores
- Altera High-Definition Multimedia Interface User Guide
- Errata for HDMI IP core in the Knowledge Base

HDMI IP Core v15.0

Table 24-2: v15.0 May 2015

Description	Impact
Upgraded support for HDMI specification compliance from version 1.4b to 2.0.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added about 4-symbol per clock.	
Added Status and Control Data Channel (SCDC) for HDMI specification version 2.0.	

Added the following interface ports:
• HDMI source
  • `TMDS_Bit_clock_Ratio`
  • `Scrambler_Enable`
• HDMI sink
  • `TMDS_Bit_clock_Ratio`
• Avalon-MM SCDC Management
  • `scdc_i2c_clk`
  • `scdc_i2c_addr[7:0]`
  • `scdc_i2c_r`
  • `scdc_i2c_rdata[31:0]`
  • `scdc_i2c_w`
  • `scdc_i2c_wdata[31:0]`	

Related Information

- **Introduction to Altera IP Cores**
- **Altera High-Definition Multimedia Interface User Guide**
- **Errata for HDMI IP core in the Knowledge Base**

HDMI IP Core v14.1

Table 24-3: v14.1 December 2014

Description	Impact
Initial release.	-

Related Information

- **Introduction to Altera IP Cores**
- **Altera High-Definition Multimedia Interface User Guide**
- **Errata for HDMI IP core in the Knowledge Base**

Hybrid Memory Cube Controller IP Core Revision History 25

2015.06.30

RN-IP Subscribe Send Feedback

Hybrid Memory Cube Controller IP Core v15.0

Table 25-1: Version 15.0 May 2015

Description	Impact	Notes
Initial public release.		

Related Information

- Hybrid Memory Cube Controller IP Core User Guide
- Errata for Hybrid Memory Cube Controller IP core in the Knowledge Base

Interlaken PHY IP Core Revision History 26

2015.06.30

RN-IP Subscribe Send Feedback

Interlaken PHY IP Core v14.1 Revision History

Table 26-1: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-

Related Information

- Altera Transceiver PHY IP Core User Guide
- Errata for Interlaken PHY IP Core in the Knowledge Base
- Introduction to Altera IP Cores

Interlaken PHY IP Core v14.0 Revision History

Table 26-2: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- Altera Transceiver PHY IP Core User Guide
- Errata for Interlaken PHY IP Core in the Knowledge Base
- Introduction to Altera IP Cores

Interlaken PHY IP Core v13.1 Revision History

Table 26-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Errata for Interlaken PHY IP Core in the Knowledge Base**
- **Introduction to Altera IP Cores**

IP Compiler for PCI Express Revision History 27

2015.06.30

RN-IP Subscribe Send Feedback

IP Compiler for PCI Express v14.1

Table 27-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1.		

Related Information

- **IP Compiler for PCI Express User Guide**
- **Errata for IP Compiler for PCI Express in the Knowledge Base**

IP Compiler for PCI Express v14.0

Table 27-2: Version 14.0 June 2014

Description	Impact	Notes
Removed support for Cyclone III, Cyclone III LS, and Stratix III device families.	If your IP core variation targets one of these device families, and you choose to upgrade it to version 14.0, this change requires that you revise your IP core variation and regenerate it.	
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	Upgrading your IP core for this change is optional.	

Related Information

- **Introduction to Altera IP Cores**
- **IP Compiler for PCI Express User Guide**
- **Errata for IP Compiler for PCI Express in the Knowledge Base**

IP Compiler for PCI Express v13.1

Table 27-3: Version 13.1 November 2013

Description	Impact	Notes
Removed support for the Arria GX, Cyclone II, HardCopy II, HardCopy III, HardCopy IV, Stratix II, and Stratix II GX device families.	If your IP core variation targets one of these device families, and you choose to upgrade it to version 14.0, this change requires that you revise your IP core variation and regenerate it.	

Related Information

- **Introduction to Altera IP Cores**
- **IP Compiler for PCI Express User Guide**
- **Errata for IP Compiler for PCI Express in the Knowledge Base**

IP Compiler for PCI Express v13.0

Table 27-4: Version 13.0 May 2013

Description	Impact	Notes
Removed support for the SOPC Builder design flow.		

Related Information

- **Introduction to Altera IP Cores**
- **IP Compiler for PCI Express User Guide**
- **Errata for IP Compiler for PCI Express in the Knowledge Base**

JESD204B IP Core Revision History 28

2015.06.30

RN-IP Subscribe Send Feedback

JESD204B IP Core v15.0

Table 28-1: v15.0 May 2015

Description	Impact
Added support for Cyclone V FPGA device family (up to 5 Gbps).	–
Added new parameters: • **Enable Capability Registers** • **Set user-defined IP identifier** • **Enable Control and Status Registers** • **Enable Prbs Soft Accumulators** • **Enable manual F configuration**	–
Added new register bits to support error detection (refer to **Table 28-2**).	These new register bits are available when you upgrade the IP core to v15.0.

Table 28-2: New Register Bits

Register	Bit	Description
tx_err (0x60)	csr_pll_locked_err	Detects and flags an error when one or more lanes of PLL locked loses lock while the JESD204B link is running.
	csr_pcfifo_full_err	Detects and flags an error when one or more lanes of the Phase Compensation FIFO is unexpectedly full while the JESD204B link is running.
	csr_pcfifo_empty_err	Detects and flags an error when one or more lanes of the Phase Compensation FIFO is unexpectedly empty while the JESD204B link is running.

Register	Bit	Description
tx_err_enable (0x64)	csr_pll_locked_err_en	Enable interrupt for PLL lose lock error.
	csr_pcfifo_full_err_en	Enable interrupt for Phase Compensation FIFO full error.
	csr_pcfifo_empty_err_en	Enable interrupt for Phase Compensation FIFO empty error.
rx_err0 (0x60)	csr_rx_locked_to_data_err	Detects and flags an error when one or more lanes is not locked to data while the JESD204B link is running.
	csr_pcfifo_full_err	Detects and flags an error when one or more lanes of the Phase Compensation FIFO is unexpectedly full while the JESD204B link is running.
	csr_pcfifo_empty_err	Detects and flags an error when when one or more lanes of the Phase Compensation FIFO is unexpectedly empty while the JESD204B link is running.
rx_err_enable (0x74)	csr_rx_locked_to_data_err_en	Enable interrupt for RX not locked to data error.
	csr_pcfifo_full_err_en	Enable interrupt for Phase Compensation FIFO full error.
	csr_pcfifo_empty_err_en	Enable interrupt for Phase Compensation FIFO empty error.
rx_err_link_reinit (0x78)	csr_rx_locked_to_data_err_link_reinit	Enable link reinitialization for RX not locked to data error.
	csr_pcfifo_full_err_link_reinit	Enable link reinitialization for Phase Compensation FIFO full error.
	csr_pcfifo_empty_err_link_reinit	Enable link reinitialization for Phase Compensation FIFO empty error.

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**

JESD204B IP Core v14.1

Table 28-3: 14.1 December 2014

Description	Impact
Revised the parameter name of **Enable PLL/CDR Dynamic Reconfiguration** to **Enable Transceiver Dynamic Reconfiguration**.	–

Description	Impact
Added a new parameter—**Altera Debug Master Endpoint**. Enable this feature to access the reconfiguration space of the Transceiver Native PHY IP Core.	This feature is available only for Arria 10 device family.

Added new register bits:
• TX core:
  • Bit: `csr_reinit_w_rxsyncn_rise` in the `dll_ctrl` register (offset 0x50).
  • Description: This bit controls the Code Group Synchronization (CGS) state exit behavior during link re-initialization.
• RX core:
  • Bit: `csr_syncn_delay` in the `syncn_sysref_ctrl` register (offset 0x54).
  • Description: This bit extends the *SYNC_N* assertion (low state) by delaying the deassertion.
	The new register bits are available when you upgrade the IP core in your design to v14.1.

Updated the test_ilas_loop bit behavior in the `dll_ctrl` register (offset 0x50).	Upgrade the IP core in your design to v14.1 to implement this new behavior.
Changed the JESD204B Avalon-MM slave interface *readLatency* value from 0 to 1.	Upgrade the IP core in your design to v14.1 to implement this new behavior. If you upgrade your IP core in your design, you have to reconnect the IP core in your design due to port change.
Changed the interface type of the `jesd204_rx_int` and `jesd204_tx_int` signals from conduit to interrupt.	–
Changed signal type of `pll_locked`, `tx_cal_busy`, `rx_cal_busy`, and `rx_is_lockedtodata`.	–
New simulation flow for the IP core design example testbench. Changed the link bring up sequence by powering up the JESD204B TX link and JESD204B RX link independently.	Regenerate the design example from the IP Parameter Editor to obtain this change.
Changed the default value of the 8B/10B encoder to /K28.5/ control word during reset assertion to resolve the CDR lock issue in the receiver. This change only affects design that select **Enabled Soft PCS** for the **PCS Option** parameter.	If you use **Enabled Soft PCS** for the **PCS Option** parameter, you must upgrade the IP core in your design to v14.1.

Related Information

- **JESD204B IP Core User Guide**

- Errata for JESD204B IP core in the Knowledge Base

JESD204B IP Core v14.0 Arria 10 Edition Update 1

Table 28-4: 14.0 Arria 10 Edition Update 1 September 2014

Description	Impact
An optional upgrade is available for the JESD204B IP core in this release of the Altera Complete Design Suite. However, neither the IP Components window in the Project Navigator nor the IP Upgrade dialog box indicate that the upgrade is available. For information on features included in this optional upgrade, refer to the Altera Complete Design Suite Version 14.0 Arria 10 Edition Update Release Notes.	To upgrade your IP core, use the IP Parameter Editor for the JESD204B IP core to regenerate the core. Automatic upgrade is not available.

Related Information

- JESD204B IP Core User Guide
- Errata for JESD204B IP core in the Knowledge Base

JESD204B IP Core v14.0 Arria 10 Edition

Table 28-5: 14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.

Description	Impact
New `pll_locked` signal behavior: • Changed the signal direction from output to input. • Changed the signal width to follow the number of lanes selected instead of fixed at 1 bit.	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition, this change requires that you regenerate the IP core manually and reconnect it in your design.
Added the following signals for JESD204B IP core variations that target an Arria 10 device: • `tx_bonding_clocks` signal on the transmitter path if you select *bonded* for the **Bonded Mode** option • `tx_serial_clk0` signal on the transmitter path if you select *non-bonded* for the **Bonded Mode** option. • `reconfig_clk`, `reconfig_reset`, `reconfig_avmm_address`, `reconfig_read`, `reconfig_readdata`, `reconfig_avmm_waitrequest`, `reconfig_write`, and `reconfig_writedata` if you turn on **Enable PLL/CDR Dynamic Reconfiguration**.	
Removed the following signals for JESD204B IP core variations that target an Arria 10 device: • `reconfig_to_xcvr` • `reconfig_from_xcvr` • `pll_ref_clk` on the transmitter path • `pll_powerdown` on the transmitter path	

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**

JESD204B IP Core v14.0

Table 28-6: 14.0 June 2014

Description	Impact
Initial release.	-

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**

LDPC IP Core Revision History 29

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LDPC IP Core v15.0

Table 29-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- LDPC IP Core User Guide
- Introduction to Altera IP Cores
- Errata for FIR II IP core in the Knowledge Base

LDPC IP Core v14.1

Table 29-2: v14.1 December 2014

Description	Impact
Initial release	-

Related Information

- LDPC IP Core User Guide
- Introduction to Altera IP Cores
- Errata for FIR II IP core in the Knowledge Base

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core Revision History 30

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Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v15.0

Table 30-1: Version 15.0 May 2015

Arria 10 support for this IP core is available in the Altera MegaCore IP Library. Stratix V support is available only through the Self-Service Licensing center.

Description	Impact	Notes
If you upgrade the LL 40-100GbE IP core to the IP core v15.0, the example design no longer functions correctly. You must regenerate the example design after you upgrade.	After you upgrade your IP core, you must regenerate the example design.	
Added optional Synchronous Ethernet support for Arria 10 variations. Turning on the new **Enable SyncE** parameter adds a new RX recovered clock output signal.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core unless you turn on the **Enable SyncE** parameter. If you upgrade, turn on this parameter, and intend to implement a Synchronous Ethernet system, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
Changed handling of received malformed packets: • The IP core asserts the `l<n>_rx_error[0]` or `rx_error[0]` signal in the case of an unexpected control character that is not an Error character. • Both the LL 40GbE IP core and the LL 100GbE IP core handle received malformed packets the same way.	If you upgrade your IP core to the v15.0 version, you must be aware of this behavior change.	

Description	Impact	Notes
New output signals explain the control frames that the IP core passes to the RX client interface. The output flags indicate whether the control frame is a standard flow-control frame, a priority-based flow-control frame, or a non-flow control frame.	Upgrading the IP core to incorporate this feature is optional. This feature adds top-level output signals to the IP core. Therefore, to utilize this feature after you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
Priority-based flow control is now available for both LL 40GbE IP core variations and LL 100GbE IP core variations. Previously it was available only in LL 100GbE variations.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
New output status flag indicates when TX lanes are fully aligned and ready to transmit data.	Upgrading the IP core to incorporate this feature is optional. This feature adds top-level output signals to the IP core. Therefore, to utilize this feature after you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
New option to direct the IP core to insert an error in a transmitted Ethernet frame.	Upgrading the IP core to incorporate this feature is optional. This feature adds top-level input signals to the IP core. Therefore, if you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
The IP core now generates an example project that you can configure on a device, for most variations. The older type of example projects, which you cannot configure on a device, are also generated.	Upgrading the IP core to incorporate this feature is optional.	
Minor changes to LL 40GBASE-KR4 feature parameters and registers: • Changed default value of link training **INITPOSTVAL** parameter from 22 to 13. • Changed `rx_ctle_mode` LL 40GBASE-KR4 register field. The IP core uses only the two least significant bits of the 10GBASE-KR register field.	If you upgrade your IP core to the v15.0 version, you must be aware of these changes, and set the parameter and access the register accordingly, in LL 40GBASE-KR4 variations..	

Table 30-2: LL 40-100GbE IP Core Signal Changes v15.0

Signals added or modified in version 15.0.

Old Signal Name	New Signal Name	Notes
—	`clk_rx_recover`	Output RX recovered clock intended to drive the input reference clock of another Ethernet component in a Synchronous Ethernet design. This signal is available if you turn on **Enable SyncE** in the LL 40-100GbE parameter editor.
—	`l<n>_rx_status[2:0]` (Avalon-ST client interface)	New three-bit control frame type flag.
—	`rx_status[2:0]` (custom client interface)	
—	`tx_lanes_stable`	New output status flag.
—	`l<n>_tx_error` (Avalon-ST client interface)	New TX error insertion signal. User logic asserts a bit to direct the IP core to insert an error in the corresponding frame on the Ethernet link.
—	`tx_error[1:0]` or `tx_error[3:0]` (custom client interface)	

Related Information

- **Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide**
- **Errata for Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base**

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v14.1

Table 30-3: Version 14.1 December 2014

Arria 10 support for this IP core is available in the Altera MegaCore IP Library. Stratix V support is available only through the Self-Service Licensing center.

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Description	Impact	Notes
Added optional 40GBASE-KR4 support in LL 40GbE IP core variations. Turning on the **Enable KR4** parameter makes many additional 40GBASE-KR4 specific parameters available. 40GBASE-KR4 variations have many additional registers but no additional signals.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
All statistics increment vectors are now available and functional whether or not you include the relevant statistics counters in your IP core variations. Previously, the statistics increment vectors were functional only in IP core variations that included the relevant statistics module.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
Added option to move the TX MAC PLL outside the IP core. Turning on the **Use external TX MAC PLL** parameter adds an input clock that drives the `clk_txmac` internal clock. This option adds no additional registers or register fields.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core unless you turn on the **Use external TX MAC PLL** parameter.	Refer to LL 40-100GbE IP Core Signal Changes table.
Added two new 64-bit statistics counters RXOctets_OK at offset 0x960 and TXOctets_OK at offset 0x860 to count the payload bytes (octets) in received and transmitted frames with no FCS errors, undersized, oversized, or payload length errors. The two registers each have two associated new signals.	Upgrading the IP core to incorporate this feature is optional. If you upgrade the IP core to the v14.1 version, this feature adds top-level signals and therefore requires that you reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes table.
Added new `CFG_PLEN_CHECK` register at offset 0x50A to support bit[4] of the new six-bit RX error signal.	If you upgrade your IP core to the v14.1 version and wish to use the new length checking status flag, you must ensure that user logic turns on the enable bit in this new register. In addition, the register supports a new RX error status flag signal that requires that you reconnect the IP core in your design.	

Description	Impact	Notes
Changed handling of received malformed packet. If the IP core detects an incoming unexpected control character, it generates an EOP for the packet. Previously the IP core did not terminate (generate an EOP for) an incoming packet if it received an unexpected control character. In addition the IP core signals an error on the new six-bit RX error status signal when appropriate.	If you upgrade your IP core to the v14.1 version, you must be aware of this behavior change.	
Newly generated IP cores do not have top-level signals that interface to modules that the IP core does not include. This change applies to the TX MAC input clock, link fault signals, pause signals, and PTP signals.	Because of the backward compatibility feature described in the Notes column, if you upgrade your IP core to the v14.1 version, this feature has no effect on the top-level signals and does not require any additional actions. Note that this feature applies only to IP core variations that do not instantiate the relevant module or modules.	For backward compatibility, if you upgrade an IP core variation, link fault signals, pause top-level signals, and PTP signals in the earlier release of the IP core variation remain available in the 14.1 version after upgrade.
Updated PTP module behavior and modified parameter name. If you turn on **Enable 1588 PTP**, the PTP module has the following new features and requirements:	Upgrading the IP core to incorporate this feature is optional. If you upgrade the IP core to the v14.1 version, and the PTP module is included in your original IP core variation, this feature adds top-level signals and therefore requires that you reconnect the IP core in your design.	

Description	Impact	Notes
• You must instantiate a time-of-day (TOD) module and connect it to the IP core. • Added new PTP signals to receive the timestamps the TOD module generates in the two clock domains. Refer to LL 40-100GbE IP Core Signal Changes table. • Removed TX PTP module TOD calculation registers at offsets 0xB06 through 0xB08. The TOD module now provides the functionality the registers supported in previous versions of the IP core. • Added support for resetting the TCP checksum to zero of the application does not recalculate it. Added two new signals with which the application communicates such a request to the IP core. Refer to LL 40-100GbE IP Core Signal Changes table.		
Improved RX skew tolerance to 1900 bits for LL 40GbE IP core variations and to 1000 bits for LL 100GbE IP core variations. Altera LL 40-100GbE IP cores exceed the IEEE 802.3-2012 Ethernet Standard Clause 82.2.12 requirements of 1856 bits skew tolerance for 40GbE IP cores and 928 bits skew tolerance for 100GbE IP cores.		

Table 30-4: LL 40-100GbE IP Core Signal Changes

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	`clk_txmac_in`	Input clock to drive the `clk_txmac` internal clock. This signal is available if you turn on **Use external TX MAC PLL** in the LL 40-100GbE parameter editor.

Old Signal Name	New Signal Name	Notes
l<n>_rx_error (1 bit)	`l<n>_rx_error[5:0]` (Avalon-ST client interface)	New six-bit RX error status signal.
—	`rx_error[5:0]` (custom client interface)	
—	`unidirectional_en`	Signals that provide status from the `LINK_FAULT_CONFIG` register.
—	`link_fault_gen_en`	
—	`tx_inc_octetsOK[15:0]`	Signals that provide per-frame information associated with the new RxOctets_OK and TXOctets_OK registers. These signals are present and functional whether or not you turn on **Enable TX statistics** or **Enable RX statistics** in the parameter editor.
—	`tx_inc_octetsOK_valid`	
—	`rx_inc_octetsOK[15:0]`	
—	`rx_inc_octetsOK_valid`	
—	`tx_in_zero_tcp`	Signals for application to direct the IP core to reset the TCP checksum field.
—	`tx_in_tcp_offset[15:0]`	
—	`tod_txmac_in[95:0]`	Signals to receive TOD values from new external TOD module.
—	`tod_rxmac_in[95:0]`	
Link fault signals are present in new IP core variations you generate in the Quartus II v14.1 IP Catalog only if you turn on **Enable link fault generation** in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.		
Pause signals are present in new IP core variations that you generate in the Quartus II v14.1 IP Catalog only if you set **Flow control mode** to standard flow control or priority-based flow control in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.		
PTP interface signals are present in new IP core variations that you generate in the Quartus II v14.1 IP Catalog only if you turn on **Enable 1588 PTP** in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.		

Related Information

- **Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide**
- **Errata for Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base**

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0 Arria 10 Edition

Table 30-5: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Initial release in the Altera MegaCore IP Library.		

Related Information

- Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Errata for Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base

Low Latency Ethernet 10G MAC IP Core Revision History 31

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Low Latency Ethernet 10G MAC IP Core v15.0

Table 31-1: v15.0 May 2015

Description	Impact
Added new registers: • Software reset register for TX and RX datapaths. • Transfer status registers for TX and RX datapaths. • VLAN and stacked VLAN detection disable. • Programmable IPG registers for 10G and 10M/100M/1G operating speeds.	If you do not upgrade your IP core, it does not have this new feature.

Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

Low Latency Ethernet 10G MAC IP Core v14.1

Table 31-2: v14.1 December 2014

Description	Impact
Added new parameter options: • Enable 10GBASE-R register mode • Time of Day Format.	If you do not upgrade your IP core, it does not have this new feature.
Added new signals to support 10GBASE-R register mode: • `tx_xcvr_clk` • `rx_xcvr_clk` • `xgmii_tx_valid` • `xgmii_rx_valid`	

Related Information

- **Introduction to Altera IP Cores**
- **Low Latency Ethernet 10G MAC MegaCore Function User Guide**
- **Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base**

Low Latency Ethernet 10G MAC IP Core v14.0 Arria 10 Edition

Table 31-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition, all of the changes require that you regenerate the IP core manually and reconnect it in your design.

Related Information

- **Introduction to Altera IP Cores**
- **Low Latency Ethernet 10G MAC MegaCore Function User Guide**
- **Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base**

Low Latency Ethernet 10G MAC IP Core v14.0

Table 31-4: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for unidirectional feature.	The following changes are optional. If you do not upgrade your IP core, it does not have these new features.
Modified the reset behavior—TX and RX reset signals changed from asynchronous reset to synchronous reset.	
Resource improvement with no impact to performance.	

Related Information

- **Introduction to Altera IP Cores**
- **Low Latency Ethernet 10G MAC MegaCore Function User Guide**
- **Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base**

Low Latency Ethernet 10G MAC IP Core v13.1 Arria 10 Edition

Table 31-5: v13.1 Arria 10 Edition December 2013

Description	Impact
Added support for Arria 10 devices.	-

Related Information

- **Introduction to Altera IP Cores**
- **Low Latency Ethernet 10G MAC MegaCore Function User Guide**
- **Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base**

Low Latency Ethernet 10G MAC IP Core v13.1

Table 31-6: v13.1 November 2013

Description	Impact
Initial release. • Lowest latency 10-Gbps Ethernet MAC with 32-bit user interface mode. • Final support for Arria V GZ and Stratix V devices.	-

Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

Nios II Processor Revision History 32

2015.06.30

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Note: Unless otherwise noted, the Nios II processor supports new device families as they are supported by the Quartus II software.

Table 32-1: Product Revision History

Version	Date	Description
15.0	June 2015	Enhanced device and IP support
14.1	December 2014	• The Nios II Gen2 processor is fully supported. • Enhanced device and IP support
14.0 A10	August 2014	The Nios II Gen2 processor supports 14.0 Arria 10 Edition.

14.0	June 2014	• Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.
		• Fixed issue concerning instruction cache operation with ECC
		• Added Nios II Gen2 core
		  • Improved Nios II/f core.
		  • ECC support for data cache and TCMs.
		  • Optional 32-bit addressing.
		  • Faster arithmetic instructions.
		  • Optional uncached peripheral memory region.
		  • More flexible debugging options.
		  • Avalon streaming interface for trace.
		  • Includes Nios II/f and Nios II/e. Nios II/s processor core not supported.
		  • Simpler, more flexible parameter editor in Qsys.
		• Removed support for the following devices:
		  • Stratix III
		  • Cyclone III
		  • Cyclone III LS

Version	Date	Description
13.1 A10	December 2013	Verified in the Quartus II software v13.1 A10

13.1	November 2013	• Enhanced floating point custom instruction support
		• Added ECC support
		• Added RTL Nios II processor trace simulation support
		• Verified in the Quartus II software v13.1
		• Removed support for the following devices:
		  • Arria GX
		  • Cyclone, Cyclone II
		  • HardCopy II, HardCopy III, and HardCopy IV
		  • Stratix, Stratix II, Stratix GX, and Stratix II GX

Related Information

- **IP Catalog and Parameter Editor**
  For more information about the IP Catalog, refer to "IP Catalog and Parameter Editor" in the *Introduction to Altera IP Cores*.
- **Nios II Embedded Design Suite Release Notes**
- **Altera Knowledge Base**
  You can search for Nios II processor errata in the Altera Knowledge Base.

What's New in v15.0

New Nios II processor and related embedded IP features:

- VHDL simulation issue resolved.
- Improved support for the MAX 10 analog-to-digital converter (ADC) through the enhanced MAX 10 ADC interface IP core.
- Support for MAX 10 dual ADC simultaneous sampling.
- Support for new generic Quad SPI (QSPI) Controller IP core.
- Support for MAX 10 Remote Update IP core.
- Nios II Flash Accelerator, available in the Nios II component editor, for increased performance when running from user flash memory (beta release).

There is a known issue with the Floating Point Hardware 2 square root custom instruction. To download a patch, refer to the *Square Root Error in Floating Point Custom Instruction 2* topic in the Knowledge Base.

Related Information

Square Root Error in Floating Point Custom Instruction 2

What's New in v14.1

The Nios II Gen2 processor is fully supported.

Other new Nios II processor and related embedded IP features:

- The original Nios II processor is referred to as the Nios II Classic processor.
- The electrically programmable configuration quad-serial (EPCQ) controller IP core is upgraded to support x4 mode and EPCQ low-voltage (EPCQ-L) devices.
- Both Nios II processor cores support the generic QSPI Controller IP core as a beta release.
- The Nios II Gen2 processor supports the MAX 10 Altera Flash Controller IP core, which interfaces MAX 10 flash memory to FPGA logic.

Related Information

- **Nios II Classic Processor Reference Handbook**
- **Nios II Gen2 Processor Reference Handbook**
- **Nios II Gen2 Migration Guide**

What's New in v14.0 Arria 10 Edition

Arria 10 FPGA devices are supported by the Nios II Gen2 processor, but not by the classic Nios II processor. To implement a Nios II system on an Arria 10 device, you must use the Nios II Gen2 processor core.

What's New in v14.0

The Nios II Gen2 Processor Core

In v14.0, the Nios II processor core includes a preview implementation of the Nios II Gen2 processor core, supporting Altera's latest device families. The Nios II Gen2 processor core delivers size and performance similar to the original Nios II processor, and is compatible with classic Nios II processor code at the binary level.

The tool flow and HAL include options to support Gen2 features. The workflow for generating BSPs and building software is the same, but BSPs generated for the classic Nios II processor must be regenerated.

Differences Between Classic and Gen2 Nios II Processors

Differences between the Nios II Gen2 core and the classic Nios II core include:

- Improved Nios II/f core
- Optional 32-bit addressing
- Improved parameter editor in Qsys

The Nios II/s core option is not available with the Nios II Gen2 core. You can create a processor configuration identical to the Nios II/s by configuring the Nios II/f Gen2 core appropriately.

Differences Between Classic and Gen2 Nios II/f Processors

Feature	Classic Nios II/f	Nios II/f Gen2
32-bit addressing	No	Optional
Configurable-size uncached peripheral memory region	No	Optional

Feature	Classic Nios II/f	Nios II/f Gen2
Uncached write updates cached data	Yes	No
Static branch prediction	No	Optional
ECC	Starting in v13.1, optional on: • Processor core RAMs • Instruction cache	Optional on: • Processor core RAMs • Instruction cache • Data cache • Tightly-coupled memories (instruction and data)
32-bit multiply performance	5 cycles	1 cycle
64-bit multiply support	Devices with DSP blocks	All devices
Low-cost shifter	1 bit/cycle	4 bits/cycle

The Nios II/f Gen2 processor core also features the following improvements over the classic Nios II/f core:

- Divide performance is higher on average, and more deterministic.
- The JTAG debug options offer more flexibility in the number of hardware breakpoints and triggers.

On the Nios II/f Gen2 processor core, off-chip trace appears as an Avalon Streaming (Avalon-ST) interface. Therefore, off-chip trace requires the addition of an IP core to bridge between the Avalon-ST interface and the trace probe connection. Consult the supplier of your trace tool for the appropriate IP core.

Uncached Writes in the Nios II/f Gen2 Core

On an uncached write, if the data to be written happens to be cached, the classic Nios II processor updates the cache. On an uncached write, the Nios II/f Gen2 processor updates memory, but ignores the cache. Software must take this behavior into account.

Differences Between Classic and Gen2 Nios II/e Processors

The Nios II/e Gen2 core optionally supports 32-bit addressing.

Nios II Gen2 Processor Cores and MAX 10 FPGA Support

MAX 10 FPGA devices are supported by the Nios II Gen2 processor, but not by the classic Nios II processor. To implement a Nios II system on a MAX 10 device, you must use the Nios II Gen2 processor core.

The Altera On-chip Flash memory component, introduced in 14.0, enables Avalon-MM access to on-chip MAX 10 user flash memory. With this component, the Nios II boot copier can copy code to RAM from the MAX 10 user flash memory.

Upgrading to the Nios II Gen2 Processor

Existing Qsys systems containing the classic Nios II processor can be automatically upgraded to the Nios II Gen2 processor by running a TCL script.

Related Information

How can I migrate my Nios II processor design to the Nios II Gen 2 processor?

Nios II Processor Core ECC Fixes in 14.0

In v13.1, when configured with ECC protection, the Nios II processor could manifest invalid instruction cache operation with ECC errors. This issue is fixed in v14.0.

What's New in v13.1

Enhanced Floating Point Custom Instruction Support

In v13.1, Qsys adds an option to select a new floating point custom instruction set component, Floating Point Hardware 2. The component consists of the following custom instructions:

- One combinatorial custom instruction—implements comparison, minimum, maximum, negate, and absolute operations
- One multi-cycle custom instruction—implements add, subtract, multiply, divide, square root, and conversion operations

These custom instructions are binary compatible with the original Nios II floating point custom instructions. They offer better performance, with fewer cycles per operation.

Note: Floating point calculation results made with the Floating Point Hardware 2 custom instructions may differ slightly from those calculated by the original custom instructions, because the new instructions use a different rounding algorithm to increase performance.

Floating Point Hardware 2 appears in the Embedded Processor section in Qsys.

The Floating Point Hardware 2 instructions are available in VHDL only. They are IEEE 754-2008 compliant with the following exceptions:

- Simplified rounding.
- Simplified NaN handling.
- No exceptions generated. Exception conditions are indicated by a specific result, such as NaN.
- No status flags.
- Subnormal supported only on a subset of operations.

To take advantage of software support for the Floating Point Hardware 2 instructions, include **altera_nios_custom_instr_floating_point_2.h**, which forces GCC to call newlib math functions (rather than GCC built-in math functions). Altera recommends that you recompile newlib with for optimum performance.

Note: Do not use the `-mcustom -fpu-cfg` command-line option for GCC. This option does not support the Floating Point Hardware 2 instructions.

The Nios II software build tools (SBT) add individual `-mcustom` commands to the makefile to support the Floating Point Hardware 2 custom instructions.

ECC Support

Starting in v13.1, the Nios II Processor parameter editor lets you enable ECC protection for the RAMs in the processor core and the instruction cache. Single-bit soft errors are corrected, and dual-bit soft errors cause either an instruction cache flush or processor exception. ECC support is only available on the Nios II/f core without the data cache.

When ECC protection is selected, an Avalon-ST source is added to the processor core to provide ECC status information to external logic. By default, ECC is not enabled on reset. Therefore, software must

enable ECC protection. Software can also inject ECC errors into RAM data bits to support testing of the ECC exception handler and event bus.

The Nios II Hardware Abstraction Layer (HAL) is extended to support ECC initialization and exception handling.

Note: ECC is not supported with the data cache.

RTL Nios II Processor Trace Simulation Support

Starting in v13.1, the Nios II processor adds RTL trace simulation support. This feature enables Nios II processor instruction execution to be recorded during RTL simulation in ModelSim™. Events are recorded and time-stamped during RTL simulation. Examples of recorded events:

- Instruction execution
- Instruction address
- Data address
- Data value
- Interrupts
- Exceptions
- Resets
- Control register changes

The time stamp lets you align hardware simulation data with software execution.

This feature is enabled by selecting the appropriate option in the Nios II processor parameter editor. When trace simulation support is enabled, Qsys adds RTL to the Nios II testbench to support the generation of a trace (***.tr**) file. The ***.tr** file can be converted to human readable format with the `nios2-display-rtl` conversion tool.

NCO IP Core Revision History 33

2015.06.30

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NCO IP Core v15.0

Table 33-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- NCO MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for NCO IP Core in the Knowledge Base

NCO IP Core v14.1

Table 33-2: v14.1 December 2014

Description	Impact
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- NCO MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for NCO IP Core in the Knowledge Base

NCO IP Core v14.0 Arria 10 Edition

Table 33-3: v14.0 Arria 10 Edition

Description	Impact
Added two new buses, `in_data` and `out_data`, which includes all Avalon-ST compilant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- **NCO MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for NCO IP Core in the Knowledge Base**

NCO IP Core v14.0

Table 33-4: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Fixed a bug where the incorrect output frequency is generated when the accumulator precision is greater than or equal to 56 in single-channel configuration.	-
Fixed a mismatch between the C model and RTL when angular precision is less than or equal to 10 in serial CORDIC architecture.	-
Added support for IP Catalog. For more information about IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **NCO MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for NCO IP Core in the Knowledge Base**

NCO IP Core v13.1

Table 33-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Added full support for Arria V and Stratix V devices	-

Related Information

- **NCO MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for NCO IP Core in the Knowledge Base**

QDR II and QDR II+ SRAM Controller with UniPHY Revision History 34

2015.06.30

RN-IP Subscribe Send Feedback

QDR II and QDR II+ SRAM Controller with UniPHY v15.0

Table 34-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0	-

Related Information

- External Memory Interfaces Handbook
- Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base

QDR II and QDR II+ SRAM Controller with UniPHY v14.1

Table 34-2: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-

Related Information

- External Memory Interfaces Handbook
- Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base

QDR II and QDR II+ SRAM Controller with UniPHY v14.0

Table 34-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Removed support for Cyclone III, Cyclone III LS, and Stratix III devices	-

Related Information

- **External Memory Interfaces Handbook**
- **Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base**

QDR II and QDR II+ SRAM Controller with UniPHY v13.1

Table 34-4: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-
Removed support for HardCopy III and HardCopy IV devices	-

Related Information

- **External Memory Interfaces Handbook**
- **Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base**

RapidIO IP Core Revision History 35

2015.06.30

RN-IP Subscribe Send Feedback

RapidIO IP Core v15.0

Table 35-1: Version 15.0 May 2015

Description	Impact	Notes
The IP core loses lane synchronization when a lane receives three errored characters. Previously the IP core lost lane synchronization after receiving two errored characters on a lane.	Lane synchronization is slightly more robust.	

Table 35-2: RapidIO IP Core Signal Changes

Signals added or modified in version 15.0.

Old Signal Name	New Signal Name	Notes
—	`no_sync_indicator`	When this new output signal is low, it indicates at least one lane is not synchronized.

Related Information

- **RapidIO MegaCore Function User Guide**
- **Errata for RapidIO IP core in the Knowledge Base**

RapidIO IP Core v14.1

Table 35-3: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core	

Description	Impact	Notes
Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	variation and regenerate it in the Quartus II software v14.1.	

Related Information

- **RapidIO MegaCore Function User Guide**
- **Errata for RapidIO IP core in the Knowledge Base**

RapidIO IP Core v14.0 Arria 10 Edition

Table 35-4: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices). RapidIO IP core variations that target an Arria 10 device have the following differences from the variations that target earlier device families.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core and a reset controller in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in **the RapidIO IP Core Signal Changes table**.

Description	Impact	Notes
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, if you turn on the new parameter **Enable transceiver dynamic reconfiguration**, these variations have an internal reconfiguration controller that the user accesses through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in **the RapidIO IP Core Signal Changes table**.
If a RapidIO IP core that targets an Arria 10 device includes an I/O Logical layer Avalon-MM slave interface or an I/O Logical layer Avalon-MM master interface, the following conditions apply: • The IP core must include both an I/O Logical layer slave interface and an I/O Logical layer master interface. It cannot include one but not the other. • The I/O Logical layer slave module preserves transaction ordering between read and write operations. • The number of RX address translation windows is 16. • The number of TX address translation windows is 16.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
If a RapidIO IP core that targets an Arria 10 device includes an I/O Maintenance Logical layer module, the following conditions apply: • The module has both master and slave ports. • The number of Maintenance transmit address translation windows is 16. • The module supports both reception and transmission of `port-write` requests, or supports neither.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Description	Impact	Notes
A RapidIO IP core that targets an Arria 10 device supports both outbound and inbound DOORBELL messages, or it supports neither.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
If a RapidIO IP core that targets an Arria 10 device supports DOORBELL messages, it preserves transaction order between DOORBELL messages and I/O write request transactions.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
A RapidIO IP core that targets an Arria 10 device automatically synchronizes transmitted ackIDs.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Description	Impact	Notes
In a RapidIO IP core that targets an Arria 10 device, the number of `link-request` attempts before declaring a fatal error is tied to 7.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In a RapidIO IP core that targets an Arria 10 device, the Physical layer receive and transmit buffers are 32 Kbytes each.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In the parameter editor for RapidIO IP core variations that target an Arria 10 device, the **Disable Destination ID checking by default** parameter is not available. Arria 10 variations do not check destination IDs, by default. However, support for controlling this feature through the IP core registers is available in all RapidIO IP core variations, as it was in the previous release.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Table 35-5: RapidIO IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_bonded_clocks_ch<n>[5:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. Individual transceiver channel clock signals. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_clk_ch<n>	New Arria 10 transceiver reconfiguration interface. This interface is available if you turn on **Enable transceiver dynamic reconfiguration** in the RapidIO parameter editor. Relevant for Arria 10 variations only. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_reset_ch<n>	
—	reconfig_read_ch<n>	
—	reconfig_write_ch<n>	
—	reconfig_address_ch<n>[9:0]	
—	reconfig_readdata_ch<n>[31:0]	
—	reconfig_waitrequest_ch<n>	
—	reconfig_writedata_ch<n>[31:0]	
—	tx_analogreset[N-1:0]	New interface to external reset controller. Relevant for Arria 10 variations only. N is the number of RapidIO lanes.
—	rx_analogreset[N-1:0]	
—	tx_digitalreset[N-1:0]	
—	rx_digitalreset[N-1:0]	
reconfig_togxb	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V, Cyclone V, and Stratix V variations. This interface is present only in Arria V, Cyclone V, and Stratix V variations (as supported in past and future versions of the Quartus II software). These signals are not present in Arria 10 variations.
reconfig_fromgxb	Not present in Arria 10 variations.	

Related Information

- **RapidIO MegaCore Function User Guide**
- **Errata for RapidIO IP core in the Knowledge Base**

RapidIO IP Core v14.0

Table 35-6: Version 14.0 June 2014

Description	Impact	Notes
Removed support for Cyclone III, Cyclone III LS, and Stratix III device families. The Quartus II software v14.0 does not support these device families.	If your IP core variation targets one of these device families, this change requires that you revise your IP core variation and regenerate it.	
Removed support for Physical-layer only variations.	If your IP core variation is no longer supported, and you choose to upgrade the IP core, this change requires that you revise your IP core variation and regenerate it.	
Removed support for external transceivers. All supported variations include configuration of the high-speed transceivers on the target device.	If your IP core variation is no longer supported, and you choose to upgrade the IP core, this change requires that you revise your IP core variation and regenerate it.	
Removed naming differences between Qsys-generated and non-Qsys-generated IP core variations. New variations generated in the 14.0 software, whether in Qsys or outside Qsys, use the port names previously identified with the Qsys variations.	If your IP core was generated in the MegaWizard Plug-In Manager flow, and you choose to upgrade the IP core, this change requires that you revise your IP core variation, upgrade it, and reconnect your IP core in your design.	
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	This change is optional for v13.1 IP cores. However, IP upgrade is required for IP cores v13.0 and earlier.	

Related Information

- **Introduction to Altera IP Cores**
- **RapidIO MegaCore Function User Guide**
- **Errata for RapidIO IP core in the Knowledge Base**

RapidIO IP Core v13.1

Table 35-7: Version 13.1 November 2013

Description	Impact	Notes
Removed support for the Arria GX, Cyclone II, HardCopy II, HardCopy III, HardCopy IV E, HardCopy IV GX, Stratix II, and Stratix II GX device families.		

Related Information

- **RapidIO MegaCore Function User Guide**
- **Errata for RapidIO IP core in the Knowledge Base**

RapidIO IP Core v13.0

Table 35-8: Version 13.0 May 2013

Description	Impact	Notes
Added 2x mode for Arria V, Cyclone V, and Stratix V devices.		
Removed support for SOPC Builder design flow.		

Related Information

- **RapidIO MegaCore Function User Guide**
- **Errata for RapidIO IP core in the Knowledge Base**

RapidIO II IP Core Revision History 36

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RapidIO II IP Core v14.1

Table 36-1: Version 14.1 December 2014

Description	Impact	Note
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added `io_error_response_set` input port. The IP core sets the `IO_ERROR_RSP` field in bit [31] of the `Logical/Transport Layer Error Detect CSR` at offset 0x308 when this signal changes value from 0 to 1.	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, you must reconnect the IP core in your design so the new input signal does not float.	

Description	Impact	Note
Changed behavior of individual baud rate _ENABLE and _SUPPORT fields of Port 0 Control 2 CSR at offset 0x154. Instead of all being set to the value of 1, now the _SUPPORT fields for baud rates less than or equal to the value of the **Maximum baud rate** parameter have the value of 1, and the _SUPPORT fields for baud rates greater than the value of the **Maximum baud rate** parameter have the value of 0. Instead of all being set to the value of 1, now the _ENABLE field for the baud rate at which the IP core is operating has the value of 1, and the _ENABLE fields for all other baud rates have the value of 0.		If you upgrade the RapidIO II IP core in your design to the IP core v14.1, the Port 0 Control 2 CSR fields are set as expected to indicate the supported and enabled baud rates.

To modify the IP core to run at a different baud rate than the **Maxim**

Description	Impact	Note
Made changes to `Port 0 Control CSR` at offset 0x15C: • Added new field `PORT_ERR_IRQ_EN` that controls whether an interrupt is generated when an error is flagged in the `Port 0 Error Detect` register at offset 0x340. The new field is in bit [6] of the `Port 0 Control CSR`. • Moved `DIS_DEST_ID_CHK` field from bit [7] to bit [8]. • Moved `LOG_TRANS_ERR_IRQ_EN` field from bit [6] to bit [7].	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, your IP core implements the new behavior. You can use the new register field to force an interrupt in this case.	

Related Information

- **RapidIO II MegaCore Function User Guide**
- **Errata for RapidIO II IP core in the Knowledge Base**

RapidIO II IP Core v14.0 Arria 10 Edition

Table 36-2: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Note
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	

Description	Impact	Note
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in **the RapidIO II IP Core Signal Changes table**.
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, if you turn on the new parameter **Enable transceiver dynamic reconfiguration**, these variations have an internal reconfiguration controller that the user accesses through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in **the RapidIO II IP Core Signal Changes table**.

Table 36-3: RapidIO II IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_bonded_clocks_ch<n>[5:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. Individual transceiver channel clock signals. One signal (_ch<n>) for each RapidIO lane <n>.

Old Signal Name	New Signal Name	Notes
—	reconfig_clk_ch<n>	New Arria 10 transceiver reconfiguration interface. This interface is available if you turn on **Enable transceiver dynamic reconfiguration** in the RapidIO II parameter editor. Relevant for Arria 10 variations only. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_reset_ ch<n>	
—	reconfig_read_ ch<n>	
—	reconfig_write_ ch<n>	
—	reconfig_address_ ch<n>[9:0]	
—	reconfig_ readdata_ch<n> [31:0]	
—	reconfig_ waitrequest_ ch<n>	
—	reconfig_ writedata_ch<n> [31:0]	
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface signals for specific non-Arria 10 device families (as supported in past and future versions of the Quartus II software). These signals are not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	
pll_locked	Not present in Arria 10 variations.	
pll_powerdown	Not present in Arria 10 variations.	

Related Information

- **RapidIO II MegaCore Function User Guide**
- **Errata for RapidIO II IP core in the Knowledge Base**

RapidIO II IP Core v14.0

Table 36-4: Version 14.0 June 2014

Description	Impact	Note
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	This change is optional for v13.1 IP cores. However, IP upgrade is required for IP cores v13.0 and earlier.	
In case of `MAINTENANCE` Response with Error status, the `ADDRESS` field of the `Logical/Transport Layer Address Capture` CSR captures the `config_offset` value from the original request.	None. This change is optional. If you do not upgrade your IP core, it does not have this new feature.	
Added new allowed value IMPLEMENTATION SPECIFIC for `INFO_TYPE` field of `Port 0 Attributes Capture` CSR.	None. This change is optional. If you do not upgrade your IP core, it does not have this new feature.	

Related Information

- **Introduction to Altera IP Cores**
- **RapidIO II MegaCore Function User Guide**
- **Errata for RapidIO II IP core in the Knowledge Base**

RapidIO II IP Core v13.1

Table 36-5: Version 13.1 November 2013

Description	Impact	Note
Verified in the Quartus II software v13.1.		

Related Information

- **RapidIO II MegaCore Function User Guide**
- **Errata for RapidIO II IP core in the Knowledge Base**

RapidIO II IP Core v13.0

Table 36-6: Version 13.0 May 2013

Description	Impact	Note
Verified in the Quartus II software v13.0.		

Related Information

- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

Reed-Solomon II IP Core Revision History 37

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Reed-Solomon II IP Core v15.0

Table 37-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- Reed-Solomon II MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for Reed-Solomon II IP core in the Knowledge Base

Reed-Solomon II IP Core v14.0 Arria 10 Edition

Table 37-2: v14.0 Arria 10 edition August 2014

Description	Impact
Added two new buses, `in_data` and `out_data`, which includes all Avalon-ST compilant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- Reed-Solomon II MegaCore Function User Guide
- Introduction to Altera IP Cores
- Errata for Reed-Solomon II IP core in the Knowledge Base

Reed-Solomon II IP Core v14.0

Table 37-3: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Added variable decoding and encoding	-
Improved compilation time for large bits-per-symbol codes	-
Added support for IP Catalog. For more information about IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **Reed-Solomon II MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for Reed-Solomon II IP core in the Knowledge Base**

Reed-Solomon II IP Core v13.1

Table 37-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Added full support for Arria V and Stratix V devices	-
Added support for erasures-supporting decoders	-

Related Information

- **Reed-Solomon II MegaCore Function User Guide**
- **Introduction to Altera IP Cores**
- **Errata for Reed-Solomon II IP core in the Knowledge Base**

RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core Revision History 38

2015.06.30

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RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v15.0

Table 38-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0	-

Related Information

- External Memory Interface Handbook
- Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base

RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v14.1

Table 38-2: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-

Related Information

- External Memory Interface Handbook
- Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base

RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v14.0

Table 38-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Removed support for Cyclone III, Cyclone III LS, and Stratix III devices	-

Related Information

- **External Memory Interface Handbook**
- **Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base**

RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v13.1

Table 38-4: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-
Removed support for HardCopy III and HardCopy IV devices	-

Related Information

- **External Memory Interface Handbook**
- **Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base**

SDI Revision History 39

2015.06.30

RN-IP Subscribe Send Feedback

SDI v15.0

Table 39-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0	-

Related Information

- Introduction to Altera IP Cores
- SDI IP Core User Guide
- Errata for SDI IP Core in the Knowledge Base

SDI v14.0

Table 39-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Removed support for Cyclone III and Stratix III devices.	

Related Information

- Introduction to Altera IP Cores
- SDI IP Core User Guide
- Errata for SDI IP Core in the Knowledge Base

SDI v13.1

Table 39-3: v13.0 November 2013

Description	Impact
Verified in the Quartus II software v13.0	-

Related Information

- **Introduction to Altera IP Cores**
- **SDI IP Core User Guide**
- **Errata for SDI IP Core in the Knowledge Base**

SDI II IP Core Revision History 40

2015.06.30

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SDI II IP Core v15.0

Table 40-1: v15.0 May 2015

Description	Impact
Added the following parameters: • Added new video standard **Multi rate (up to 12G)** for Arria 10 devices. • Added TX PLL reference clock switching option for **Dynamic Tx clock switching** parameter.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Included design example for TX PLL reference clock switching. **Note:** Tx PLL reference clock switching is not supported for ATX PLL in Arria V GZ and Stratix V devices.	

Related Information

- Introduction to Altera IP Cores
- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base

SDI II IP Core v14.1

Table 40-2: v14.1 December 2014

Description	Impact
The **run_sim** script for each simulator is now located in its respective folder.	-

Description	Impact
`rx_format` signal now reports video transport format instead of picture format. The signal reports 3G Level A RGB or YCbCr 4:4:4 format.	If you update to the Quartus II software version 14.1, you must update your SDI II IP core to incorporate this fix.
Changed the names of the following parameters: • **Convert Level A to Level B (SMPTE 372M)** changed to **Convert HD-SDI dual link to 3G-SDI (level B)** • **Convert Level B to Level A (SMPTE 372M)** changed to **Convert 3G-SDI (level B) to HD-SDI dual link**	-

Related Information

- **Introduction to Altera IP Cores**
- **SDI II IP Core User Guide**
- **Errata for SDI II IP Core in the Knowledge Base**

SDI II IP Core v14.0 Update 2

Table 40-3: v14.0 Update 2 September 2014

Description	Impact
Fixed an issue in which RX cannot lock to HD-SDI standard in certain seed.	If you update to the Quartus II software version 14.0 Update 2, you must update your SDI II IP core to incorporate this fix.

Related Information

- **Introduction to Altera IP Cores**
- **SDI II IP Core User Guide**
- **Errata for SDI II IP Core in the Knowledge Base**

SDI II IP Core v13.1

Table 40-4: v13.1 November 2013

Description	Impact
Added support for segmented frame video format.	-
Added option for easier HD-SDI single-rate only reference clock selection.	-
Added ATX and CMU PLL selections for Arria V GZ and Stratix V devices.	-

Related Information

- Introduction to Altera IP Cores
- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base

SDI II IP Core v14.0 Arria 10

Table 40-5: v14.0 Arria 10 August 2014

Description	Impact
Added support for Arria 10 devices.	If you update your SDI II IP core to the the Quartus II software v14.0 Arria 10 Edition, all of the changes require that you regenerate the IP core manually and reconnect it in your design.
Removed the transceiver PHY and TX PLL from the SDI II IP core. You must generate the transceiver and the TX PLL separately.	
You will need to update your design if you are migrating to Arria 10 from a 28nm device family because the IP ports have changed.	
The Arria 10 variations include the following new signals: • Transceiver signals: `rx_ready`, `gxb_ltr`, `gxb_ltd`, `trig_rst_ctrl`, `rx_ready_b`, `gxb_ltr_b`, and `gxb_ltd_b`. • Transceiver Reconfiguration Controller signals: `xcvr_reconfig_clk`, `xcvr_reconfig_rst`, `xcvr_reconfig_write`, `xcvr_reconfig_read`, `xcvr_reconfig_address`, `xcvr_reconfig_writedata`, `xcvr_reconfig_readdata`, `xcvr_reconfig_waitrequest`, `cdr_reconfig_sel`, `cdr_reconfig_req`, `cdr_reconfig_busy`, `pll_sel`, `pll_sw_req`, `pll_busy`, `external_avmm_master_req`, `reconfig_write_from_ext_avmm_master`, `reconfig_read_from_ext_avmm_master`, `reconfig_address_from_ext_avmm_master`, `reconfig_writedata_from_ext_avmm_master`, `reconfig_readdata_from_ext_avmm_master`, and `reconfig_waitrequest_from_ext_avmm_master`. • Connecting input signals: `rx_manual` and `rx_is_lockedtodata`.	
Added **Example Design** options in the SDI II parameter editor.	

Related Information

- Introduction to Altera IP Cores
- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base

SDI II IP Core v14.0

Table 40-6: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Updated reconfiguration logic for enhanced rate switching stability.	-
Increased HD Dual Link timing difference requirement between links, in compliance with SMPTE372.	-

Related Information

- **Introduction to Altera IP Cores**
- **SDI II IP Core User Guide**
- **Errata for SDI II IP Core in the Knowledge Base**

SDI Audio IP Cores Revision History 41

2015.06.30

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SDI Audio IP Cores v15.0

Table 41-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0	-

Related Information

- Introduction to Altera IP Cores
- SDI Audio IP Cores User Guide
- Errata for SDI IP Core in the Knowledge Base

SDI Audio IP Cores v14.0

Table 41-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Removed support for Cyclone III and Stratix III devices.	-

Related Information

- Introduction to Altera IP Cores
- SDI Audio IP Cores User Guide
- Errata for SDI IP Core in the Knowledge Base

SDI Audio IP Cores v13.1

Table 41-3: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone and Cyclone II • HardCopy III and HardCopy IV • Stratix, Stratix GX, Stratix II, and Stratix II GX	-

Related Information

- **Introduction to Altera IP Cores**
- **SDI Audio IP Cores User Guide**
- **Errata for SDI IP Core in the Knowledge Base**

SerialLite II Revision History 42

2015.06.30

RN-IP Subscribe Send Feedback

SerialLite II v14.0

Table 42-1: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **Introduction to Altera IP Cores**
- **SerialLite II IP Core User Guide**
- **Errata for SerialLite II IP Core in the Knowledge Base**

SerialLite II v13.1

Table 42-2: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • HardCopy IV • Stratix GX and Stratix II GX	-
OpenCore Plus feature will not be supported for Arria V, Arria V GX, Cyclone V, and Stratix V devices.	-

Related Information

- **Introduction to Altera IP Cores**
- **SerialLite II IP Core User Guide**

- **Errata for SerialLite II IP Core in the Knowledge Base**

SerialLite III Streaming IP Core Revision History 43

2015.06.30

RN-IP Subscribe Send Feedback

SerialLite III Streaming IP Core v15.0

Table 43-1: v15.0 May 2015

Description	Impact
Updated `sync_tx` and `sync_rx` signal bus width to 8-bits.	–
Design example now supports simulation testbench based on user configurations in the Seriallite III Streaming IP core parameter editor.	–

Related Information

- SerialLite III Streaming MegaCore Function User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

SerialLite III Streaming IP Core v14.1

Table 43-2: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added support for 17.4 Gbps data rate in variations that target an Arria 10 device. In the parameter editor, added support for the value of 17.4 Gbps for the **Transceiver data rate per lane** parameter in variations that target an Arria 10 device.		

Related Information

- SerialLite III Streaming MegaCore Function User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

SerialLite III Streaming IP Core v14.0 Arria 10 Edition

Table 43-3: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices). SerialLite III IP core variations that target an Arria 10 device have the following differences from the variations that target earlier device families.	This IP core requires manual regeneration and reconnection in your design. You cannot use the standard process in the Quartus II IP Upgrade tool to upgrade this IP core. Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your SerialLite III IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	
Arria 10 variations have a new IP core name in the IP Catalog. Instead of **SerialLite III Streaming**, the Arria 10 IP core name is **Arria 10 SerialLite III Streaming**.	When you begin the regeneration process by selecting the IP core, note the change in IP core name in the IP Catalog.	
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in **the SerialLite III Streaming IP Core Signal Changes table**.
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, these variations have an internal reconfiguration controller that you access through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in **the SerialLite III Streaming IP Core Signal Changes table**.

Description	Impact	Notes
You must select the value for the **Transceiver reference clock frequency** parameter from a drop-down menu. The SerialLite III Streaming parameter editor does not automatically set the value for Arria 10 variations.		Parameter editor change.
The **Device speed grade** parameter is not available in the SerialLite III parameter editor for variations that target an Arria 10 device.		Parameter editor change.
If you specify the **Source** direction, you must set the value of the **Transceiver reference clock frequency** parameter to **none**. Arria 10 **Source** variations do not receive the transceiver TX reference clock as an input signal, and therefore this parameter does not modify the SerialLite III IP core.		Parameter editor change.
Currently, Arria 10 variations do not provide support for Transceiver data rate per lane greater than 15.625 Gbps.		
Currently, Altera does not provide a hardware design example for Arria 10 variations.		
The testbench you can generate from the SerialLite III parameter editor for Arria 10 variations is only available for **Sink** and **Duplex** directions. If your IP core has the value of the **Direction** parameter set to **Source**, the testbench does not simulate correctly with the IP core.		Testbench availability change.
The testbench you can generate from the SerialLite III parameter editor for Arria 10 variations automatically forces the DUT meta frame length to 200 words. If you specify a different value for the **Meta frame length** parameter, your IP core retains the value you specify, but when the testbench runs it simulates with the IP core meta frame length set to 200 words.		Testbench behavior change.

Table 43-4: SerialLite III Streaming IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_serial_clk[N-1:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. N is the number of IP core lanes.
—	tx_pll_locked	
phy_mgmt_clk	phy_mgmt_clk	In Arria 10 variations, this interface provides access to control Arria 10 transceiver reconfiguration, by connecting directly to the reconfiguration interface of the included Arria 10 Native PHY IP core. In Arria 10 variations, the width of `phy_mgmt_addr` is a value in the range of 11 to 16, depending on the number of lanes. (M is 10 to 15).
phy_mgmt_clk_reset	phy_mgmt_clk_reset	
phy_mgmt_read	phy_mgmt_read	
phy_mgmt_write	phy_mgmt_write	
phy_mgmt_addr[8:0]	phy_mgmt_addr[M:0]	
phy_mgmt_readdata[31:0]	phy_mgmt_readdata[31:0]	
phy_mgmt_waitrequest	phy_mgmt_waitrequest	
phy_mgmt_writedata[31:0]	phy_mgmt_writedata[31:0]	
reconfig_busy	reconfig_busy	Arria 10 variations of the IP core ignore this input signal.
xcvr_pll_ref_clk	xcvr_pll_ref_clk	Arria 10 Source-only variations of the iP core ignore this input signal.
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V GZ and Stratix V variations. This interface is present only in Arria V GZ and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Information

- **SerialLite III Streaming MegaCore Function User Guide**
- **Errata for SerialLite III Streaming IP core in the Knowledge Base**

SerialLite III Streaming IP Core v14.0

Table 43-5: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.		
Changed component subfolder name from **seriallite_iii** to **seriallite_iii_sv**.		

Related Information

- **Introduction to Altera IP Cores**
- **SerialLite III Streaming MegaCore Function User Guide**
- **Errata for SerialLite III Streaming IP core in the Knowledge Base**

SerialLite III Streaming IP Core v13.1

Table 43-6: Version 13.1 November 2013

Description	Impact	Notes
Added support for CRC-32 error injection.		
Added support for FIFO ECC protection.		

Related Information

- **SerialLite III Streaming MegaCore Function User Guide**
- **Errata for SerialLite III Streaming IP core in the Knowledge Base**

SerialLite III Streaming IP Core v13.0

Table 43-7: Version 13.0 May 2013

Description	Impact	Notes
Initial release.		

Related Information

- **SerialLite III Streaming MegaCore Function User Guide**
- **Errata for SerialLite III Streaming IP core in the Knowledge Base**

SmartVID Controller IP Core Revision History 44

2015.06.30

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SmartVID Controller v15.0

Table 44-1: v15.0 May 2015

Description	Impact
Updated the legal range for the VID Computation Delay (`VID_COMPUTE_DELAY`) register from 1 ms–1 second to 10 ms–1 second.	-

Related Information

- Introduction to Altera IP Cores
- SmartVID Controller User Guide
- Errata for SmartVID Controller IP core in the Knowledge Base

SmartVID Controller v14.1

Table 44-2: v14.1 December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- Introduction to Altera IP Cores
- SmartVID Controller User Guide
- Errata for SmartVID Controller IP core in the Knowledge Base

Stratix V Hard IP for PCI Express IP Core Revision History 45

2015.06.30

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Stratix V Hard IP for PCI Express IP Core v15.0

Table 45-1: v15.0 May 2015

Description	Impact
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

Related Information

- Introduction to Altera IP Cores
- Stratix V Avalon-ST Interface for PCIe Solutions User Guide
- Stratix V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Stratix V Hard IP for PCI Express in the Knowledge Base

Stratix V Hard IP for PCI Express IP Core v14.1

Table 45-2: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- Introduction to Altera IP Cores
- Stratix V Avalon-ST Interface for PCIe Solutions User Guide
- Stratix V Avalon-MM Interface for PCIe Solutions User Guide
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Stratix V Hard IP for PCI Express in the Knowledge Base

Stratix V Hard IP for PCI Express IP Core v14.0

Table 45-3: v14.0 June 2014

Description	Impact
Added preliminary support for Stratix V Hard IP for PCI Express with SR-IOV (Single Root I/O Virtualization).	-
Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core). • Revised programming model and optimized the performance of the Descriptor Controller. • Added support for either 128- or 256-bit interface to the Application Layer. • Added support for 64-bit addressing, making address translation unnecessary. • Added support for optional bursting RX Master for BAR2. • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. • Due to the many changes, the support level has reverted to preliminary.	The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to v14.0. Altera no longer support v13.1.

Description	Impact
Made the following changes to the Avalon-MM Stratix V Hard IP for PCI Express IP core: • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. • Added support for 64-bit addressing, making address translation unnecessary. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM. • Increased CRA address to 14 bits from 12 bits.	All of these new features are optional. If you include an optional feature that changes the port signature of your IP core, you must regenerate your design and connect the signals
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **Introduction to Altera IP Cores**
- **Stratix V Avalon-ST Interface for PCIe Solutions User Guide**
- **Stratix V Avalon-MM Interface for PCIe Solutions User Guide**
- **V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide**
- **Errata for Stratix V Hard IP for PCI Express in the Knowledge Base**

Stratix V Hard IP for PCI Express IP Core v13.1

Table 45-4: v13.1 November 2013

Description	Impact
Support for a Avalon-MM 256-Bit Hard IP for PCI Express Gen3 ×8 with DMA is final.	-
Support for Gen2 CvP is removed.	-

Related Information

- **Introduction to Altera IP Cores**
- **Stratix V Avalon-ST Interface for PCIe Solutions User Guide**
- **Stratix V Avalon-MM Interface for PCIe Solutions User Guide**

- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for Stratix V Hard IP for PCI Express in the Knowledge Base

Triple Speed Ethernet IP Core Revision History 46

2015.06.30

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Triple Speed Ethernet IP Core v15.0

Table 46-1: v15.0 May 2015

Description	Impact
You may observe hold time violation in designs targeting the Stratix® V, Arria V, Cyclone® V, and Arria 10 (10AS066ES) devices in this release.	Refer to the following errata for more information and the workaround: **Hold Time Violation in Triple Speed Ethernet IP Core**.

Related Information

- **Introduction to Altera IP Cores**
- **Triple Speed Ethernet MegaCore Function User Guide**
- **Errata for Triple Speed Ethernet IP core in the Knowledge Base**

Triple Speed Ethernet IP Core v14.0 Arria 10 Edition

Table 46-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition , all of the changes require that you regenerate the IP core manually and reconnect it in your design.

Related Information

- **Introduction to Altera IP Cores**
- **Triple Speed Ethernet MegaCore Function User Guide**

- Errata for Triple Speed Ethernet IP core in the Knowledge Base

Triple Speed Ethernet IP Core v14.0

Table 46-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added ECC support for M20K blocks.	Optional changes. If you do not upgrade your IP core, it does not have these new features:
Added 1588v2 support for LVDS variant.	

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

Triple Speed Ethernet IP Core v13.1 Arria 10 Edition

Table 46-4: v13.1 Arria 10 Edition December 2014

Description	impact
Added support for Arria 10 devices.	-

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

Triple Speed Ethernet IP Core v13.1

Table 46-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix II and Stratix II GX	-

Description	Impact
Added 1588v2 support for Arria V, Arria V SoC, Cyclone V, Cyclone V SoC and Stratix V devices.	-
Added 1588v2 support for MAC-only variants	-
Added ATX and CMU Tx PLL options for variations that include the PCS block targeting Arria V GZ and Stratix V devices.	-
Added SyncE support by separating Tx PLL and Rx PLL reference clock.	-
The period in nanosecond for csr registers: `tx_period`, `rx_period`, `Period`, and `AdjustPeriod`, was changed from bit 16 to 19 to bit 16 to 24.	-

Related Information

- **Introduction to Altera IP Cores**
- **Triple Speed Ethernet MegaCore Function User Guide**
- **Errata for Triple Speed Ethernet IP core in the Knowledge Base**

Video and Image Processing Suite Revision History 47

2015.06.30

RN-IP Subscribe Send Feedback

Caution: The Clipper and Test Pattern Generator IP cores are scheduled for product obsolescence and discontinued support. Therefore, Altera does not recommend use of these IP cores in new designs. For more information about Altera's current IP offering, refer to Altera's **Intellectual Property** website.

101 Innovation Drive, San Jose, CA 95134

Video and Image Processing Suite v15.0

Table 47-1: v15.0 May 2015

Description	Impact

• Updated the `Input (0-3) Enable` registers for the Mixer II IP core. The 1-bit registers are changed to 2-bit registers:
  • Set to bit 0 of the registers to display input 0.
  • Set to bit 1 of the registers to enable consume mode.
• Updated the parameter settings for the Mixer II IP core.
  • Added a new parameter **Pattern** which enables you to select the pattern for the background layer.
  • Removed **Color planes transmitted in parallel** . This feature is now default and internally handled through the hardware TCL file.
• Updated the parameter settings for the Frame Buffer II IP core.
  • Added support for the following parameters (these were not supported in the previous version): **Maximum ancillary packets per frame**, **Interlace support**, **Locked rate support**, **Run-time writer control**, and**Run-time reader control**
  • Removed **Ready latency** and **Delay length (frames)**. These features are fixed to 1 and internally handled through the hardware TCL file.
• Updated the parameter settings for the Avalon-ST Video Monitor IP core.
  • Added new parameters: **Color planes transmitted in parallel** and **Pixels in parallel**.
  • Removed **Number of color planes in sequence**. You can specify whether to transmit the planes in parallel or in series using the **Color planes transmitted in parallel** parameter.
	These changes are optional. If you do not upgrade your IP core, it does not have these new features.

Related Information

- **Introduction to Altera IP Cores**
- **Video and Image Processing Suite User Guide**
- **Errata for the Video and Image Processing Suite in the Knowledge Base**

Video and Image Processing Suite v14.1

Table 47-2: v14.1 December 2014

Description	Impact
Updated the parameters for Clocked Video Input II and Clocked Video Output II IP cores. • Edited the function of the **Use control port** parameter. The control ports will now only appear when you turn on this parameter. • Removed the **Generate Display Port output** parameter.	-

Related Information

- **Introduction to Altera IP Cores**
- **Video and Image Processing Suite User Guide**
- **Errata for the Video and Image Processing Suite in the Knowledge Base**

Video and Image Processing Suite v14.0 Arria 10 Edition

Table 47-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices only in the following IP cores: • Avalon-ST Video Monitor • Broadcast Deinterlacer • Clipper II • Clocked Video Input II • Clocked Video Output II • Color Space Converter II • Deinterlacer II • Frame Buffer II • Mixer II • Scaler II • Switch II • Test Pattern Generator II	-

Related Information

- **Introduction to Altera IP Cores**
- **Video and Image Processing Suite User Guide**
- **Errata for the Video and Image Processing Suite in the Knowledge Base**

Video and Image Processing Suite v14.0

Table 47-4: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. You can instantiate the VIP Suite IP cores only from the Qsys IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added new IP cores: Clocked Video Output II, Clocked Video Input II, Color Space Converter II, Mixer II, Frame Buffer II, Test Pattern Generator II, and Switch II.	-
Removed support for Cyclone III and Stratix III devices.	-

Related Information

- **Introduction to Altera IP Cores**
- **Video and Image Processing Suite User Guide**
- **Errata for the Video and Image Processing Suite in the Knowledge Base**

Video and Image Processing Suite v13.1

Table 47-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Improved the Broadcast Deinterlacer video-over-film mode scene change.	

Related Information

- **Introduction to Altera IP Cores**
- **Video and Image Processing Suite User Guide**
- **Errata for the Video and Image Processing Suite in the Knowledge Base**

Viterbi IP Core Revision History 48

2015.06.30

RN-IP Subscribe Send Feedback

Viterbi IP Core v15.0

Table 48-1: v15.0 May 2015

Description	Impact
Verified in the Quartus II software v15.0.	-

Related Information

- Viterbi IP Core User Guide
- Introduction to Altera IP Cores
- Errata for Viterbi IP core in the Knowledge Base

Viterbi IP Core v14.1

Table 48-2: v14.1 December 2014

Description	Impact
Added support for multiple codesets for Arria 10 devices.	-
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- Viterbi IP Core User Guide
- Introduction to Altera IP Cores
- Errata for Viterbi IP core in the Knowledge Base

Viterbi IP Core v14.0 Arria 10 Edition

Table 48-3: v14.0 Arria 10 Edition August 2014

Description	Impact
Added two new buses, `sink_data` and `out_data`, which includes all Avalon-ST compilant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- **Viterbi IP Core User Guide**
- **Introduction to Altera IP Cores**
- **Errata for Viterbi IP core in the Knowledge Base**

Viterbi IP Core v14.0

Table 48-4: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices.	-
Added preliminary support for MAX 10 FPGAs	-
Added support for IP Catalog. For more information about IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **Viterbi IP Core User Guide**
- **Introduction to Altera IP Cores**
- **Errata for Viterbi IP core in the Knowledge Base**

Viterbi IP Core v13.1

Table 48-5: v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Added full support for Arria V and Stratix V devices	-

Related Information

- **Viterbi IP Core User Guide**
- **Introduction to Altera IP Cores**
- **Errata for Viterbi IP core in the Knowledge Base**

V-Series Avalon-MM DMA for PCI Express IP Core Revision History 49

2015.06.30

RN-IP Subscribe Send Feedback

V-Series Avalon-MM DMA PCI Express IP Core v15.0

Table 49-1: v15.0 May 2015

Description	Impact
Added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	The IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.

Related Information

- Introduction to Altera IP Cores
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for V-Series Avalon-MM DMA Interface for PCI Express in the Knowledge Base

V-Series Avalon-MM DMA PCI Express IP Core v14.1

Table 49-2: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.
Added support for 128-Bit Avalon-MM RX master.	If you add this Avalon-MM RX master to your design, you must regenerate your IP core.

Related Information

- Introduction to Altera IP Cores

- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for V-Series Avalon-MM DMA Interface for PCI Express in the Knowledge Base

V-Series Avalon-MM DMA PCI Express IP Core v14.0

Table 49-3: v14.0 December 2014

Description	Impact
Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core). • Revised programming model and optimized the performance of the Descriptor Controller. • Added support for either 128- or 256-bit interface to the Application Layer. • Added support for 64-bit addressing, making address translation unnecessary. • Added support for optional bursting RX Master for BAR2. • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. • Due to the many changes, the support level has reverted to preliminary.	The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to v14.0. Altera no longer support v13.1.

Related Information

- Introduction to Altera IP Cores
- V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide
- Errata for V-Series Avalon-MM DMA Interface for PCI Express in the Knowledge Base

XAUI PHY Revision History 50

2015.06.30

RN-IP Subscribe Send Feedback

XAUI PHY IP Core v14.1 Revision History

Table 50-1: v14.1 December 2014

Description	Impact
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.
Added the **Enable phase compensation FIFO** parameter.	-
Added the `xgmii_rx_inclk` port, which is available when **Enable phase compensation FIFO** is enabled.	-
Added the `pll_cal_busy_i` port, which connects to the `pll_cal_busy` output port of the external PLL.	-
Added a new Arria 10 SDC constraint requirement. Refer to the "XAUI PHY TimeQuest SDC Constraint" section of the *Arria 10 Transceiver PHY User Guide*.	-

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Arria 10 Transceiver PHY User Guide**
- **Errata for XAUI PHY IP Core in the Knowledge Base**
- **Introduction to Altera IP Cores**

XAUI PHY IP Core v14.0 Arria 10 Revision History

Table 50-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices. To use the XAUI PHY IP core for Arria 10 devices, you must instantiate an external transmit PLL. You can only use the ATX PLL IP core with the XAUI PHY IP core for Arria 10 devices.	-
Added **Enable dynamic reconfiguration** parameter.	-
Removed the following parameters: • **PLL type**. • **External PMA control and configuration**.	-
Added new port to enable connectivity with an external transmit PLL and with the dynamic reconfiguration interface. Refer to the *Arria 10 Transceiver PHY User Guide* parameter and port descriptions.	-
The XAUI PHY IP core does not support NCSIM simulator. You will see an error message during elaboration.	-
The XAUI PHY IP core does not support VHDL. You will get a compilation error when you simulate the XAUI PHY IP core generated in VHDL. You must generate this IP core in Verilog.	-

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Arria 10 Transceiver PHY User Guide**
- **Errata for XAUI PHY IP Core in the Knowledge Base**
- **Introduction to Altera IP Cores**

XAUI PHY IP Core v14.0 Revision History

Table 50-3: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Errata for XAUI PHY IP Core in the Knowledge Base**
- **Introduction to Altera IP Cores**

XAUI PHY IP Core v13.1 Revision History

Table 50-4: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- **Altera Transceiver PHY IP Core User Guide**
- **Errata for XAUI PHY IP Core in the Knowledge Base**
- **Introduction to Altera IP Cores**

Other IP Cores Product Revision History 51

2015.06.30

RN-IP Subscribe Send Feedback

ALTERA_FP_FUNCTIONS v15.0

Table 51-1: v15.0 May 2015

Description	Impact
Added new functions: Multiply Add, Multiply Accumulate, Accumulate, and Scalar Product..	-
Added support for range reduction option for appropriate trigonometric functions.	-
Added **Manually Specify DSP Registers** option on the **Performance** tab that shows a GUI and allows you to target specific registers on Arria 10 devices. applies to Add, Subtract, Multiply Add functions	-
Added target option on the **Performance** tab to allow you to constrain both latency and frequency	-

Related Information

- Floating-Point Megafunctions User Guide
- Errata for other IP cores in the Knowledge Base

Altera Voltage Sensor IP Core v15.0

Table 51-2: v15.0 May 2015

Description	Impact
Initial release.	-

Related Information

- Altera Voltage Sensor IP Core User Guide
- Errata for other IP cores in the Knowledge Base

ALTERA_FP_MATRIX_MULT v14.1

Table 51-3: v14.1 December 2014

Description	Impact
Added support for Arria 10 device hard floating-point blocks.	Only for new IP cores.
Changed reset port. It is no longer optional and is always present	
Removed option to add an enable port	
Changed performance. Specify twice the number of memory blocks compared to previous version for the equivalent performance	
Changed the signals to use Avalon-ST interfaces.	Only for new IP cores. Any existing IP cores continue to have the same signals even when you edit and regenerate the IP core.
Changed `reset` to active low	

Related Information

- **Floating-Point Megafunctions User Guide**
- **Errata for other IP cores in the Knowledge Base**

Altera Advanced SEU Detection IP Core v14.1

Table 51-4: v14.1 December 2014

Description	Impact
Added support for double-adjacent SEU sensitivity processing.	Initiates an .smh lookup for correctable double-adjacent EDCRC errors instead of identifying such SEU as critical.
Added `critical_clear` signal to `errors` interface	-
Added `busy` signal to `errors` interface	For on-chip processing configuration only.

Related Information

- **Advanced SEU Detection IP Core User Guide**
- **Errata for other IP cores in the Knowledge Base**

Altera Dual Configuration v14.0 Update 2

Table 51-5: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- MAX 10 FPGA Configuration User Guide
- Errata for other IP cores in the Knowledge Base

Altera EMR Unloader IP Core v14.1

Table 51-6: v14.1 December 2014

Description	Impact
Fixed an issue with synchronization the of `CRCERROR` signal, which comes from the EDCRC circuitry that the internal oscillator drives.	-

Related Information

- Advanced SEU Detection IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera OCT IP Core v14.0 Arria 10 Edition

Table 51-7: v14.0 Arria 10 Edition August 2014

Description	Impact
• Changed signal names • Added user mode OCT	

Table 51-8: Signal Name Changes

Old Name	New Name	Notes
`core_rzqin_export`	`rzqin`	-
`core_series_termination_control_expor`	`oct_#_series_termination_control`	-
`core_parallel_termination_control_export`	`oct_#_parallel_termination_control`	-

Related Information

- Altera OCT Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

Altera GPIO IP Core v14.0 Arria 10 Edition

Table 51-9: v14.0 Arria 10 Edition August 2014

Description	Impact
Changed signal names	-

Table 51-10: Signal Name Changes

Old Name	New Name	Notes
core_ck_fr_in_export	ck_fr_in	
core_ck_fr_out_export	ch_fr_out	
core_ck_hr_in_export	ch_hr_in	
core_ck_hr_out_export	ch_hr_out	
core_dout_export	dout	
core_din_export	din	
core_oe_export	oe	
core_pad_io_export	pad_io	
core_pad_io_b_export	pad_io_b	
core_aclr_export	aclr	
core_sclr_export	sclr	
core_cke_export	cke	
core_ck_export	ck	
core_ck_in_export	ck_in	
core_ck_out_export	ck_out	
core_ck_fr_export	ck_fr	
core_ck_hr_export	ck_hr	
core_pad_in_export	pad_in	
core_pad_in_b_export	pad_in_b	
core_pad_out_export	pad_out	
core_pad_out_b_export	pad_out_b	
core_aset_export	aset	

Old Name	New Name	Notes
core_sset_export	sset	

Related Information

- Altera GPIO Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

Altera GPIO Lite IP Core v14.0 Update 2

Table 51-11: v14.0 Update 2 September 2014

Description	Impact
Initial release.	

Related Information

- MAX 10 General Purpose I/O User Guide
- Errata for other IP cores in the Knowledge Base

Altera Modular ADC IP Core v14.0 Update 2

Table 51-12: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- MAX 10 Analog to Digital Converter User Guide
- Errata for other IP cores in the Knowledge Base

Altera LVDS SERDES IP Core v14.1

Table 51-13: v14.1 December 2014

Description	Impact
Added internal PLL additional clock export parameter	-

Related Information

- Altera LVDS SERDES Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

Altera LVDS SERDES IP Core v14.0 Arria 10 Edition

Table 51-14: v14.0 Arria 10 Edition August 2014

Description	Impact
Added feature that creates **.sdc** file for generated designs (previously only for example designs)	-
Added support for external PLL mode	-
Added option to clock TX core registers using reference clock	-

Related Information

- **Altera LVDS SERDES Megafunction User Guide**
- **Errata for other IP cores in the Knowledge Base**

Altera PHYLite for Memory IP Core v14.1

Table 51-15: v14.1 December 2014

Description	Impact
Added internal PLL additional clock export parameter	-
Added setup delay constraint timing parameters in the **Group** tabs in the parameter editor	-

Related Information

- **Altera PHYLite for Memory Megafunction User Guide**
- **Errata for other IP cores in the Knowledge Base**

Altera PHYLite for Memory IP Core v14.0 Arria 10 Edition

Table 51-16: v14.0 Arria 10 Edition August 2014

Description	Impact
Added dynamic reconfiguration	-
Added I/O standard and OCT settings	-
Added complementary strobe type	-
Changed `pll_locked` port name to `interface_locked`	-

Related Information

- **Altera PHYLite for Memory Megafunction User Guide**

- Errata for other IP cores in the Knowledge Base

Altera On-Chip Flash IP Core v14.1

Table 51-17: v14.1 December 2014

Description	Impact
Added new parameters: • **Data interface** parameter. • **Read burst count** parameter. Adjusts the maximum burst count for Incrementing read mode. Also autoadjusts `burstcount` bus width. • **Serial** data interfaces • **Flash Memory**. Indicates the address mapping for each sector and adjusts the **Access Mode** for each sector individually	-
Replaced **Dual Images** parameter with **Configuration Scheme** and **Configuration Mode** parameters which includes all supported configuration modes. Use CFM as UFM during single image configuration mode without memory initialization.	
Fixed a bug, which allows you to adjust the **Read burst count** from 1 to 2 or 4 while using **WrappingRead burst mode**.	

Related Information

- MAX 10 User Flash Memory User Guide
- Errata for other IP cores in the Knowledge Base

Altera On-Chip Flash IP Core v14.0 Update 2

Table 51-18: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- MAX 10 User Flash Memory User Guide
- Errata for other IP cores in the Knowledge Base

Altera Soft LVDS IP Core v14.0 Update 2

Table 51-19: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- MAX 10 High-Speed LVDS I/O User Guide
- Errata for other IP cores in the Knowledge Base

Arria 10 Native Fixed Point DSP IP Core v14.1

Table 51-20: v14.1 December 2014

Description	Impact
Initial release. Only supports Arria 10 device family.	-

Related Information

- Arria 10 Native Fixed Point DSP IP Core User Guide
- Errata for other IP cores in the Knowledge Base

RAM: 1-port and RAM: 2-port v14.0 Arria 10 Edition

Table 51-21: v14.0 Arria 10 Edition August 2014

Description	Impact
Changed GUI. When upgrading, you lose any value in **Memory Initial Mode** > **File name**. For the work around, refer to the Knowledge Base.	-

Related Information

- Internal Memory (ROM and RAM) User Guide
- Errata for other IP cores in the Knowledge Base

SLD Hub Controller System v14.1

Table 51-22: v14.1 December 2014

Description	Impact
Enhanced the register map	The pre-v14.1 and v14.1 register maps are similar. Pre v14.1 register maps work unchanged with v14.1 hardware.

Related Information

Errata for other IP cores in the Knowledge Base

Internal Oscillator IP Core v14.0 Update 2

Table 51-23: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- MAX 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

Other Transceiver IP Cores Product Revision History 52

2015.06.30

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Transceiver PHY Reset Controller IP Core v14.1 Revision History

Table 52-1: v14.1 December 2014

Description	Impact
Added an optional port `pll_cal_busy`. To enable `pll_cal_busy` select **Enable pll_cal_busy input port** parameter under the **TX Channel** option in the Reset Controller IP Core parameter editor. If not enabled, then by default, this port is connected to 1'b0.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Transceiver PHY Reset Controller IP Core v14.0 Arria 10 Revision History

Table 52-2: v14.0 Arria 10 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Information

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

Transceiver PHY Reset Controller IP Core v13.0 Arria 10 Revision History

Table 52-3: v13.0 Arria 10 December 2013

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- **Arria 10 Transceiver PHY User Guide**
- **Errata for Transceiver IP Cores in the Knowledge Base**
- **Introduction to Altera IP Cores**