NOTES:

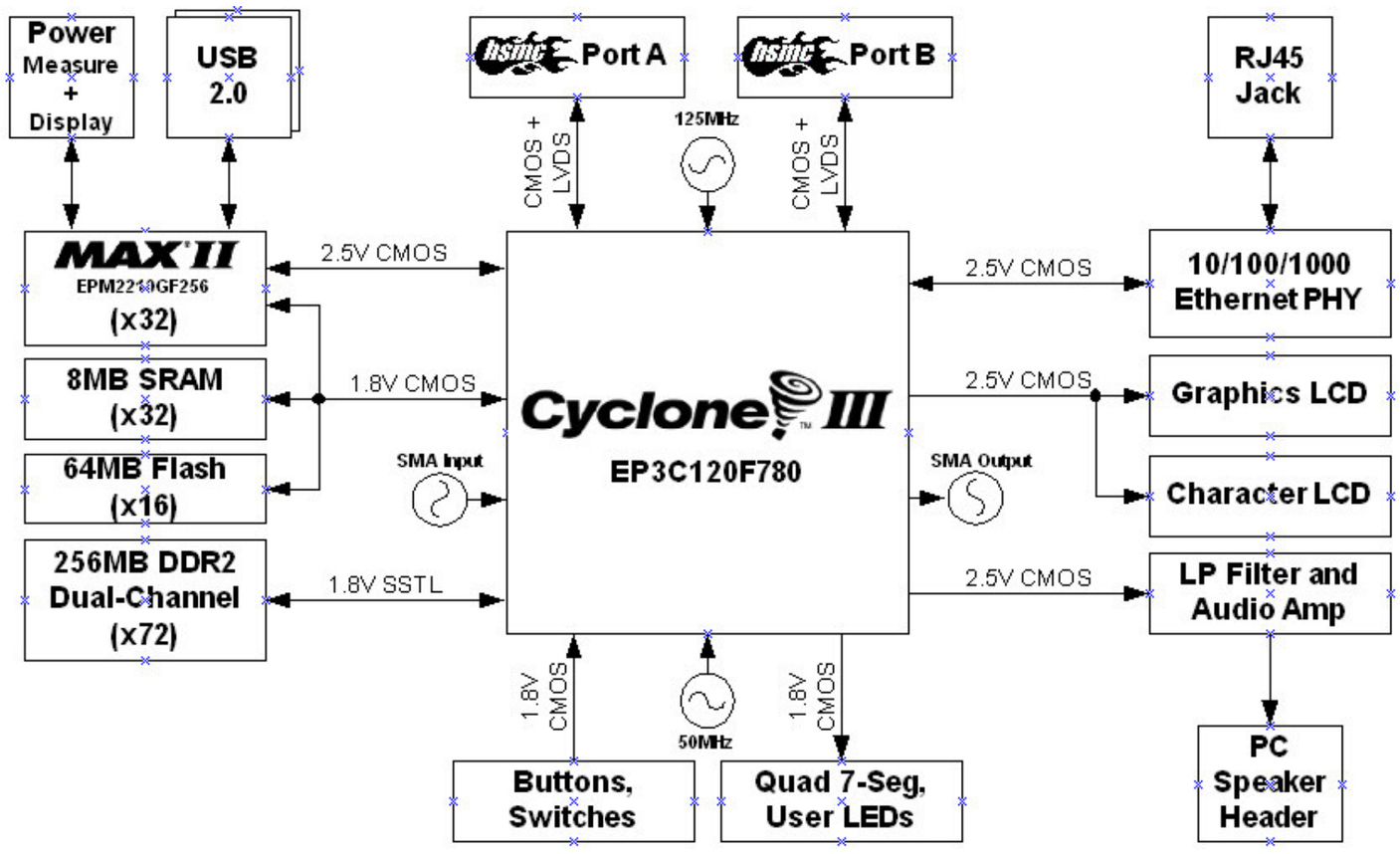
1. Project Drawing Numbers:

Raw PCB	100-0310703-D1
Gerber Files	110-0310703-D1
PCB Design Files	120-0310703-D1
Assembly Drawing	130-0310703-D1
Fab Drawing	140-0310703-D1
Schematic Drawing	150-0310703-D1
PCB Film	160-0310703-D1
Bill of Materials	170-0310703-D1
Schematic Design Files	180-0310703-D1
Functional Specification	210-0310703-D1
PCB Layout Guidelines	220-0310703-D1
Assembly Rework	320-0310703-D1

2. 938 Parts, 61 Library Parts, 803 Nets, 4689 Pins

REV	DATE	PAGES	DESCRIPTION
B-1	8/13/2007	ALL	Release B-1
C-1	10/2/2007	ALL	Moved C507 to pwr instead of gnd, Changed D35 to 40V schottky, Routed DEV_SEL & JTAG_SEL jumper signals back to MAXII, Changed VCCA and VCCD PLL power decoupling, Changed R35,R38 to DNI, Changed CPU_RESETn pullup to 2.5V and changed MAXII pin to 2.5V bank, Changed current sense circuit completely to version from SIII Host Board and added more measurements, Moved several MAXII pins to accomodate more 2.5V signals to power measurement circuit. Changed OLED display connector to DNI, Increased output and coupling caps on -12V reg
D-1	10/9/2007	3,4,5	Changed U18, C247-248, R140 to DNI and shorted pins 1 to 5 on U18. Changed R13,R24,R28,R32,R43,R44,R46,R48,R49,R51,R80,R81,R134 from 3mohm to 9mohm.

Cyclone III F780 Development Kit Host Block Diagram



PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	C3 FPGA Package Top
3	Power 1
4	Power 2
5	Current Sense
6	Cyclone III Power
7	Cyclone III Clocks
8	MAX II
9	DDR2 SDRAM (x72)
10	DDR2 SDRAM POWER & TERM
11	SRAM & FLASH
12	USB 2.0
13	10/100/1000 Ethernet
14	HSM Connectors
15	HSM Termination
16	User IO & Connector
17	Cyclone III Configuration
18	Cyclone III Banks 1,2,5&6
19	Cyclone III Banks 3,4,7&8
20	Decoupling
21	
22	
23	
24	
25	
26	
27	

Digital Ground

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Cyclone III FPGA Package Top

Notes:

1. FPGA Schematic Symbol Breakdown:
   - (A) Bank 1 - ENET,HSMA, LCD
   - (B) Bank 2 - ENET, HSMA, LCD
   - (C) Bank 3 - DDR2 SDRAM,FSA, HSMA (CLKIN), SRAM, USER I/O
   - (D) Bank 4 - DDR2 SDRAM, FLASH, FSA, SRAM, USER I/O
   - (E) Bank 5 - HSMB
   - (F) Bank 6 - HSMB, LCD, USB
   - (G) Bank 7 - DDR2 SDRAM, FSD, HSMB (CLKIN), MAX, USER I/O
   - (H) Bank 8 - DDR2 SDRAM, FSD, SRAM, USER I/O
   - (I) Some Clocks
   - (J) Configuration
   - (K) VCCINT, VCCA
   - (L) VCCIO, VREF
   - (M) Ground and NCs
   - (N) Ground
   - (O) Ground

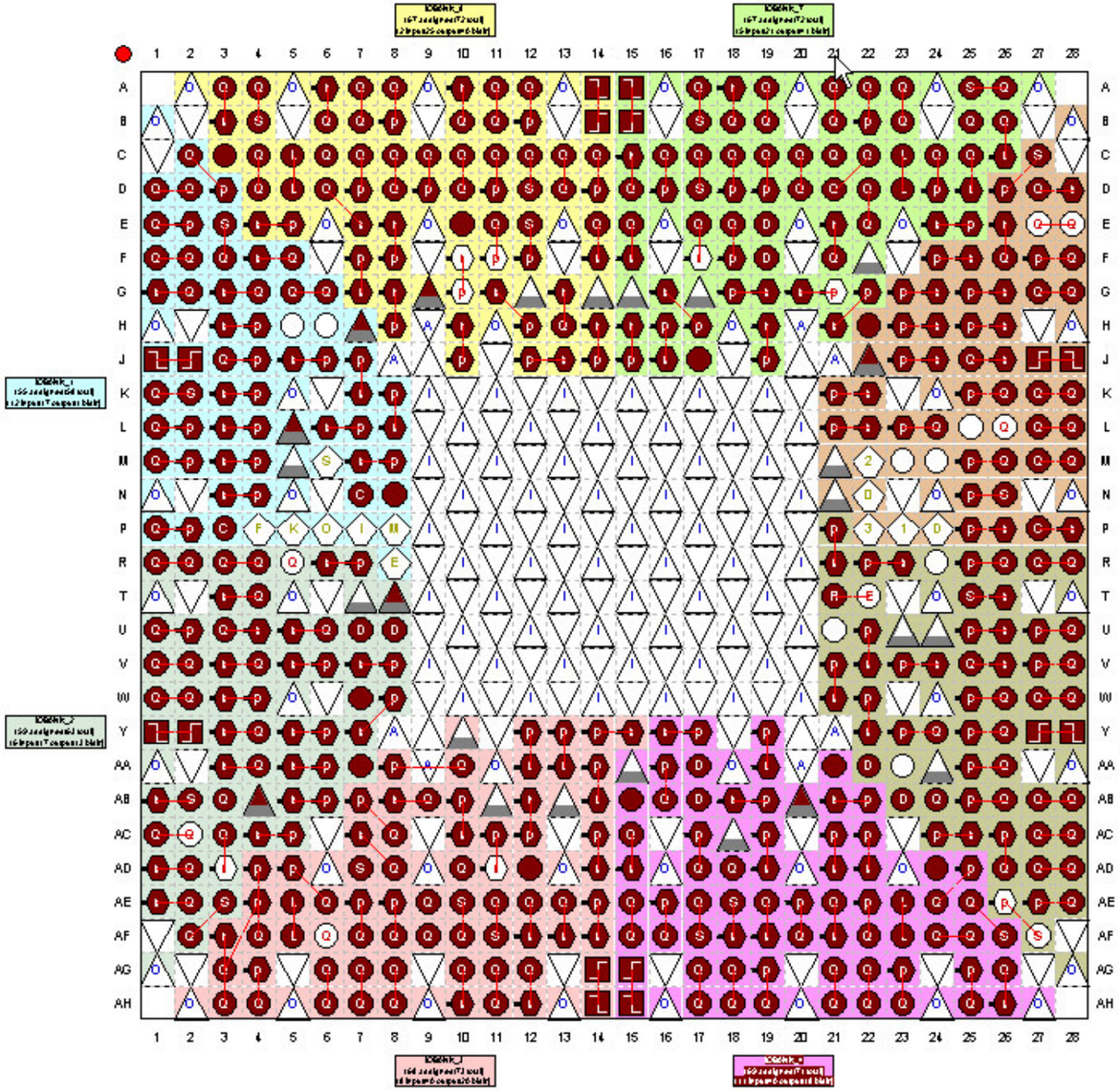
I/O Bank Usage

	I/O Bank	Usage	VCCIO Voltage	VREF Voltage
1	1	55 / 58 (95 %)	2.5V	--
2	2	59 / 63 (94 %)	2.5V	--
3	3	68 / 73 (93 %)	1.8V	0.9V
4	4	69 / 71 (97 %)	1.8V	0.9V
5	5	56 / 65 (86 %)	2.5V	--
6	6	50 / 58 (86 %)	2.5V	--
7	7	67 / 72 (93 %)	1.8V	0.9V
8	8	67 / 72 (93 %)	1.8V	0.9V

BANK 8
VCCIO = 1.8V

BANK 7
VCCIO = 1.8V

Cyclone III - EP3C120F780C7



BANK 1
VCCIO = 2.5V

BANK 6
VCCIO = 2.5V

BANK 2
VCCIO = 2.5V

BANK 5
VCCIO = 2.5V

VCCIO = 1.8V

VCCIO = 1.8V

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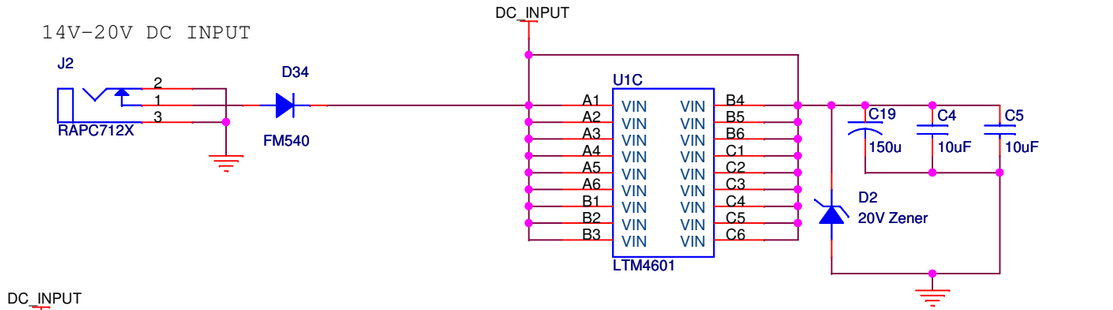
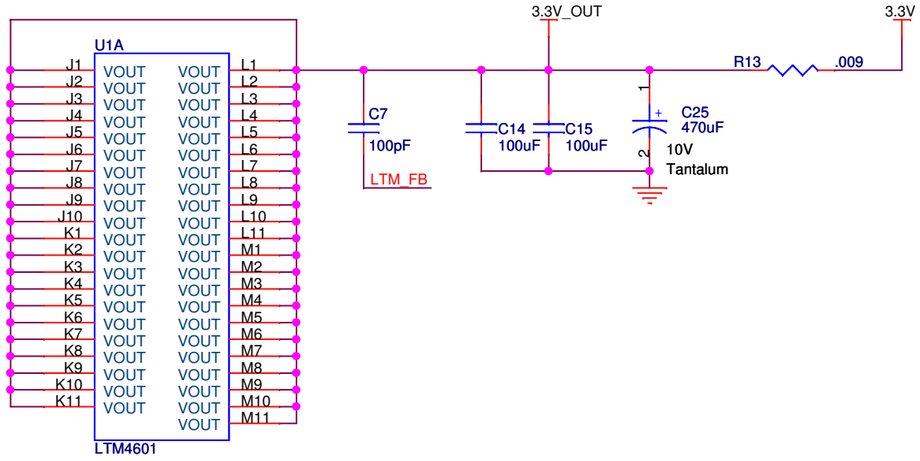
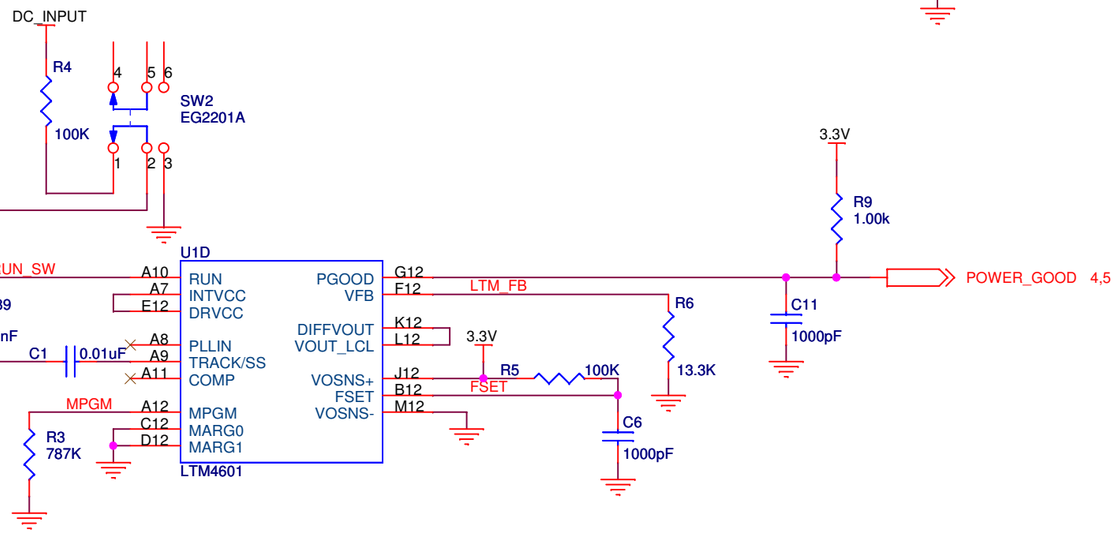
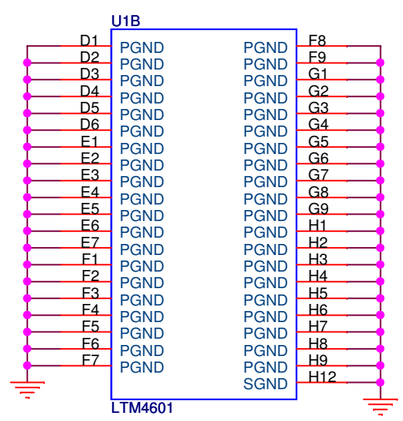
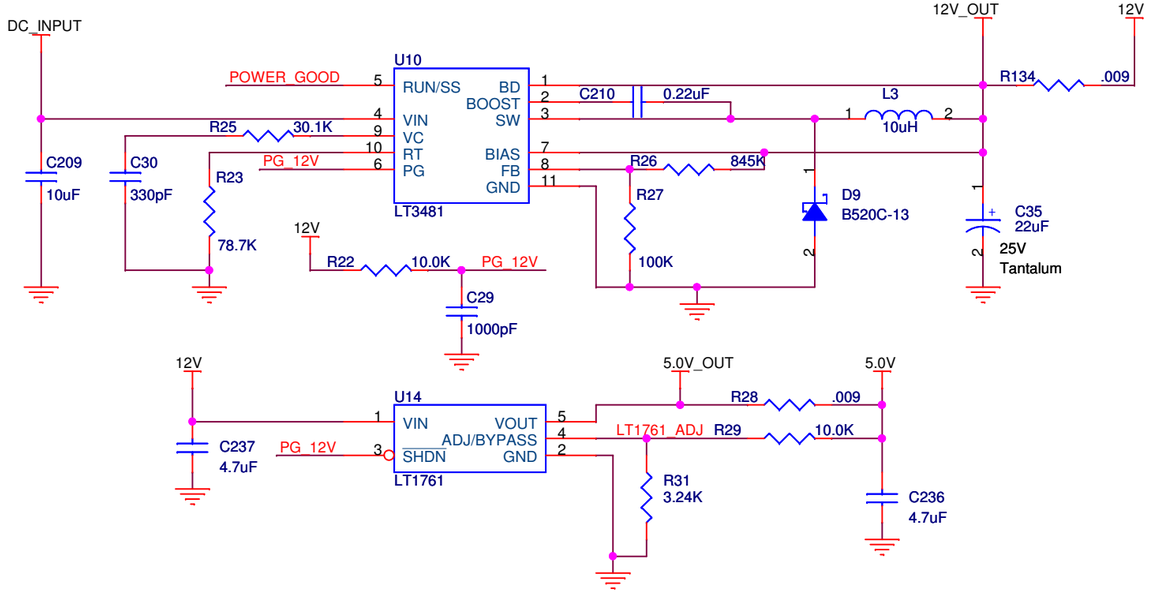
Power 1

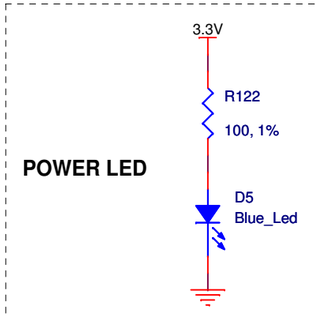












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Power 2

POWER_GOOD → POWER_GOOD 3,5

0.9V VTT (3A Sink/Src)

5.0V, C444 1uF, R53 10.0K, R50 10.0K, VREF_B3_B4, C451 0.1uF

U27 TPS51100DGQ: VIN, VLDOIN, VDDQSNS, VTT, VTTSNS, S3, S5, VTTREF, PGND, GND, GND

1.8V, C445 10uF

VTT_B3_B4: C459 10uF, C470 10uF, C471 10uF, C472 10uF, C473 10uF, C474 10uF

5.0V, C150 1uF, R19 10.0K, R20 10.0K, VREF_B7_B8, C28 0.1uF

U6 TPS51100DGQ: VIN, VLDOIN, VDDQSNS, VTT, VTTSNS, S3, S5, VTTREF, PGND, GND, GND

1.8V, C149 10uF

VTT_B7_B8: C207 10uF, C131 10uF, C130 10uF, C129 10uF, C257 10uF, C128 10uF

3.3V, C484 10uF, POWER_GOOD

U33 LT1963A: IN, NC, OUT, SHDNn, SENSE, GND, GND, GND

2.5V_OUT

- R81 .009 → 2.5V → Other 2.5V (non-FPGA)
- R48 .009 → 2.5V_B1_B2 → CIII BANKS 1 & 2
- R51 .009 → 2.5V_B5_B6 → CIII BANKS 5 & 6
- R80 .009 → 2.5V_VCCA → CIII PLL ANALOG POWER

C486 10uF

3.3V, C51 10uF, POWER_GOOD

U21 LT1963A: IN, NC, OUT, SHDNn, SENSE, GND, GND, GND

1.2V_PLL, R43 .009 → 1.2V_VCCD → CIII PLL DIGITAL POWER

3.3V, POWER_GOOD

U2 LTC3418: RUN/SS, PVIN, SVIN, TRACK, SYNC/MODE, ITH, RT, SW, VFB, VREF, PGOOD, SGND, PGND, GND

C3 10uF, C2 10uF, C93 10uF, C94 10uF

L2 0.2uH: 1.8V_SW → 1.8V_OUT

R15 12.7K, C16 1000pF, R14 10.0K, 1.8V_VFB

C26 100uF, C27 100uF

R32 .009 → 1.8V, R44 .009 → 1.8V_B3_B4, R24 .009 → 1.8V_B7_B8

C9 2.2uF

R16 5.1K, R7 30.1K, C17 2.2nF

3.3V, POWER_GOOD

U29 LTC3418: RUN/SS, PVIN, SVIN, TRACK, SYNC/MODE, ITH, RT, SW, VFB, VREF, PGOOD, SGND, PGND, GND

C69 10uF, C68 10uF, C476 10uF, C475 10uF

L6 0.2uH: 1.2V_OUT

R58 5.1K, C66 1000pF, R59 10.0K, 1.2V_VFB

C419 100uF, C418 100uF

R46 .009 → 1.2V, R49 .009 → 1.2V_INT

C67 2.2uF

R57 5.1K, R68 30.1K, C64 2.2nF

12V, C500 10uF

L8 10uH: +12SW

C498 4.7uF: -12SW

L9 10uH

U38 LT1931: VIN, SW1, GND, SHDN, NFB

40V Schottky D35

C490 DNI

-12V, R240 80.6K, C497 10uF, R241 10.0K, -12FB

R242 2.2K → V5 R92 4.7K → V4 R91 4.7K → V3 R90 22K → V2 R89 4.7K → V1 R88 4.7K → 2.5V

C77 0.1uF, C76 0.1uF, C75 0.1uF, C74 0.1uF, C73 0.1uF

-12V, R93 100, BLACK, RED, J12 HDR2X1

Graphics LCD Backlight Power Header (Hook black wire to pin 1)

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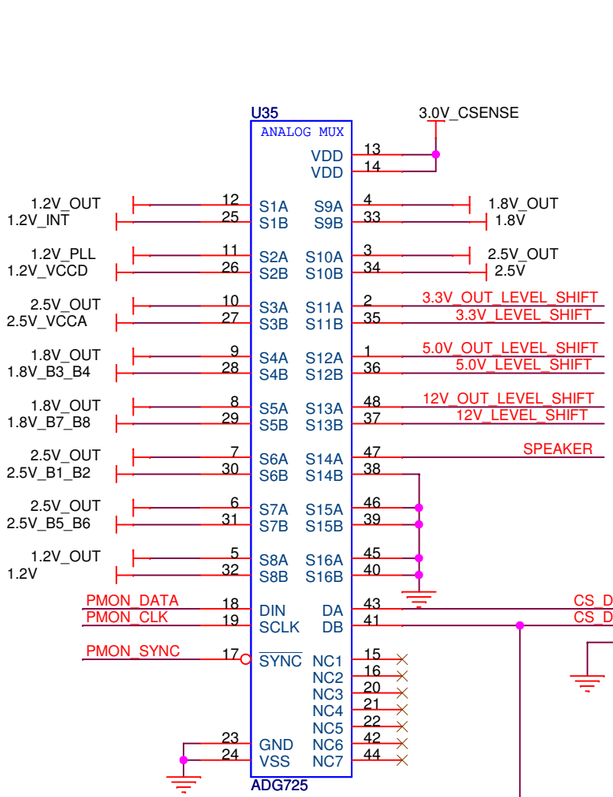
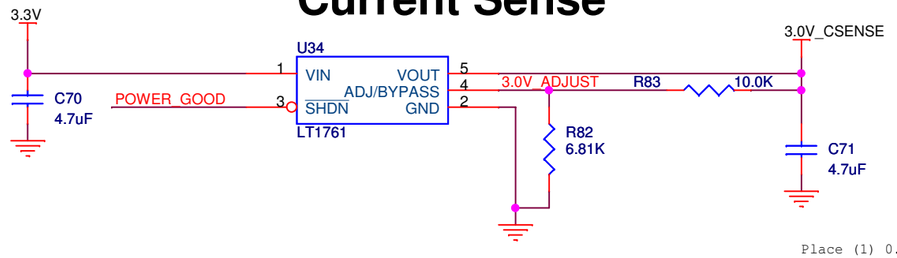
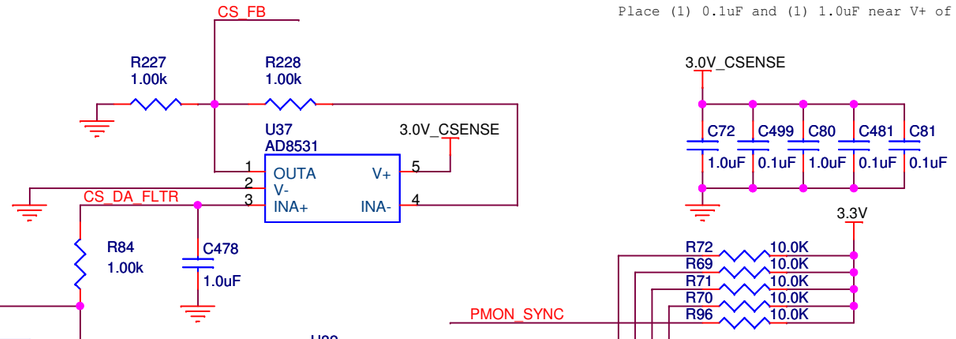
Current Sense





Place (1) 0.1uF near VDD of ADG725.
Place (1) 0.1uF and (1) 1.0uF near V+ of INA271
Place (1) 0.1uF and (1) 1.0uF near V+ of AD7940



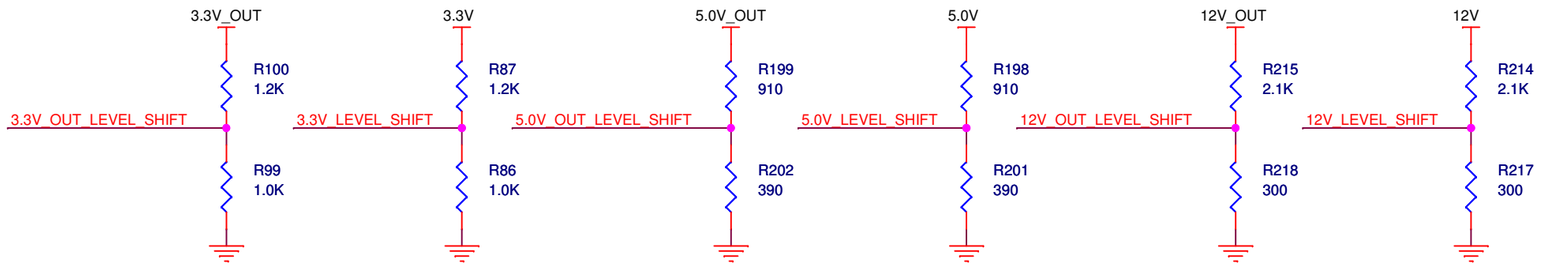
Current Sense A/D

CURRENT SENSE INTERFACE

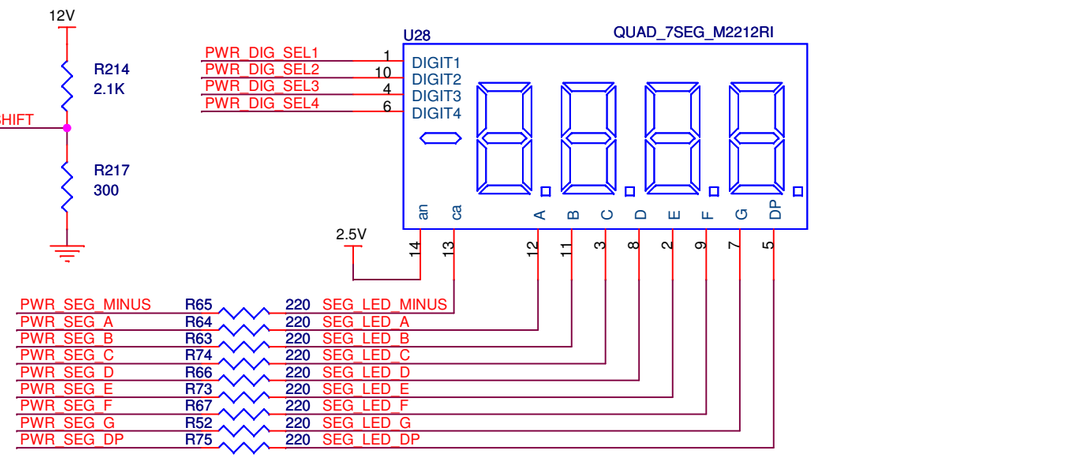
PMON_DATA — PMON_DATA 8
PMON_CLK — PMON_CLK 8
PMON_CSN — PMON_CSN 8
PMON_SYNC — PMON_SYNC 8
PMON_SDI — PMON_SDI 8
SPEAKER — SPEAKER 16

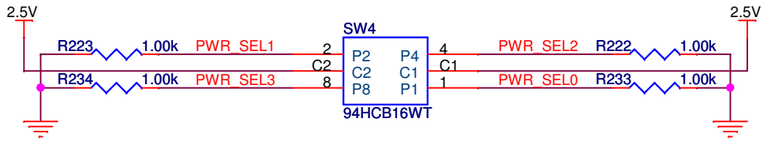
POWER DISPLAY INTERFACE

PWR_DIG_SEL[4:1] — PWR_DIG_SEL[4:1] 8
PWR_SEG_A — PWR_SEG_A 8
PWR_SEG_B — PWR_SEG_B 8
PWR_SEG_C — PWR_SEG_C 8
PWR_SEG_D — PWR_SEG_D 8
PWR_SEG_E — PWR_SEG_E 8
PWR_SEG_F — PWR_SEG_F 8
PWR_SEG_G — PWR_SEG_G 8
PWR_SEG_DP — PWR_SEG_DP 8
PWR_SEG_MINUS — PWR_SEG_MINUS 8
PWR_SEL[3:0] — PWR_SEL[3:0] 8
PG_12V — PG_12V 3
POWER_GOOD — POWER_GOOD 3,4



POWER DISPLAY





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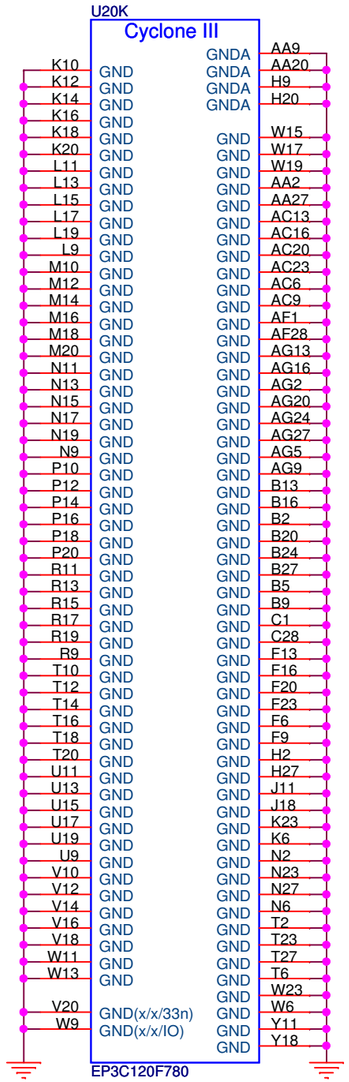
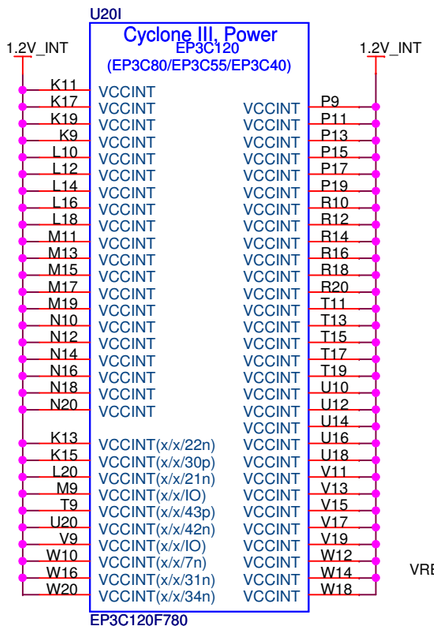
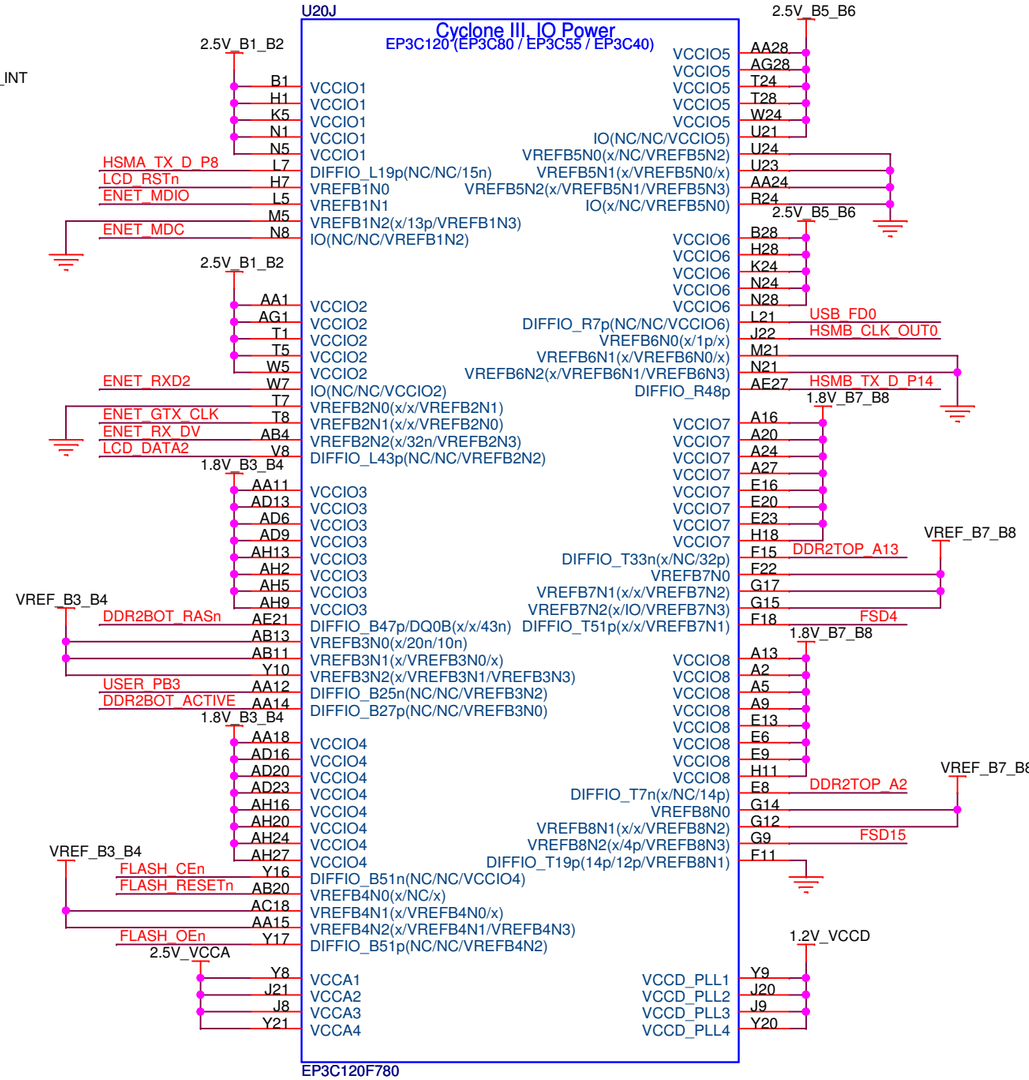
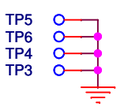
Cyclone III Power

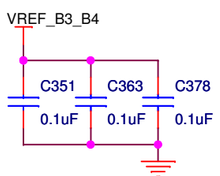


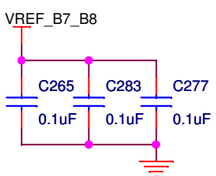






PLACE NEAR CIII





HSMC PORT A

HSMA_TX_D_P[16:0] → HSMA_TX_D_P[16:0] 14,18

HSMC PORT B

HSMB_D[3:0] → HSMB_D[3:0] 14,18

HSMB_TX_D_P[16:0] → HSMB_TX_D_P[16:0] 14,18

HSMB_CLK_OUT0 → HSMB_CLK_OUT0 14

ETHERNET INTERFACE

ENET_RXD[3..0] → ENET_RXD[3..0] 13,18

ENET_MDIO → ENET_MDIO 13

ENET_RX_DV → ENET_RX_DV 13

ENET_GTX_CLK → ENET_GTX_CLK 13

ENET_MDC → ENET_MDC 13

DDR2 INTERFACE

DDR2TOP_A[15:0] → DDR2TOP_A[15:0] 7,9,10,19

DDR2BOT_RASn → DDR2BOT_RASn 9,10

DDR2BOT_ACTIVE → DDR2BOT_ACTIVE 9

SHARED BUS

FSD[31:0] → FSD[31:0] 8,11,19

USB 2.0 INTERFACE

USB_FD[7:0] → USB_FD[7:0] 8,18

OLED DISPLAY INTERFACE

LCD_DATA[7:0] → LCD_DATA[7:0] 16,18

LCD_RSTn → LCD_RSTn 16

FLASH INTERFACE

FLASH_CEn → FLASH_CEn 8,11

FLASH_OEn → FLASH_OEn 8,11

FLASH_RESETn → FLASH_RESETn 8,11

USER I/O's

USER_PB[3:0] → USER_PB[3:0] 16,19

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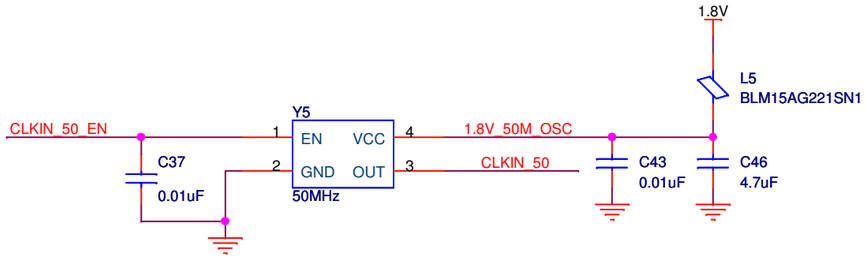
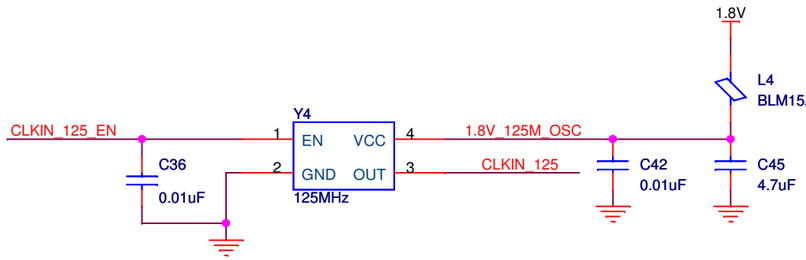
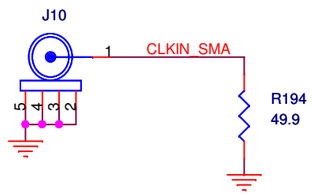
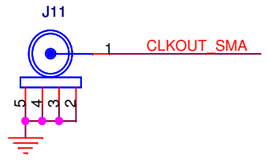
Cyclone III Clocks

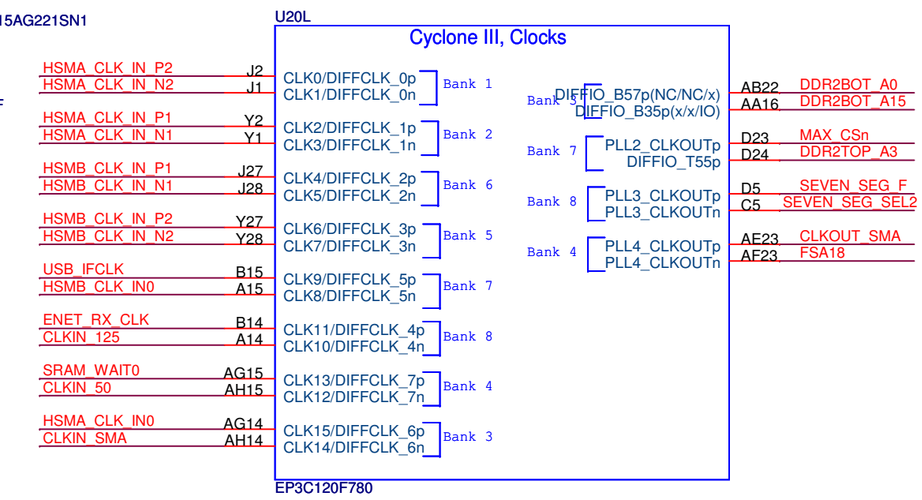


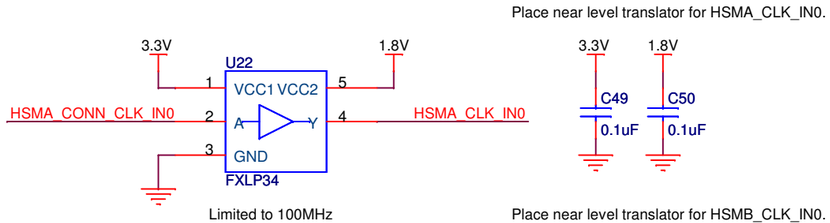


SMA Connector
(external clock source)









MAX_CSn — MAX_CSn 8

HSMC PORT A

HSMA_CLK_IN_P[2:1] — HSMA_CLK_IN_P[2:1] 14,15
HSMA_CLK_IN_N[2:1] — HSMA_CLK_IN_N[2:1] 14,15
HSMA_CONN_CLK_IN0 — HSMA_CONN_CLK_IN0 14

HSMC PORT B

HSMB_CLK_IN_P[2:1] — HSMB_CLK_IN_P[2:1] 14,15
HSMB_CLK_IN_N[2:1] — HSMB_CLK_IN_N[2:1] 14,15
HSMB_CONN_CLK_IN0 — HSMB_CONN_CLK_IN0 14

SHARED BUS

FSA[24:0] — FSA[24:0] 8,11,19

SEVEN-SEG DISPLAY

SEVEN_SEG_SEL[4:1] — SEVEN_SEG_SEL[4:1] 16,19
SEVEN_SEG_F — SEVEN_SEG_F 16

USB 2.0 INTERFACE

USB_IFCLK — USB_IFCLK 8

OSCILLATOR CONTROL

CLKIN_50_EN — CLKIN_50_EN 8
CLKIN_125_EN — CLKIN_125_EN 8

ETHERNET INTERFACE

ENET_RX_CLK — ENET_RX_CLK 13

DDR2 INTERFACE

DDR2BOT_A[15:0] — DDR2BOT_A[15:0] 9,10,19
DDR2TOP_A[15:0] — DDR2TOP_A[15:0] 6,9,10,19

PSRAM INTERFACE

SRAM_WAIT0 — SRAM_WAIT0 11

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MAX II

U7A — MAX II BANK1

FPGA_DATA	D3	IOB1_1	IOB1_25	H3	PMON_DATA
FPGA_DCLK	C2	IOB1_2	IOB1_26	J1	PMON_CLK
FPGA_CONF_DONE	E3	IOB1_3	IOB1_27	H4	PMON_SDI
FPGA_nSTATUS	C3	IOB1_4	IOB1_28	J2	PMON_CSN
FPGA_nCONFIG	E4	IOB1_5	IOB1_29	J4	MAX_ERROR
PWR_SEG_A	D2	IOB1_6	IOB1_30	K1	MAX_LOAD
PWR_SEG_B	E5	IOB1_7	IOB1_31	J3	MAX_FACTORY
PWR_SEG_C	D1	IOB1_8	IOB1_32	K2	MAX_USER
PWR_SEG_D	F3	IOB1_9			
PWR_SEG_E	E2	IOB1_10	IOB1_34	L1	USB_PA5_IF0ADR1
PWR_SEG_F	F4	IOB1_11	IOB1_35	K5	USB_PA6_PKTEND
PWR_SEG_G	E1	IOB1_12	IOB1_36	L2	USB_PA7_SLCSn
PWR_SEG_DP	F5	IOB1_13	IOB1_37	K4	HSMA_JTAG_TDO
PWR_SEG_MINUS	F2	IOB1_14	IOB1_38	M1	MAXGP_JTAG_TCK
PWR_DIG_SEL1	F6	IOB1_15	IOB1_39	K3	USB_TXEn
PWR_DIG_SEL2	F1	IOB1_16	IOB1_40	M2	MAXGP_JTAG_TMS
PWR_DIG_SEL3	G3	IOB1_17	IOB1_41	L5	MAXGP_JTAG_TDO
PWR_DIG_SEL4	G2	IOB1_18	IOB1_42	M3	USB_WEN
PWR_SEL0	G4	IOB1_19	IOB1_43	L4	MAXGP_JTAG_TDI
PWR_SEL1	G1	IOB1_20	IOB1_44	N1	FPGA_JTAG_TDI
PWR_SEL2	G5	IOB1_21	IOB1_45	L3	USB_PA4_IF0ADR0
PWR_SEL3	H2	IOB1_22	IOB1_46	N2	FPGA_JTAG_TDO
			IOB1_47	M4	HSMA_JTAG_TDI
HSMB_JTAG_TDI	H1	IOB1_24	IOB1_48	N3	FPGA_JTAG_TCK
			IOB1_49	P2	FPGA_JTAG_TMS
PMON_SYNC	H5	IOB1/GCLK0	TCK	P3	MAX_JTAG_TCK
MAX_EMB	J5	IOB1/GCLK1	TDI	L6	MAX_JTAG_TDI
			TDO	M5	MAX_JTAG_TDO
			TMS	N4	MAX_JTAG_TMS

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U7B — MAX II BANK2

USB_PHY_FD0	C13	IOB2_50	IOB2_74	E9	USB_FD0
USB_PHY_FD1	B16	IOB2_51	IOB2_75	A9	USB_FD1
USB_PHY_FD2	C12	IOB2_52	IOB2_76	A8	USB_FD2
USB_PHY_FD3	A15	IOB2_53	IOB2_77	B8	USB_FD3
USB_PHY_FD4	D12	IOB2_54	IOB2_78	E8	USB_FD4
USB_PHY_FD5	B14	IOB2_55	IOB2_79	A7	USB_FD5
USB_PHY_FD6	C11	IOB2_56	IOB2_80	D8	USB_FD6
USB_PHY_FD7	B13	IOB2_57	IOB2_81	B7	USB_FD7
USB_PHY_FD8	D11	IOB2_58	IOB2_82	C8	USB_RDn
USB_PHY_FD9	A13	IOB2_59	IOB2_83	A6	USB_WR
USB_PHY_FD10	E11	IOB2_60			
USB_PHY_FD11	B12	IOB2_61	IOB2_85	B6	USB_RXFn
USB_PHY_FD12	C10	IOB2_62	IOB2_86	E7	USB_PWR_ENn
USB_PHY_FD13	A12	IOB2_63	IOB2_87	A5	USB_RSTn
USB_PHY_FD14	D10	IOB2_64	IOB2_88	D7	USB_RSTOUTn
USB_PHY_FD15	B11	IOB2_65	IOB2_89	B5	USB_SI_WU
USB_CMD_DATA	E10	IOB2_66	IOB2_90	C7	USB_PHY_IFCLK
USB_REN	A11	IOB2_67	IOB2_91	A4	USB_PHY_CMD_DATA
			IOB2_92	E6	USB_PHY_REN
USB_EMPTY	B10	IOB2_69	IOB2_93	B4	USB_PHY_WEN
USB_FULL	C9	IOB2_70	IOB2_94	D6	USB_PHY_EMPTY
FACTORY_CONFIGn	A10	IOB2_71	IOB2_95	C4	USB_PHY_FULL
LCD_BS1	D9	IOB2_72	IOB2_96	C6	USB_RESETn
HSMB_JTAG_TDO	B9	IOB2_73	IOB2_97	B3	USB_CLKOUT
			IOB2_98	C5	USB_WAKEUP
			IOB2_99	A2	USB_PA0_INT0n
			IOB2_100	D5	USB_PA1_INT1n
			IOB2_101	B1	USB_PA2_SLOE
			IOB2_102	D4	USB_PA3_WU2

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U7C — MAX II BANK3

MAX_RESERVE1	P14	IOB3_103	IOB3_127	J16	FPGA_BYPASS
MWATTS_MAMPS	N13	IOB3_104	IOB3_128	J13	HSMA_BYPASS
VOLTS_WATTS	P15	IOB3_105	IOB3_129	H16	HSMB_BYPASS
MAX_RESERVE0	M14	IOB3_106	IOB3_130	H13	PGM0
MAX_DIP0	N14	IOB3_107	IOB3_131	H15	PGM1
MAX_DIP1	M13	IOB3_108	IOB3_132	H14	PGM2
MAX_DIP2	N15	IOB3_109	IOB3_133	G16	PGM3
MAX_DIP3	L14	IOB3_110	IOB3_134	G12	
LCD_SERn	N16	IOB3_111	IOB3_135	G15	
	L13	IOB3_112			
FLASH_RESETn	M15	IOB3_113	IOB3_137	F16	SRAM_ACTIVE
FLASH_WEn	L12	IOB3_114	IOB3_138	G13	FLASH_ACTIVE
FLASH_OEn	M16	IOB3_115	IOB3_139	F15	SRAM_CSn
FLASH_RDYBSYn	L11	IOB3_116	IOB3_140	G14	
FLASH_BYTEn	L15	IOB3_117	IOB3_141	E16	JTAG_SEL
FLASH_CEn	K14	IOB3_118	IOB3_142	F11	DEV_SEL
MAX_CSn	L16	IOB3_119	IOB3_143	E15	
MAX_OEn	K13	IOB3_120	IOB3_144	F12	FSD24
MAX_WEn	K15	IOB3_121	IOB3_145	D16	FSD25
	K12	IOB3_122	IOB3_146	F13	FSD26
FSA6	K16	IOB3_123	IOB3_147	D15	FSD27
FSD18	J15	IOB3_125	IOB3_148	F14	FSD28
USB_IFCLK	J14	IOB3_126	IOB3_149	D14	FSD29
			IOB3_150	E12	FSD30
			IOB3_151	C15	FSD31
			IOB3_152	E13	CLKIN_50_EN
			IOB3_153	C14	CLKIN_125_EN
CLKIN_24	J12	IOB3/GLCK2	IOB3_154	E14	
MAX2_CLK	H12	IOB3/GLCK3	IOB3_155	D13	

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U7D — MAX II BANK4

FSD0	P4	IOB4_156	IOB4_180	N9	FSA0
FSD1	R1	IOB4_157	IOB4_181	T8	FSA1
FSD2	P5	IOB4_158	IOB4_182	T9	FSA2
FSD3	T2	IOB4_159	IOB4_183	R9	FSA3
FSD4	N5	IOB4_160	IOB4_184	P9	FSA4
FSD5	R3	IOB4_161	IOB4_185	T10	FSA5
FSD6	P6	IOB4_162			
FSD7	R4	IOB4_163	IOB4_187	R10	FSA7
FSD8	N6	IOB4_164	IOB4_188	M10	FSA8
FSD9	T4	IOB4_165	IOB4_189	T11	FSA9
FSD10	M6	IOB4_166	IOB4_190	N10	FSA10
FSD11	R5	IOB4_167	IOB4_191	R11	FSA11
FSD12	P7	IOB4_168	IOB4_192	P10	FSA12
FSD13	T5	IOB4_169	IOB4_193	T12	FSA13
FSD14	N7	IOB4_170	IOB4_194	M11	FSA14
FSD15	R6	IOB4_171	IOB4_195	R12	FSA15
FSD16	M7	IOB4_172	IOB4_196	N11	FSA16
FSD17	T6	IOB4_173	IOB4_197	T13	FSA17
			IOB4_198	P11	FSA18
FSD19	R7	IOB4_175	IOB4_199	R13	FSA19
FSD20	P8	IOB4_176	IOB4_200	M12	FSA20
FSD21	T7	IOB4_177	IOB4_201	R14	FSA21
FSD22	N8	IOB4_178	IOB4_202	N12	FSA22
FSD23	R8	IOB4_179	IOB4_203	T15	FSA23
			IOB4_204	P12	FSA24
CPU_RESETn	M9	IOB4/DEV_CLRn	IOB4_205	R16	RESET_CONFIGn
MAX_EN	M8	IOB4/DEV_OE	IOB4_206	P13	

EPM2210_F256FBGA

USB Blaster Clock

1.8V — L7 BLM15AG221SN1 — Y3 24MHz (EN, GND, VCC, OUT) — 1.8V_24M_OSC — CLKIN_24

C38 0.01uF; C34 0.01uF; C239 4.7uF

FPGA JTAG INTERFACE

FPGA_JTAG_TCK	FPGA_JTAG_TCK 14,17
FPGA_JTAG_TMS	FPGA_JTAG_TMS 14,17
FPGA_JTAG_TDO	FPGA_JTAG_TDO 17
FPGA_JTAG_TDI	FPGA_JTAG_TDI 17

MAXII JTAG INTERFACE

MAX_JTAG_TCK	MAX_JTAG_TCK 17
MAX_JTAG_TMS	MAX_JTAG_TMS 17
MAX_JTAG_TDO	MAX_JTAG_TDO 17
MAX_JTAG_TDI	MAX_JTAG_TDI 17

MAXII GPIO JTAG

MAXGP_JTAG_TCK	MAXGP_JTAG_TCK 17
MAXGP_JTAG_TMS	MAXGP_JTAG_TMS 17
MAXGP_JTAG_TDO	MAXGP_JTAG_TDO 17
MAXGP_JTAG_TDI	MAXGP_JTAG_TDI 17
HSMA_JTAG_TDO	HSMA_JTAG_TDO 14
HSMA_JTAG_TDI	HSMA_JTAG_TDI 14
HSMB_JTAG_TDO	HSMB_JTAG_TDO 14
HSMB_JTAG_TDI	HSMB_JTAG_TDI 14

FSM BUS

FSD[31:0]	FSD[31:0] 6,11,19
FSA[24:0]	FSA[24:0] 7,11,19

CONFIGURATION INTERFACE

MAX_ERROR	MAX_ERROR 16
MAX_LOAD	MAX_LOAD 16
MAX_FACTORY	MAX_FACTORY 16
MAX_USER	MAX_USER 16
MAX_EMB	MAX_EMB 16
RESET_CONFIGn	RESET_CONFIGn 16
CPU_RESETn	CPU_RESETn 16,18
FACTORY_CONFIGn	FACTORY_CONFIGn 16
PGM[3:0]	PGM[3:0] 16
FPGA_DATA	FPGA_DATA 17
FPGA_DCLK	FPGA_DCLK 17
FPGA_CONF_DONE	FPGA_CONF_DONE 16,17
FPGA_nSTATUS	FPGA_nSTATUS 17
FPGA_nCONFIG	FPGA_nCONFIG 17

U7E — MAX II Power

H7	GNDINT	VCCINT	H8
H9	GNDINT	VCCINT	H10
J8	GNDINT	VCCINT	J7
J10	GNDINT	VCCINT	J9
G6	GNDINT	VCCINT	K6
F7	GNDINT	VCCINT	L7
K11	GNDINT	VCCINT	G11
L10	GNDINT	VCCINT	F10
A1	GNDIO	VCCIO1	C1
A16	GNDIO	VCCIO1	H6
B2	GNDIO	VCCIO1	J6
B15	GNDIO	VCCIO1	P1
G7	GNDIO		
G8	GNDIO	VCCIO2	A3
G9	GNDIO	VCCIO2	A14
G10	GNDIO	VCCIO2	F8
K7	GNDIO	VCCIO2	F9
K8	GNDIO		
K9	GNDIO	VCCIO3	C16
K10	GNDIO	VCCIO3	H11
R2	GNDIO	VCCIO3	J11
R15	GNDIO	VCCIO3	P16
T1	GNDIO		
T16	GNDIO	VCCIO4	L8
		VCCIO4	L9
		VCCIO4	T3
		VCCIO4	T14

1.8V; 2.5V

EPM2210_F256FBGA

USB TO C3 INTERFACE

USB_FD[7:0]	USB_FD[7:0] 6,18
USB_IFCLK	USB_IFCLK 7
USB_CMD_DATA	USB_CMD_DATA 18
USB_REN	USB_REN 18
USB_WEN	USB_WEN 18
USB_EMPTY	USB_EMPTY 18
USB_FULL	USB_FULL 18

FLASH INTERFACE

FLASH_RESETn	FLASH_RESETn 6,11
FLASH_WEn	FLASH_WEn 11,19
FLASH_OEn	FLASH_OEn 6,11
FLASH_RDYBSYn	FLASH_RDYBSYn 11,19
FLASH_BYTEn	FLASH_BYTEn 11
FLASH_CEn	FLASH_CEn 6,11
MAX_CSn	MAX_CSn 7
MAX_OEn	MAX_OEn 19
MAX_WEn	MAX_WEn 19
MAX2_CLK	MAX2_CLK 19

JTAG CONTROL

FPGA_BYPASS	FPGA_BYPASS 16
HSMA_BYPASS	HSMA_BYPASS 16
HSMB_BYPASS	HSMB_BYPASS 16
MAX_EN	MAX_EN 16
JTAG_SEL	JTAG_SEL 17
DEV_SEL	DEV_SEL 17

MAX II DIPSWITCH

MWATTS_MAMPS	MWATTS_MAMPS 16
VOLTS_WATTS	VOLTS_WATTS 16
MAX_RESERVE0	MAX_RESERVE0 16
MAX_RESERVE1	MAX_RESERVE1 16
MAX_DIP[3:0]	MAX_DIP[3:0] 16

C3 OSCILLATOR CONTROL

CLKIN_50_EN	CLKIN_50_EN 7
CLKIN_125_EN	CLKIN_125_EN 7

MEMORY ACTIVITY LEDs

SRAM_ACTIVE	SRAM_ACTIVE 11
FLASH_ACTIVE	FLASH_ACTIVE 11
SRAM_CSn	SRAM_CSn 11,19

LCD INTERFACE CONTROL

LCD_SERn	LCD_SERn 16
LCD_BS1	LCD_BS1 16

Place near MAX II

2.5V: C147 C157 C108 C179 C107 C126 C109 C127 (0.1uF)

1.8V: C211 C144 C146 C145 C137 C178 C125 C148 C212 C177 C213 C156 (0.1uF)

USB 2.0 INTERFACE

USB_PHY_FD[15..0]	USB_PHY_FD[15..0] 12
USB_RDn	USB_RDn 12
USB_WR	USB_WR 12
USB_TXEn	USB_TXEn 12
USB_RXFn	USB_RXFn 12
USB_PWR_ENn	USB_PWR_ENn 12
USB_RSTn	USB_RSTn 12
USB_RSTOUTn	USB_RSTOUTn 12
USB_SI_WU	USB_SI_WU 12
USB_PHY_IFCLK	USB_PHY_IFCLK 12
USB_PHY_CMD_DATA	USB_PHY_CMD_DATA 12
USB_PHY_REN	USB_PHY_REN 12
USB_PHY_WEN	USB_PHY_WEN 12
USB_PHY_EMPTY	USB_PHY_EMPTY 12
USB_PHY_FULL	USB_PHY_FULL 12
USB_RESETn	USB_RESETn 12
USB_WAKEUP	USB_WAKEUP 12
USB_CLKOUT	USB_CLKOUT 12
USB_PA0_INT0n	USB_PA0_INT0n 12
USB_PA1_INT1n	USB_PA1_INT1n 12
USB_PA2_SLOE	USB_PA2_SLOE 12
USB_PA3_WU2	USB_PA3_WU2 12
USB_PA4_IF0ADR0	USB_PA4_IF0ADR0 12
USB_PA5_IF0ADR1	USB_PA5_IF0ADR1 12
USB_PA6_PKTEND	USB_PA6_PKTEND 12
USB_PA7_SLCSn	USB_PA7_SLCSn 12

POWER DISPLAY

PWR_DIG_SEL[4:1]	PWR_DIG_SEL[4:1] 5
PWR_SEG_A	PWR_SEG_A 5
PWR_SEG_B	PWR_SEG_B 5
PWR_SEG_C	PWR_SEG_C 5
PWR_SEG_D	PWR_SEG_D 5
PWR_SEG_E	PWR_SEG_E 5
PWR_SEG_F	PWR_SEG_F 5
PWR_SEG_G	PWR_SEG_G 5
PWR_SEG_DP	PWR_SEG_DP 5
PWR_SEG_MINUS	PWR_SEG_MINUS 5
PWR_SEL[3:0]	PWR_SEL[3:0] 5

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone III Development Kit Host Board

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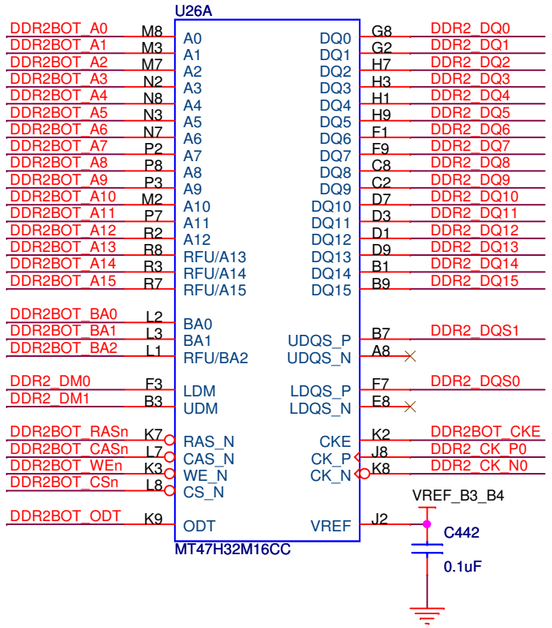
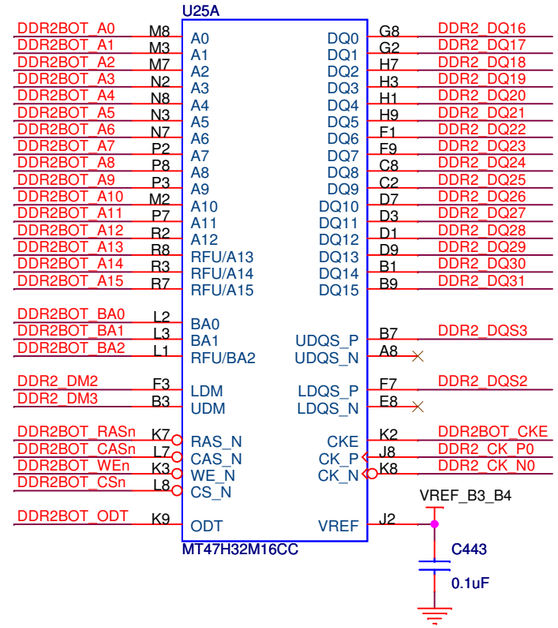
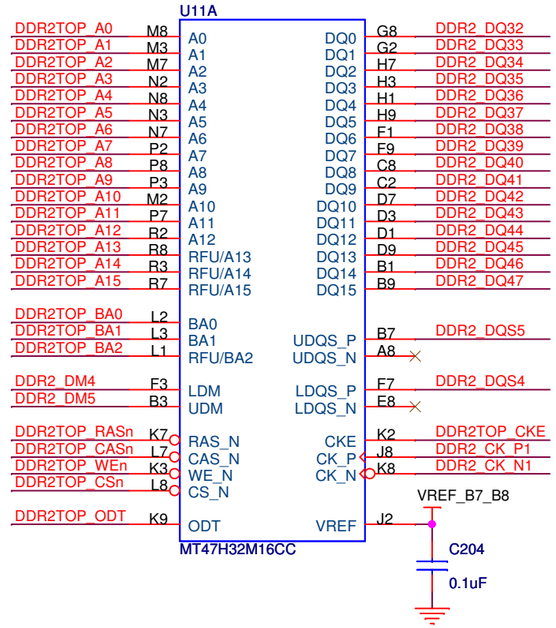
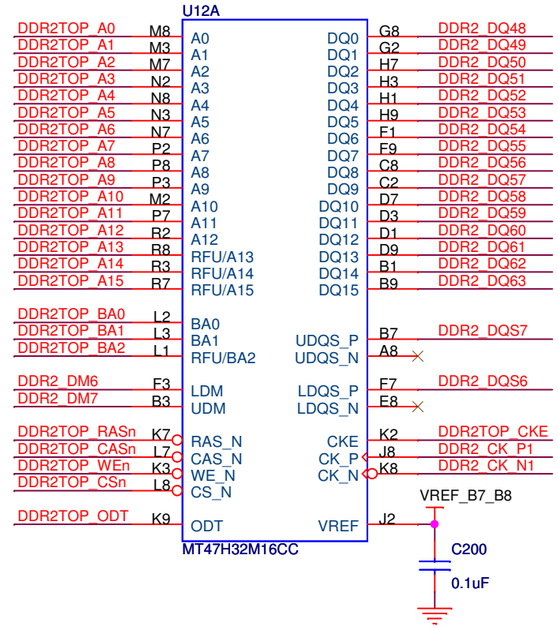
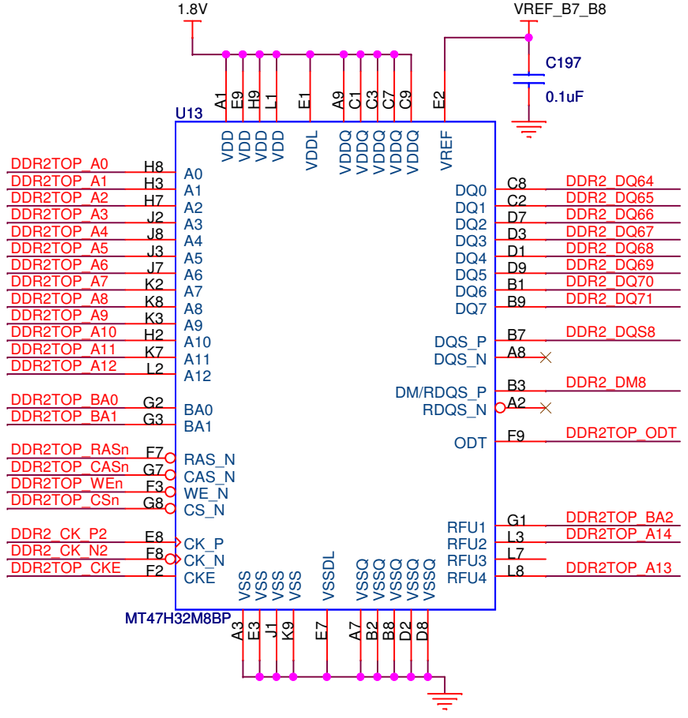
DDR2 SDRAM (x72)

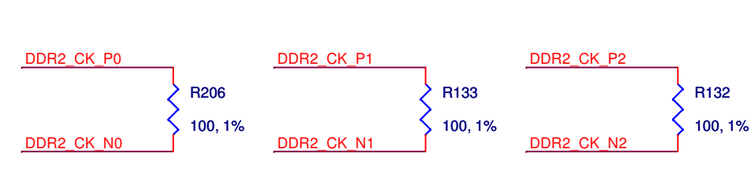




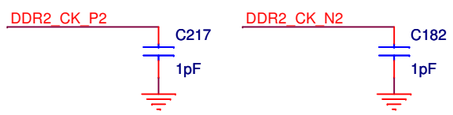


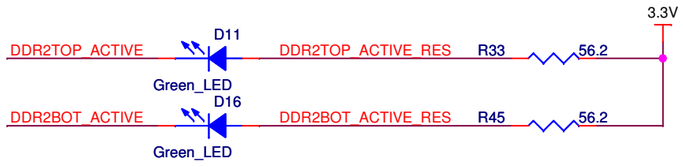






PROVIDES CLOCK SIGNAL LOAD
SIMILAR TO OTHER DDR2 CLK SIGNALS.





DDR2_DQ[71:0] DDR2_DQ[71:0] 10,19
DDR2_DQS[8:0] DDR2_DQS[8:0] 10,19
DDR2_DM[8:0] DDR2_DM[8:0] 10,19
DDR2BOT_A[15:0] DDR2BOT_A[15:0] 7,10,19
DDR2BOT_BA[2:0] DDR2BOT_BA[2:0] 10,19
DDR2TOP_A[15:0] DDR2TOP_A[15:0] 6,7,10,19
DDR2TOP_BA[2:0] DDR2TOP_BA[2:0] 10,19
DDR2BOT_RASn DDR2BOT_RASn 6,10
DDR2BOT_CASn DDR2BOT_CASn 10,19
DDR2BOT_WEn DDR2BOT_WEn 10,19
DDR2BOT_CSn DDR2BOT_CSn 10,19
DDR2BOT_ODT DDR2BOT_ODT 10,19
DDR2BOT_CKE DDR2BOT_CKE 10,19
DDR2TOP_RASn DDR2TOP_RASn 10,19
DDR2TOP_CASn DDR2TOP_CASn 10,19
DDR2TOP_WEn DDR2TOP_WEn 10,19
DDR2TOP_CSn DDR2TOP_CSn 10,19
DDR2TOP_ODT DDR2TOP_ODT 10,19
DDR2TOP_CKE DDR2TOP_CKE 10,19
DDR2_CK_P[2:0] DDR2_CK_P[2:0] 19
DDR2_CK_N[2:0] DDR2_CK_N[2:0] 19
DDR2TOP_ACTIVE DDR2TOP_ACTIVE 19
DDR2BOT_ACTIVE DDR2BOT_ACTIVE 6

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DDR2 SDRAM POWER & TERM

DDR2_DQ[71:0] 9,19
DDR2_DQS[8:0] 9,19
DDR2_DM[8:0] 9,19
DDR2BOT_A[15:0] 7,9,19
DDR2BOT_BA[2:0] 9,19
DDR2TOP_A[15:0] 6,7,9,19
DDR2TOP_BA[2:0] 9,19
DDR2BOT_RASn 6,9
DDR2BOT_CASn 9,19
DDR2BOT_WEn 9,19
DDR2BOT_CSn 9,19
DDR2BOT_ODT 9,19
DDR2BOT_CKE 9,19
DDR2TOP_RASn 9,19
DDR2TOP_CASn 9,19
DDR2TOP_WEn 9,19
DDR2TOP_CSn 9,19
DDR2TOP_ODT 9,19
DDR2TOP_CKE 9,19

1.8V

U26B

A1	VDD	NC2	VSS	A3
E1	VDD	NC1	VSS	E3
J9	VDD		VSS	J3
M9	VDD		VSS	N1
R1	VDD		VSS	P9
J1	VDDL		VSSDL	J7
A9	VDDQ		VSSQ	A7
C1	VDDQ		VSSQ	B2
C3	VDDQ		VSSQ	B8
C7	VDDQ		VSSQ	D2
C9	VDDQ		VSSQ	D8
E9	VDDQ		VSSQ	E7
G1	VDDQ		VSSQ	F2
G3	VDDQ		VSSQ	F8
G7	VDDQ		VSSQ	H2
G9	VDDQ		VSSQ	H8

MT47H32M16CC

U25B

A1	VDD	NC2	VSS	A3
E1	VDD	NC1	VSS	E3
J9	VDD		VSS	J3
M9	VDD		VSS	N1
R1	VDD		VSS	P9
J1	VDDL		VSSDL	J7
A9	VDDQ		VSSQ	A7
C1	VDDQ		VSSQ	B2
C3	VDDQ		VSSQ	B8
C7	VDDQ		VSSQ	D2
C9	VDDQ		VSSQ	D8
E9	VDDQ		VSSQ	E7
G1	VDDQ		VSSQ	F2
G3	VDDQ		VSSQ	F8
G7	VDDQ		VSSQ	H2
G9	VDDQ		VSSQ	H8

MT47H32M16CC

U11B

A1	VDD	NC2	VSS	A3
E1	VDD	NC1	VSS	E3
J9	VDD		VSS	J3
M9	VDD		VSS	N1
R1	VDD		VSS	P9
J1	VDDL		VSSDL	J7
A9	VDDQ		VSSQ	A7
C1	VDDQ		VSSQ	B2
C3	VDDQ		VSSQ	B8
C7	VDDQ		VSSQ	D2
C9	VDDQ		VSSQ	D8
E9	VDDQ		VSSQ	E7
G1	VDDQ		VSSQ	F2
G3	VDDQ		VSSQ	F8
G7	VDDQ		VSSQ	H2
G9	VDDQ		VSSQ	H8

MT47H32M16CC

U12B

A1	VDD	NC2	VSS	A3
E1	VDD	NC1	VSS	E3
J9	VDD		VSS	J3
M9	VDD		VSS	N1
R1	VDD		VSS	P9
J1	VDDL		VSSDL	J7
A9	VDDQ		VSSQ	A7
C1	VDDQ		VSSQ	B2
C3	VDDQ		VSSQ	B8
C7	VDDQ		VSSQ	D2
C9	VDDQ		VSSQ	D8
E9	VDDQ		VSSQ	E7
G1	VDDQ		VSSQ	F2
G3	VDDQ		VSSQ	F8
G7	VDDQ		VSSQ	H2
G9	VDDQ		VSSQ	H8

MT47H32M16CC

PLACE CAPS NEAR U22

1.8V

C198	C216	C226	C158	C227	C228	C229	C218	C199	C183
0.1uF	0.1uF	0.1uF	0.1uF	4.7nF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

PLACE CAPS NEAR U18

1.8V

C396	C397	C427	C411	C441	C426	C425	C410	C405	C395	C398	C406	C412	C456	C455	C454
0.1uF	0.1uF	0.01uF	0.1uF	4.7nF	0.1uF	0.1uF	0.01uF	0.1uF	0.1uF	0.01uF	4.7nF	0.1uF	0.1uF	0.1uF	0.1uF

PLACE CAPS NEAR U19

1.8V

C429	C414	C400	C457	C458	C428	C413	C407	C399	C402	C408	C415	C430	C431	C449	C401
0.1uF	0.1uF	0.01uF	0.1uF	4.7nF	0.1uF	0.1uF	0.01uF	0.1uF	0.1uF	0.01uF	4.7nF	0.1uF	0.1uF	0.1uF	0.1uF

PLACE CAPS NEAR U20

1.8V

C223	C234	C246	C160	C186	C245	C222	C233	C244	C187	C206	C224	C235	C248	C205	C247
0.1uF	0.1uF	0.01uF	0.1uF	4.7nF	0.1uF	0.1uF	0.01uF	0.1uF	0.1uF	0.01uF	4.7nF	0.1uF	0.1uF	0.1uF	0.1uF

PLACE CAPS NEAR U21

1.8V

C241	C240	C230	C219	C201	C184	C159	C220	C231	C242	C185	C202	C243	C203	C232	C221
0.1uF	0.1uF	0.01uF	0.1uF	4.7nF	0.1uF	0.1uF	0.01uF	0.1uF	0.1uF	0.01uF	4.7nF	0.1uF	0.1uF	0.1uF	0.1uF

PLACE CAPS NEAR U18, U19, U20, U21, U22

VTT_B3_B4 VTT_B7_B8

CN18 0.1uf x 4
CN15 0.1uf x 4
CN16 0.1uf x 4
CN17 0.1uf x 4
CN13 0.1uf x 4
CN14 0.1uf x 4
CN11 0.1uf x 4
CN12 0.1uf x 4
CN19 0.1uf x 4

CN2 0.1uf x 4
CN8 0.1uf x 4
CN6 0.1uf x 4
CN7 0.1uf x 4
CN5 0.1uf x 4
CN10 0.1uf x 4
CN9 0.1uf x 4
CN4 0.1uf x 4
CN3 0.1uf x 4
CN1 0.1uf x 4

VTT_B7_B8

DDR2TOP_BA0	RN4D	4	13 56
DDR2TOP_BA1	RN4G	7	10 56
DDR2TOP_BA2	RN4E	5	12 56
	RN9D	4	13 56
	RN8F	6	11 56
	RN8G	7	10 56
	RN9B	2	15 56
	RN9A	1	16 56

VTT_B3_B4

DDR2_DQ0	RN14A	1	16 56
DDR2_DQ1	RN15F	6	11 56
DDR2_DQ2	RN15H	8	9 56
DDR2_DQ3	RN15G	7	10 56
DDR2_DQ4	RN14D	4	13 56
DDR2_DQ5	RN14B	2	15 56
DDR2_DQ6	RN14E	5	12 56
DDR2_DQ7	RN14C	3	14 56
DDR2_DQ8	RN13F	6	11 56
DDR2_DQ9	RN13C	3	14 56
DDR2_DQ10	RN13E	5	12 56
DDR2_DQ11	RN14G	7	10 56
DDR2_DQ12	RN14F	6	11 56
DDR2_DQ13	RN13G	7	10 56
DDR2_DQ14	RN15E	5	12 56
DDR2_DQ15	RN13H	8	9 56
DDR2_DQ16	RN20H	8	9 56
DDR2_DQ17	RN20C	3	14 56
DDR2_DQ18	RN20G	7	10 56
DDR2_DQ19	RN20D	4	13 56
DDR2_DQ20	RN21H	8	9 56
DDR2_DQ21	RN19D	4	13 56
DDR2_DQ22	RN20A	1	16 56
DDR2_DQ23	RN19A	1	16 56
DDR2_DQ24	RN18A	1	16 56
DDR2_DQ25	RN19C	3	14 56
DDR2_DQ26	RN19G	7	10 56
DDR2_DQ27	RN19F	6	11 56
DDR2_DQ28	RN20F	6	11 56
DDR2_DQ29	RN18C	3	14 56
DDR2_DQ30	RN20E	5	12 56
DDR2_DQ31	RN18B	2	15 56
DDR2_DQS0	RN14H	8	9 56
DDR2_DQS1	RN13D	4	13 56
DDR2_DQS2	RN19B	2	15 56
DDR2_DQS3	RN19H	8	9 56
DDR2_DM0	RN13B	2	15 56
DDR2_DM1	RN13A	1	16 56
DDR2_DM2	RN20B	2	15 56
DDR2_DM3	RN19E	5	12 56
V12 DDR2BOT_A0	RN16G	7	10 56
V9 DDR2BOT_A1	RN17B	2	15 56
V10 DDR2BOT_A2	RN16H	8	9 56
V14 DDR2BOT_A3	RN17C	3	14 56
V20 DDR2BOT_A4	RN16F	6	11 56
V16 DDR2BOT_A5	RN17D	4	13 56
V18 DDR2BOT_A6	RN16E	5	12 56
V15 DDR2BOT_A7	RN17E	5	12 56
V21 DDR2BOT_A8	RN16D	4	13 56
V17 DDR2BOT_A9	RN17F	6	11 56
V7 DDR2BOT_A10	RN17A	1	16 56
V19 DDR2BOT_A11	RN16C	3	14 56
V22 DDR2BOT_A12	RN17G	7	10 56
V25 DDR2BOT_A13	RN16B	2	15 56
V23 DDR2BOT_A14	RN17H	8	9 56
V24 DDR2BOT_A15	RN16A	1	16 56
V6 DDR2BOT_BA0	RN18G	7	10 56
V8 DDR2BOT_BA1	RN18H	8	9 56
V5 DDR2BOT_BA2	RN18F	6	11 56
V3 DDR2BOT_RASn	RN15D	4	13 56
V1 DDR2BOT_CASn	RN15B	2	15 56
V2 DDR2BOT_WEn	RN18E	5	12 56
V13 DDR2BOT_CSn	RN15A	1	16 56
V4 DDR2BOT_ODT	RN15C	3	14 56
V1 DDR2BOT_CKE	RN18D	4	13 56
	RN21B	2	15 56
	RN21C	3	14 56
	RN21D	4	13 56
	RN21E	5	12 56
	RN21F	6	11 56
	RN21G	7	10 56
	RN21A	1	16 56

VTT_B7_B8

DDR2_DQ32	RN10D	4	13 56
DDR2_DQ33	RN10A	1	16 56
DDR2_DQ34	RN9H	8	9 56
DDR2_DQ35	RN9E	5	12 56
DDR2_DQ36	RN9F	6	11 56
DDR2_DQ37	RN10C	3	14 56
DDR2_DQ38	RN9G	7	10 56
DDR2_DQ39	RN10F	6	11 56
DDR2_DQ40	RN11B	2	15 56
DDR2_DQ41	RN11F	6	11 56
DDR2_DQ42	RN10H	8	9 56
DDR2_DQ43	RN10G	7	10 56
DDR2_DQ44	RN11G	7	10 56
DDR2_DQ45	RN11A	1	16 56
DDR2_DQ46	RN11H	8	9 56
DDR2_DQ47	RN11D	4	13 56
DDR2_DQ48	RN7E	5	12 56
DDR2_DQ49	RN5C	3	14 56
DDR2_DQ50	RN7A	1	16 56
DDR2_DQ51	RN6C	3	14 56
DDR2_DQ52	RN5A	1	16 56
DDR2_DQ53	RN7G	7	10 56
DDR2_DQ54	RN4F	6	11 56
DDR2_DQ55	RN7H	8	9 56
DDR2_DQ56	RN12B	2	15 56
DDR2_DQ57	RN12G	7	10 56
DDR2_DQ58	RN12C	3	14 56
DDR2_DQ59	RN12F	6	11 56
DDR2_DQ60	R139		56
DDR2_DQ61	R140		56
DDR2_DQ62	RN12H	8	9 56
DDR2_DQ63	RN12A	1	16 56
DDR2_DQ64	RN3H	8	9 56
DDR2_DQ65	RN3C	3	14 56
DDR2_DQ66	RN3F	6	11 56
DDR2_DQ67	RN3E	5	12 56
DDR2_DQ68	RN3A	1	16 56
DDR2_DQ69	RN4B	2	15 56
DDR2_DQ70	RN3B	2	15 56
DDR2_DQ71	RN4A	1	16 56
DDR2TOP_A0	RN8A	1	16 56
DDR2TOP_A1	RN4H	8	9 56
DDR2TOP_A2	RN6E	5	12 56
DDR2TOP_A3	RN5D	4	13 56
DDR2TOP_A4	RN7F	6	11 56
DDR2TOP_A5	RN5E	5	12 56
DDR2TOP_A6	RN7D	4	13 56
DDR2TOP_A7	RN5F	6	11 56
DDR2TOP_A8	RN7B	2	15 56
DDR2TOP_A9	RN5G	7	10 56
DDR2TOP_A10	RN5B	2	15 56
DDR2TOP_A11	RN6H	8	9 56
DDR2TOP_A12	RN5H	8	9 56
DDR2TOP_A13	RN6G	7	10 56
DDR2TOP_A14	RN6B	2	15 56
DDR2TOP_A15	RN6F	6	11 56
DDR2_DQS4	RN10E	5	12 56
DDR2_DQS5	RN11C	3	14 56
DDR2_DQS6	R142		56
DDR2_DQS7	RN12D	4	13 56
DDR2_DQS8	RN3G	7	10 56
DDR2_DM4	RN10B	2	15 56
DDR2_DM5	RN11E	5	12 56
DDR2_DM6	R141		56
DDR2_DM7	RN12E	5	12 56
DDR2_DM8	RN3D	4	13 56
DDR2TOP_RASn	RN6D	4	13 56
DDR2TOP_CASn	RN8B	2	15 56
DDR2TOP_WEn	RN6A	1	16 56
DDR2TOP_CSn	RN8C	3	14 56
DDR2TOP_ODT	RN7C	3	14 56
DDR2TOP_CKE	RN4C	3	14 56

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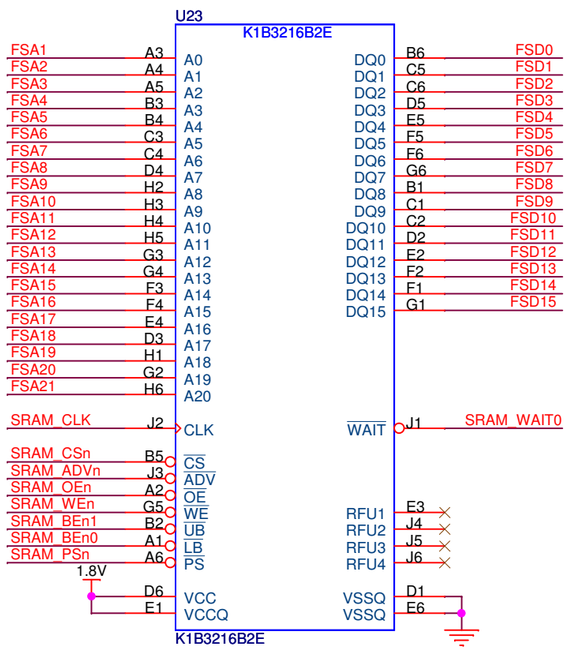
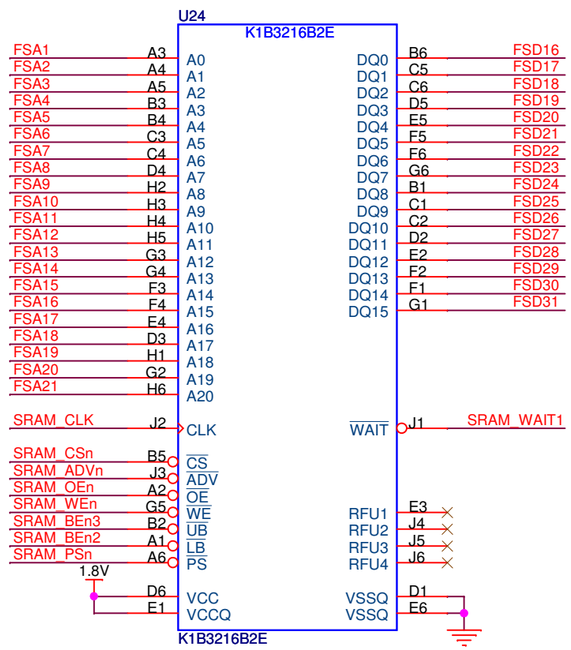
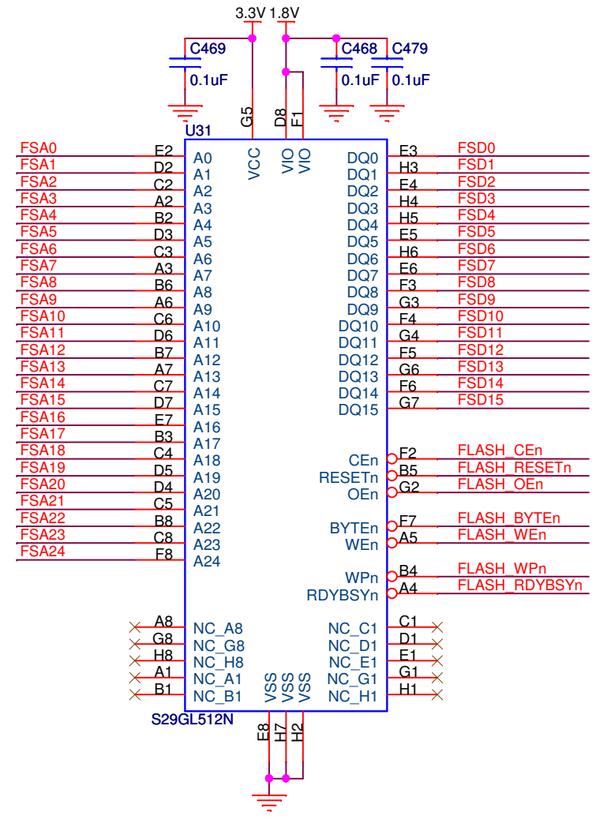
SRAM & Flash

SRAM 32Mb (2M X 16)



SRAM 32Mb (2M X 16)





SHARED BUS

FSD[31:0] — FSD[31:0] 6,8,19

FSA[24:0] — FSA[24:0] 7,8,19

PSRAM INTERFACE

SRAM_CLK — SRAM_CLK 19

SRAM_CSn — SRAM_CSn 8,19

SRAM_ADVn — SRAM_ADVn 19

SRAM_OEn — SRAM_OEn 19

SRAM_WEn — SRAM_WEn 19

SRAM_PSn — SRAM_PSn 19

SRAM_WAIT0 — SRAM_WAIT0 7

SRAM_WAIT1 — SRAM_WAIT1 19

SRAM_BEn[3:0] — SRAM_BEn[3:0] 19

SRAM_ACTIVE — SRAM_ACTIVE 8

FLASH INTERFACE

FLASH_RESETn — FLASH_RESETn 6,8

FLASH_WEn — FLASH_WEn 8,19

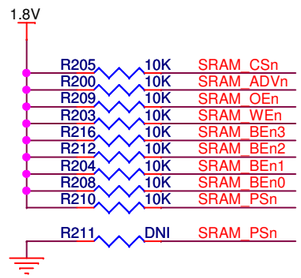
FLASH_OEn — FLASH_OEn 6,8

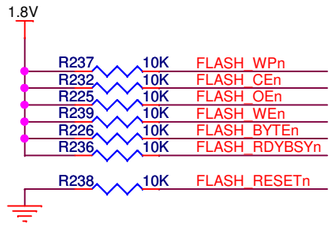
FLASH_RDYBSYn — FLASH_RDYBSYn 8,19

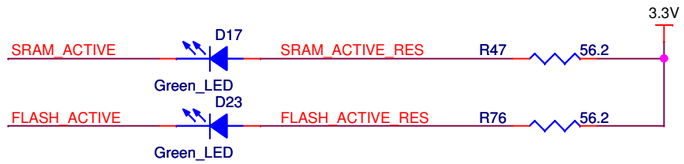
FLASH_CEn — FLASH_CEn 6,8

FLASH_BYTEn — FLASH_BYTEn 8

FLASH_ACTIVE — FLASH_ACTIVE 8







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USB 2.0

USB

U18
SN65220DBV

L1
BLM21PG331SN1

J3
USB CON

C22 10uF
C105 36pF
C96 36pF
Y2 6.000 MHZ

R121 27 USB_DM
R120 27 USB_DP

5V_USB
R124 470
C136 0.1uF
C143 33nF
C175 0.1uF

U8
FT245BL

R128 1.5K USB_RSTOUTn
R127 10.0K USB_RSTn
XTIN
XTOUT

USB_FTDI_DM
USB_FTDI_DP

USB_EECS
USB_EESK
EEDATA

USB_PHY_FD0
USB_PHY_FD1
USB_PHY_FD2
USB_PHY_FD3
USB_PHY_FD4
USB_PHY_FD5
USB_PHY_FD6
USB_PHY_FD7

USB_RDn
USB_WR
USB_TXEn
USB_RXFn

R130 1.00k
USB_SI_WU
USB_PWR_ENn

U17
AT93C46DN-SH-B
(Optional)

R144 2.2K
R143 10.0K
USB_EEDATA

DECOUPLING CAPS

C47 10uF 10V Tantalum
C124 0.1uF
C142 0.1uF

USB 2.0 INTERFACE

USB_PHY_FD[15..0] 8
USB_RDn 8
USB_WR 8
USB_TXEn 8
USB_RXFn 8
USB_PWR_ENn 8
USB_RSTn 8
USB_RSTOUTn 8
USB_SI_WU 8
USB_PHY_IFCLK 8
USB_PHY_CMD_DATA 8
USB_PHY_REN 8
USB_PHY_WEN 8
USB_PHY_EMPTY 8
USB_PHY_FULL 8
USB_RESETn 8
USB_WAKEUP 8
USB_CLKOUT 8
USB_PA0_INT0n 8
USB_PA1_INT1n 8
USB_PA2_SLOE 8
USB_PA3_WU2 8
USB_PA4_IF0ADR0 8
USB_PA5_IF0ADR1 8
USB_PA6_PKTEND 8
USB_PA7_SLCSn 8

U9
CY7C68013A-56LFXC

R17 2.2K USB_SCL
R18 2.2K USB_SDA
R21 2.2K USB_WAKEUP
R111 10.0K USB_RESETn
R110 27 IFCLK
USB_CLKOUT

C97 12pF XTALIN
C106 12pF XTALOUT
Y1 24.000 MHZ

QUSB2CP1

U15
USB_SCL
USB_SDA

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10/100/1000 Ethernet

RGMII Mode

ETHERNET INTERFACE

ENET_TXD[3..0] — ENET_TXD[3..0] 18

ENET_GTX_CLK — ENET_GTX_CLK 6
ENET_TX_EN — ENET_TX_EN 18
ENET_MDC — ENET_MDC 6

ENET_RXD[3..0] — ENET_RXD[3..0] 6,18

ENET_RX_CLK — ENET_RX_CLK 7
ENET_RX_DV — ENET_RX_DV 6
ENET_MDIO — ENET_MDIO 6
ENET_RESETn — ENET_RESETn 18
ENET_LED_LINK1000 — ENET_LED_LINK1000 18

2.5V
R123 4.7K ENET_MDIO
R115 4.7K ENET_MDC
R125 4.7K ENET_INTn
R116 4.7K ENET_RESETn

C10 0.01uF R12 49.9 MDI_P0
C8 0.01uF R11 49.9 MDI_N0
C86 0.01uF R10 49.9 MDI_P1
C87 0.01uF R8 49.9 MDI_N1
R105 49.9 MDI_P2
R106 49.9 MDI_N2
R107 49.9 MDI_P3
R108 49.9 MDI_N3

TP2
TP1 ENET_HSDAC_P
ENET_HSDAC_N

3.3V
R113 10.0K

X1
EN OUT NC1 NC2 GND VCC
25MHz
3.3V

J1
VCC 9
TD0_P 1
TD0_N 2
TD1_P 3
TD1_N 6
TD2_P 4
TD2_N 5
TD3_P 7
TD3_N 8
GND 10
GND_TAB 12
GND_TAB 11
HFJ11-1G02E

R117 4.99K
R118 4.7K

U5A
88E1111

27	COMA		
28	RESET_N	ENET_RESETn	
65	CONFIG0	ENET_LED_RX	
64	CONFIG1	ENET_LED_LINK10	
63	CONFIG2		
61	CONFIG3	ENET_LED_TX	
60	CONFIG4	ENET_LED_DUPLEX	
59	CONFIG5		
58	CONFIG6		
29	MDI0_P	MDI_P0	MDI INTERFACE
31	MDI0_N	MDI_N0	
33	MDI1_P	MDI_P1	
34	MDI1_N	MDI_N1	
39	MDI2_P	MDI_P2	
41	MDI2_N	MDI_N2	
42	MDI3_P	MDI_P3	
43	MDI3_N	MDI_N3	
24	MDIO	ENET_MDIO	MGMT
25	MDC	ENET_MDC	
23	INT_N	ENET_INTn	
37	HSDAC_P	ENET_HSDAC_P	TEST
38	HSDAC_N	ENET_HSDAC_N	
30	RSET	ENET_RSET	
56	SEL_FREQ		
22	125CLK	ENET_XTAL_25MHZ	
55	XTAL1		
54	XTAL2		
53	VSSC		
47	TRST_N		JTAG
49	TCK		
44	TDI		
50	TDO		
46	TMS		

8	GTX_CLK	ENET_GTX_CLK	GMII/MII/TBI INTERFACE
4	TX_CLK		
9	TX_EN	ENET_TX_EN	
7	TX_ER		
11	TXD0	ENET_TXD0	
12	TXD1	ENET_TXD1	
14	TXD2	ENET_TXD2	
16	TXD3	ENET_TXD3	
17	TXD4		
18	TXD5		
19	TXD6		
20	TXD7		
2	RXCLK	ENET_RX_CLK	
94	RX_DV	ENET_RX_DV	
3	RX_ER		
95	RXD0	ENET_RXD0	
92	RXD1	ENET_RXD1	
93	RXD2	ENET_RXD2	
91	RXD3	ENET_RXD3	
90	RXD4		
89	RXD5		
87	RXD6		
86	RXD7		
84	CRS		
83	COL		
79	S_CLK_P		SGMII INTERFACE
80	S_CLK_N		
82	S_IN_P		
81	S_IN_N		
77	S_OUT_P		
75	S_OUT_N		
68	LED_TX	ENET_LED_TX	
69	LED_RX	ENET_LED_RX	
70	LED_DUPLEX	ENET_LED_DUPLEX	
73	LED_LINK1000	ENET_LED_LINK1000	
74	LED_LINK100	ENET_LED_LINK100	
76	LED_LINK10	ENET_LED_LINK10	

2.5V
U5B
88E1111

26	VDDOX		
48	VDDOX		
5	VDDO		
21	VDDO		
88	VDDO		
96	VDDO		
72	VDDOH		
66	VDDOH		
52	VDDOH		
32	AVDD		
36	AVDD		
35	AVDD		
40	AVDD		
45	AVDD		
78	AVDD		
13	NC1		
51	NC2		
97	VSS		
1	DVDD	1.2V	
6	DVDD		
10	DVDD		
15	DVDD		
57	DVDD		
62	DVDD		
67	DVDD		
71	DVDD		
85	DVDD		

Place near 88E1111 PHY

2.5V
C191 C164 C115 C166 C132 C117 C193 C116
0.1uF

1.2V
C153 C167 C192 C138 C165
0.1uF

2.5V
ENET_LED_TX R129 220 D7 Green_LED
ENET_LED_RX R131 220 D8 Green_LED
ENET_LED_DUPLEX R126 220 D6 Green_LED
ENET_LED_LINK1000 R119 220 D4 Green_LED
ENET_LED_LINK100 R114 220 D3 Green_LED
ENET_LED_LINK10 R109 220 D1 Green_LED

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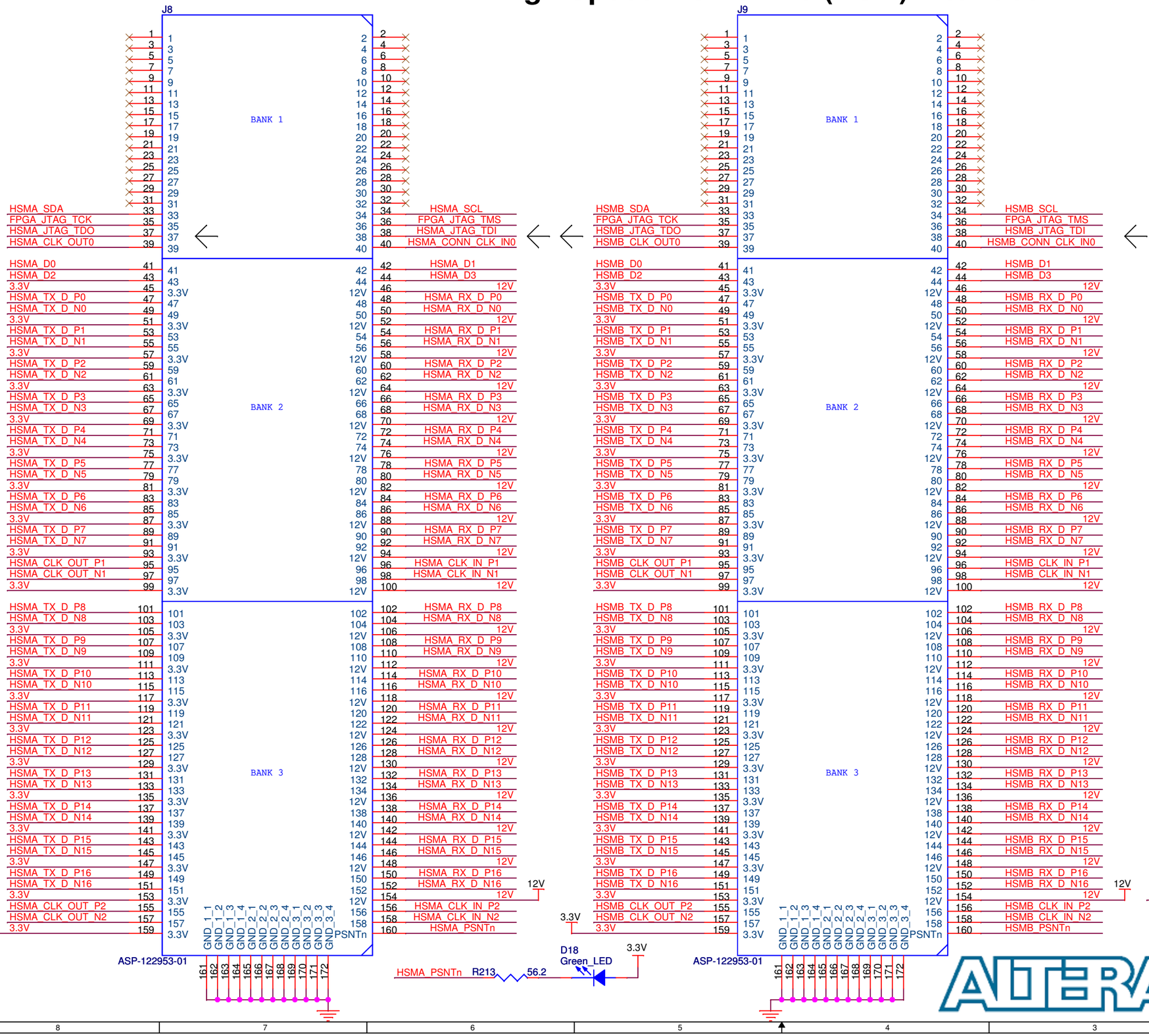
High Speed Mezzanine (HSM) Interface



JTAG INTERFACE

FPGA_JTAG_TCK	FPGA_JTAG_TCK 8,17
FPGA_JTAG_TMS	FPGA_JTAG_TMS 8,17
HSMA_JTAG_TDO	HSMA_JTAG_TDO 8
HSMA_JTAG_TDI	HSMA_JTAG_TDI 8
HSMB_JTAG_TDO	HSMB_JTAG_TDO 8
HSMB_JTAG_TDI	HSMB_JTAG_TDI 8

HSMC PORT A

HSMA_SDA	HSMA_SDA 18
HSMA_SCL	HSMA_SCL 18
HSMA_CONN_CLK_IN0	HSMA_CONN_CLK_IN0 7
HSMA_CLK_OUT0	HSMA_CLK_OUT0 18
HSMA_CLK_IN_P[2:1]	HSMA_CLK_IN_P[2:1] 7,15
HSMA_CLK_IN_N[2:1]	HSMA_CLK_IN_N[2:1] 7,15
HSMA_CLK_OUT_P[2:1]	HSMA_CLK_OUT_P[2:1] 18
HSMA_CLK_OUT_N[2:1]	HSMA_CLK_OUT_N[2:1] 18
HSMA_D[3:0]	HSMA_D[3:0] 18
HSMA_TX_D_P[16:0]	HSMA_TX_D_P[16:0] 6,18
HSMA_TX_D_N[16:0]	HSMA_TX_D_N[16:0] 18
HSMA_RX_D_P[16:0]	HSMA_RX_D_P[16:0] 15,18
HSMA_RX_D_N[16:0]	HSMA_RX_D_N[16:0] 15,18

HSMC PORT B

HSMB_SDA	HSMB_SDA 18
HSMB_SCL	HSMB_SCL 18
HSMB_CONN_CLK_IN0	HSMB_CONN_CLK_IN0 7
HSMB_CLK_OUT0	HSMB_CLK_OUT0 6
HSMB_CLK_IN_P[2:1]	HSMB_CLK_IN_P[2:1] 7,15
HSMB_CLK_IN_N[2:1]	HSMB_CLK_IN_N[2:1] 7,15
HSMB_CLK_OUT_P[2:1]	HSMB_CLK_OUT_P[2:1] 18
HSMB_CLK_OUT_N[2:1]	HSMB_CLK_OUT_N[2:1] 18
HSMB_D[3:0]	HSMB_D[3:0] 18
HSMB_TX_D_P[16:0]	HSMB_TX_D_P[16:0] 6,18
HSMB_TX_D_N[16:0]	HSMB_TX_D_N[16:0] 18
HSMB_RX_D_P[16:0]	HSMB_RX_D_P[16:0] 15,18
HSMB_RX_D_N[16:0]	HSMB_RX_D_N[16:0] 15,18

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High Speed Mezzanine (HSM) Termination

By default all of the data signal on the HSMC's are single ended. 100 Ohm resistors should be installed between the P/N pairs in order to use differential signals.

R190 DNI HSMA_RX_D_P0 / HSMA_RX_D_N0
R187 DNI HSMA_RX_D_P1 / HSMA_RX_D_N1
R186 DNI HSMA_RX_D_P2 / HSMA_RX_D_N2
R181 DNI HSMA_RX_D_P3 / HSMA_RX_D_N3
R180 DNI HSMA_RX_D_P4 / HSMA_RX_D_N4
R176 DNI HSMA_RX_D_P5 / HSMA_RX_D_N5
R175 DNI HSMA_RX_D_P6 / HSMA_RX_D_N6
R172 DNI HSMA_RX_D_P7 / HSMA_RX_D_N7

R150 DNI HSMB_RX_D_P0 / HSMB_RX_D_N0
R149 DNI HSMB_RX_D_P1 / HSMB_RX_D_N1
R154 DNI HSMB_RX_D_P2 / HSMB_RX_D_N2
R153 DNI HSMB_RX_D_P3 / HSMB_RX_D_N3
R158 DNI HSMB_RX_D_P4 / HSMB_RX_D_N4
R157 DNI HSMB_RX_D_P5 / HSMB_RX_D_N5
R162 DNI HSMB_RX_D_P6 / HSMB_RX_D_N6
R161 DNI HSMB_RX_D_P7 / HSMB_RX_D_N7

R166 DNI HSMA_RX_D_P8 / HSMA_RX_D_N8
R165 DNI HSMA_RX_D_P9 / HSMA_RX_D_N9
R160 DNI HSMA_RX_D_P10 / HSMA_RX_D_N10
R159 DNI HSMA_RX_D_P11 / HSMA_RX_D_N11
R156 DNI HSMA_RX_D_P12 / HSMA_RX_D_N12
R155 DNI HSMA_RX_D_P13 / HSMA_RX_D_N13
R152 DNI HSMA_RX_D_P14 / HSMA_RX_D_N14
R151 DNI HSMA_RX_D_P15 / HSMA_RX_D_N15
R148 DNI HSMA_RX_D_P16 / HSMA_RX_D_N16

R167 DNI HSMB_RX_D_P8 / HSMB_RX_D_N8
R174 DNI HSMB_RX_D_P9 / HSMB_RX_D_N9
R173 DNI HSMB_RX_D_P10 / HSMB_RX_D_N10
R179 DNI HSMB_RX_D_P11 / HSMB_RX_D_N11
R178 DNI HSMB_RX_D_P12 / HSMB_RX_D_N12
R184 DNI HSMB_RX_D_P13 / HSMB_RX_D_N13
R183 DNI HSMB_RX_D_P14 / HSMB_RX_D_N14
R189 DNI HSMB_RX_D_P15 / HSMB_RX_D_N15
R188 DNI HSMB_RX_D_P16 / HSMB_RX_D_N16

HSMA_CLK_IN_P1 — R185 — DNI — HSMA_CLK_IN_N1
HSMA_CLK_IN_P2 — R147 — DNI — HSMA_CLK_IN_N2
HSMB_CLK_IN_P1 — R168 — DNI — HSMB_CLK_IN_N1
HSMB_CLK_IN_P2 — R192 — DNI — HSMB_CLK_IN_N2

HSMC PORT A

HSMA_CLK_IN_P[2:1]	HSMA_CLK_IN_P[2:1]	7,14
HSMA_CLK_IN_N[2:1]	HSMA_CLK_IN_N[2:1]	7,14
HSMA_RX_D_P[16:0]	HSMA_RX_D_P[16:0]	14,18
HSMA_RX_D_N[16:0]	HSMA_RX_D_N[16:0]	14,18

HSMC PORT B

HSMB_CLK_IN_P[2:1]	HSMB_CLK_IN_P[2:1]	7,14
HSMB_CLK_IN_N[2:1]	HSMB_CLK_IN_N[2:1]	7,14
HSMB_RX_D_P[16:0]	HSMB_RX_D_P[16:0]	14,18
HSMB_RX_D_N[16:0]	HSMB_RX_D_N[16:0]	14,18

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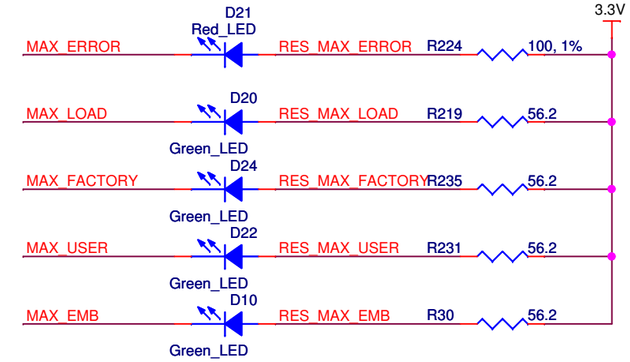
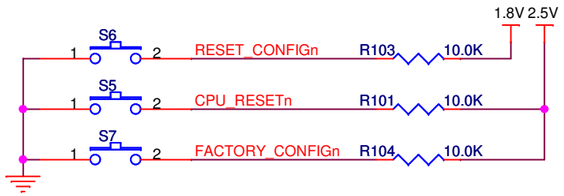
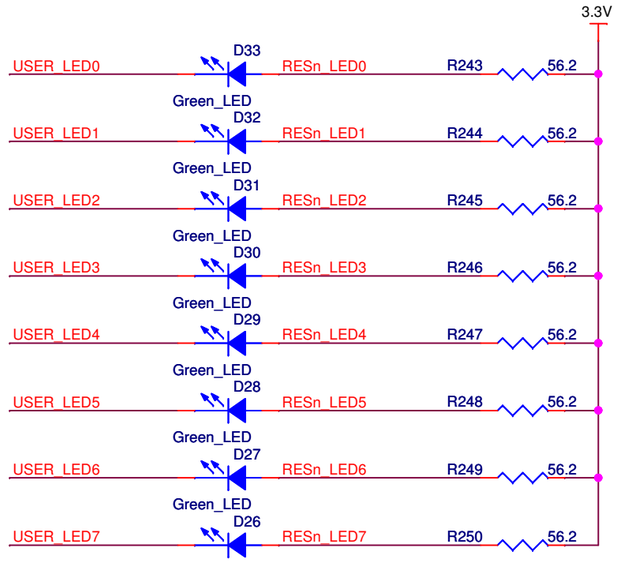
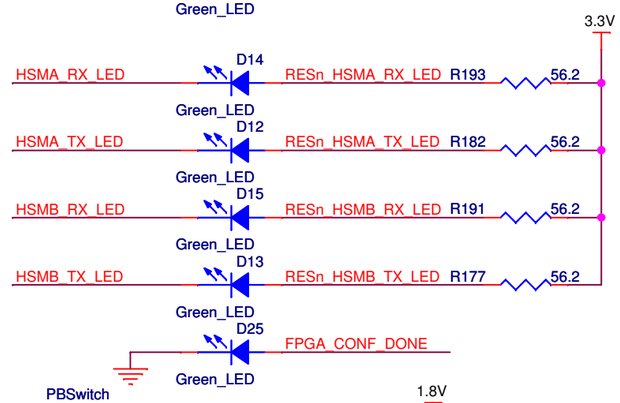
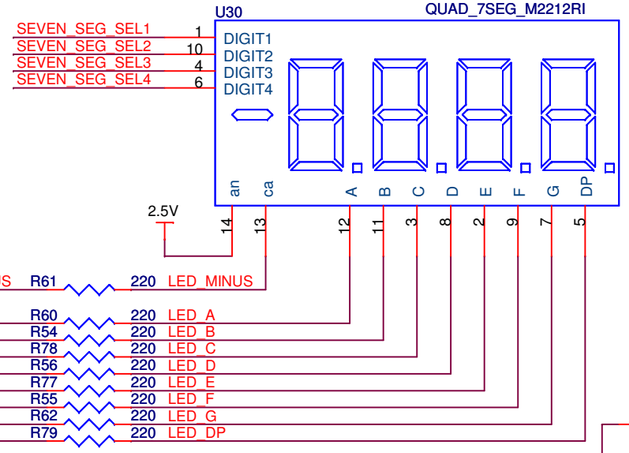
User IO & Connector

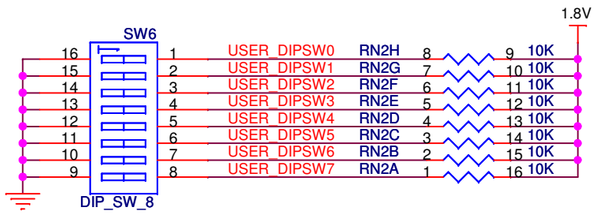


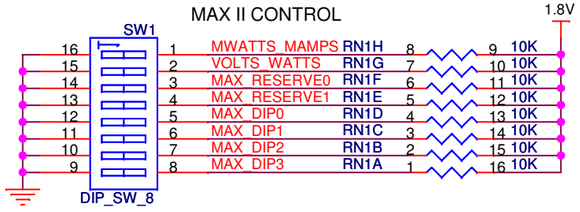


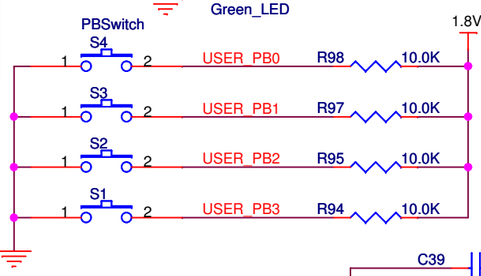


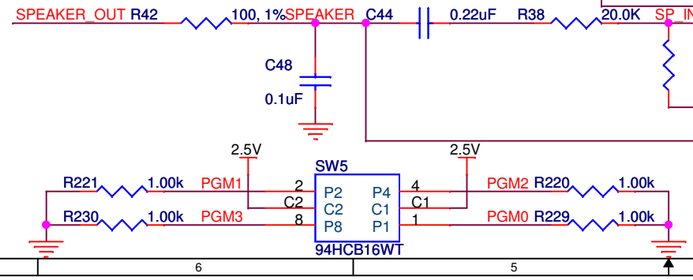


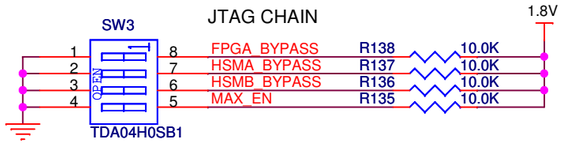


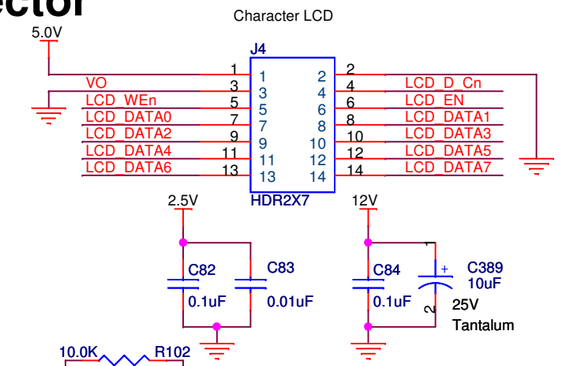


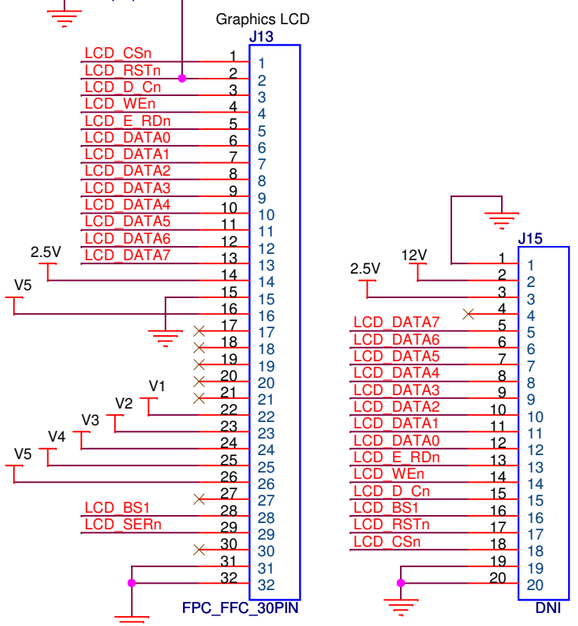


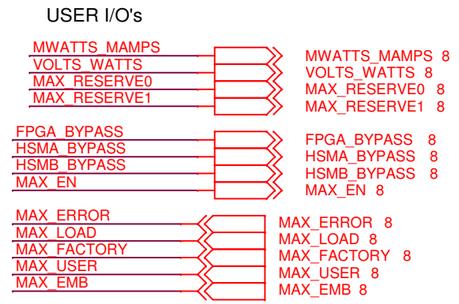


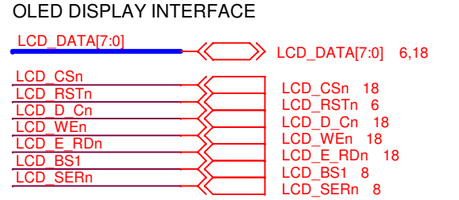












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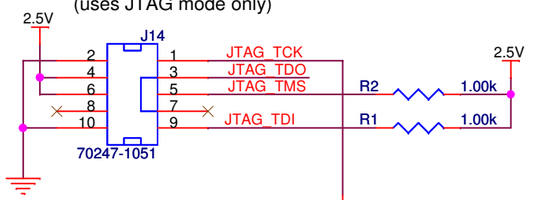
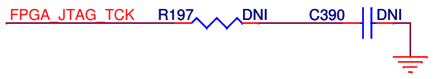
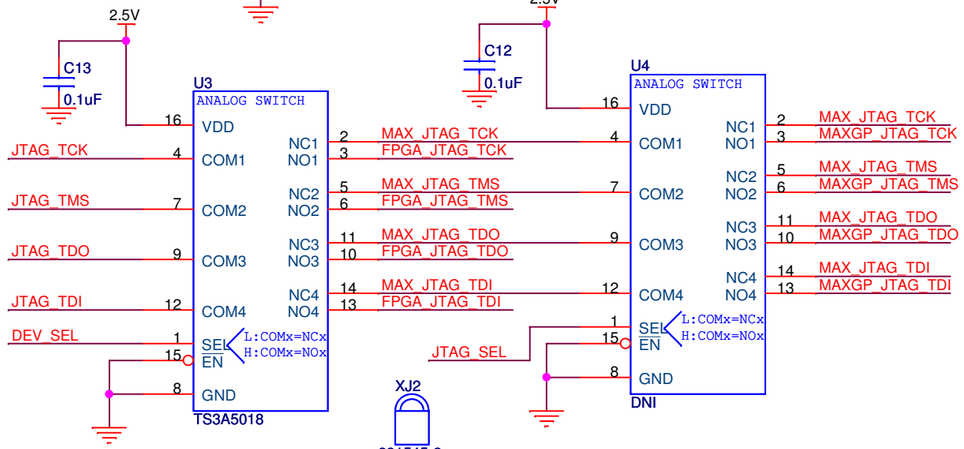
Cyclone III Configuration

USB Blaster Programming Header
(uses JTAG mode only)

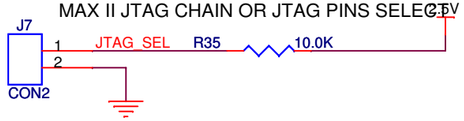


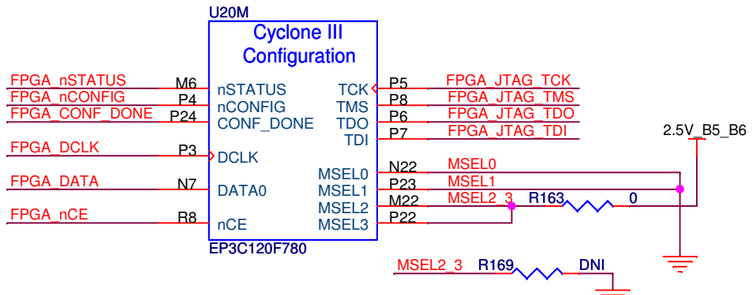




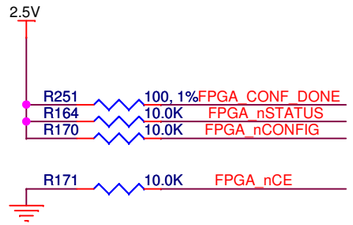
JTAG CYCLONE III OR MAXII SELECT

MAX II JTAG CHAIN OR JTAG PINS SELECT





Passive Serial Standard: MSEL[3:0]=0000
Passive Serial Fast: MSEL[3:0]=1100
MSEL pins have internal 5kOhm pull-downs.



CONFIGURATION INTERFACE

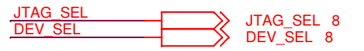
FPGA JTAG INTERFACE

MAXII JTAG INTERFACE

MAXII GPIO JTAG

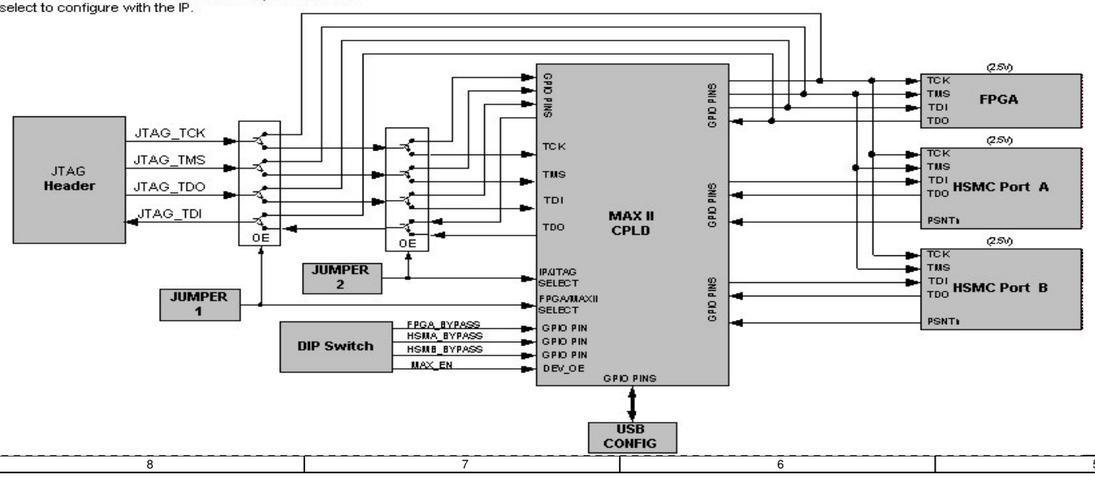
HSMC JTAG

JUMPER STATE TO MAX II



JTAG REFERENCE

JUMPER1 will be usede to select between a direct JTAG connection to the FPGA or the MAXII. By default it will select a direct connection to the FPGA.
JUMPER2 will be used to select between configuring with the IP or the MAX II JTAG header. By default it will select to configure with the IP.



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Cyclone III Banks 1, 2, 5 & 6

U20A
Cyclone III, Bank 1A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

HSMA_TX_D_P0	R7	DIFFIO_L26p(NC/NC/29n)	DIFFIO_L24p	P2	HSMA_TX_D_P5
HSMA_TX_D_N0	R6	DIFFIO_L26n(IO/NC/x)	DIFFIO_L24n/DQ0L	P1	HSMA_TX_D_N5
HSMA_CLK_OUT_P2	D2	DIFFIO_L2p/DQ2L	DIFFIO_L30p(x/x/27n)	U2	HSMA_RX_D_P5
HSMA_CLK_OUT_N2	D1	DIFFIO_L2n/DQ2L	DIFFIO_L30n/DQ1L(x/x/32p)	U1	HSMA_RX_D_N5
HSMA_CLK_OUT_N1	G5	DIFFIO_L3n/DQ2L	DIFFIO_L15p(x/NC/IO)	M4	HSMA_TX_D_P6
			DIFFIO_L15n(x/NC/21p)	M3	HSMA_TX_D_N6
HSMA_RX_D_P0	AB2	DIFFIO_L33p/DQS1L			
HSMA_RX_D_N0	AB1	DIFFIO_L33n	DIFFIO_L35p/DQ3L(x/x/39n)	U6	HSMA_RX_D_P6
HSMA_TX_D_P1	V4	DIFFIO_L31p/DQ1L(x/x/32n)	DIFFIO_L35n	U5	HSMA_RX_D_N6
			DIFFIO_L23p	M2	HSMA_TX_D_P7
HSMA_RX_D_P1	Y4	DIFFIO_L36p/DQ3L	DIFFIO_L23n/DQ0L	M1	HSMA_TX_D_N7
HSMA_RX_D_N1	Y3	DIFFIO_L36n	DIFFIO_L19n(NC/NC/x)	L6	HSMA_TX_D_N8
HSMA_RX_D_P2	U3	DIFFIO_L27p/DM0L			
HSMA_RX_D_N2	U4	DIFFIO_L27n(x/x/31p)	DIFFIO_L18p(NC/NC/VCCIO1)	K8	HSMA_TX_D_P9
HSMA_TX_D_N2	T3	DIFFIO_L29n	DIFFIO_L18n(NC/NC/15p)	L8	HSMA_TX_D_N9
			DIFFIO_L25p/DQ0L	R2	HSMA_RX_D_P7
HSMA_RX_D_P3	W2	DIFFIO_L34p/DQ1L	DIFFIO_L25n	R1	HSMA_RX_D_N7
HSMA_RX_D_N3	W1	DIFFIO_L34n/DM1L	DIFFIO_L13p(x/NC/x)	K4	HSMA_TX_D_P10
			DIFFIO_L13n(x/NC/x)	K3	HSMA_TX_D_N10
HSMA_TX_D_P3	R3	DIFFIO_L28p/DQ1L			
HSMA_TX_D_N3	R4	DIFFIO_L28n/DQ1L(x/x/29p)	DIFFIO_L20p(IO/NC/x)	N4	HSMA_RX_D_P8
HSMA_TX_D_P4	M8	DIFFIO_L21p(NC/NC/x)	DIFFIO_L20n(IO/NC/x)	N3	HSMA_RX_D_N8
HSMA_TX_D_N4	M7	DIFFIO_L21n(NC/NC/x)	DIFFIO_L10p	J4	HSMA_TX_D_P11
HSMA_RX_D_P4	V2	DIFFIO_L32p/DQ1L(x/x/33n)	DIFFIO_L10n/DQ0L	J3	HSMA_TX_D_N11
HSMA_RX_D_N4	V1	DIFFIO_L32n/DQ1L(x/x/33p)	DIFFIO_L17p(NC/NC/11n)	J7	HSMA_TX_D_P12
			DIFFIO_L17n(NC/NC/14p)	K7	HSMA_TX_D_N12
	H5	IO(x/x/18n)			
	H6	IO(x/x/18p)			

U20N
Cyclone III, Bank 1B
EP3C120
(EP3C80/EP3C55/EP3C40)
EP3C120F780

HSMA_TX_D_P2	T4	DIFFIO_L29p/DQ1L	
HSMA_TX_D_N1	V3	DIFFIO_L31n(x/x/33p)	
HSMA_CLK_OUT_P1	G6	DIFFIO_L3p/nRESET/DQ2L	

U20O
Cyclone III, Bank 5B
EP3C120
(EP3C80/EP3C55/EP3C40)
EP3C120F780

CPU_RESETn	T21	DIFFIO_R29p/DEV_CLRn	
	T22	DIFFIO_R29n/DEV_OE	

U20E
Cyclone III, Bank 5A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

HSMB_RX_D_P8	P21	DIFFIO_R25p(NC/NC/IO)	DM3R(x/x/55n)	AB24	LCD_CSn
HSMB_RX_D_N8	R21	DIFFIO_R25n(NC/NC/29p)			
HSMB_RX_D_P7	P27	DIFFIO_R23p/CLKUSR	DIFFIO_R14p(x/x/28n)	K25	HSMB_RX_D_P2
HSMB_RX_D_N7	P28	DIFFIO_R23n/nCEO	DIFFIO_R14n/DQ2R(x/x/10p)	K26	HSMB_RX_D_N2
HSMB_TX_D_P12	AB25	DIFFIO_R44p(x/x/40n)	DIFFIO_R28p	R25	HSMB_TX_D_P5
HSMB_TX_D_N12	AB26	DIFFIO_R44n/DQ3R(x/x/46p)	DIFFIO_R28n/DQ1R	R26	HSMB_TX_D_N5
			DIFFIO_R27p(x/x/IO)	R27	HSMB_TX_D_P4
HSMB_TX_D_P11	AA25	DIFFIO_R43p(x/x/39n)	DIFFIO_R27n/DM0R	R28	HSMB_TX_D_N4
HSMB_TX_D_N11	AA26	DIFFIO_R43n/DQ3R			
			DIFFIO_R15p/nOE/DQ2R	G27	HSMB_RX_D_P1
HSMB_RX_D_P6	P25	DIFFIO_R24p/CRC_ERROR	DIFFIO_R15n/nWE/DQ2R	G28	HSMB_RX_D_N1
HSMB_RX_D_N6	P26	DIFFIO_R24n/INIT_DONE	DIFFIO_R22p(x/x/25n)	N25	HSMB_TX_D_P3
HSMB_TX_D_P10	Y25	DIFFIO_R41p(x/x/35n)	DIFFIO_R22n/DQS0R	N26	HSMB_TX_D_N3
HSMB_TX_D_N10	Y26	DIFFIO_R41n/DQ1R(x/x/43p)	DIFFIO_R20p(x/x/VREFB6N2)	M25	HSMB_TX_D_P2
HSMB_RX_D_P5	M27	DIFFIO_R21p/DQ0R(x/x/IO)	DIFFIO_R20n/DQ0R(x/x/21p)	M26	HSMB_TX_D_N2
HSMB_RX_D_N5	M28	DIFFIO_R21n/DQ0R			
			DIFFIO_R13p/RDY	F27	HSMB_RX_D_P0
HSMB_TX_D_P9	W25	DIFFIO_R40p(x/x/IO)	DIFFIO_R13n/nAVD/DQ2R	F28	HSMB_RX_D_N0
HSMB_TX_D_N9	W26	DIFFIO_R40n/DQ1R(x/x/42p)	DIFFIO_R18p	L23	HSMB_TX_D_P1
HSMB_RX_D_P4	L27	DIFFIO_R19p/DQ0R(x/x/17n)	DIFFIO_R18n/DQ0R(x/x/17p)	L24	HSMB_TX_D_N1
HSMB_RX_D_N4	L28	DIFFIO_R19n/DQ0R(x/x/18p)	DIFFIO_R47p/DQ3R(x/x/49n)	AD27	HSMB_CLK_OUT_P2
HSMB_TX_D_P8	V25	DIFFIO_R37p/DQ1R(x/x/38n)	DIFFIO_R47n/DQ3R	AD28	HSMB_CLK_OUT_N2
HSMB_TX_D_N8	V26	DIFFIO_R37n(x/x/IO)			
			DIFFIO_R16p	J25	HSMB_TX_D_P0
HSMB_RX_D_P3	K27		DIFFIO_R16n(x/x/IO)	J26	HSMB_TX_D_N0
HSMB_RX_D_N3	K28	DIFFIO_R17p/DQ0R	DIFFIO_R49p	AC26	HSMB_CLK_OUT_P1
HSMB_TX_D_P7	V27	DIFFIO_R17n/DQ0R(x/x/16p)	DIFFIO_R49n/DQ3R(x/x/52p)	AD26	HSMB_CLK_OUT_N1
HSMB_TX_D_N7	V28	DIFFIO_R38p	DIFFIO_R50p(NC/NC/54n)	AE26	GND
HSMB_TX_D_P6	U25	DIFFIO_R38n/DQ1R(x/x/40p)	DIFFIO_R50n/DQS3R(IO/IO/IO)	AF27	GND
HSMB_TX_D_N6	U26	DIFFIO_R33p	DIFFIO_R51p	AC24	LCD_EN
		DIFFIO_R33n(x/x/45p)	DIFFIO_R51n	AC25	ENET_LED_LINK1000
	AA22	RUP3	IO(NC/NC/51p)	AA23	
	AB23	RDN3			

U20B
Cyclone III, Bank 2
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

GND	R5	DQ1L(x/x/31n)	DQ3L(x/x/47p)	AB3	LCD_DATA7
HSMA_RX_D_P9	L4	DIFFIO_L14p(x/NC/x)	DIFFIO_L38p/DQ3L(x/x/45n)	AC3	HSMA_SCL
HSMA_RX_D_N9	L3	DIFFIO_L14n(x/NC/x)	DIFFIO_L38n	AD3	GND
HSMA_TX_D_P13	G2	DIFFIO_L11p/DQ0L	DIFFIO_L39p/DQ3L	AD2	ENET_RESETn
HSMA_TX_D_N13	G1	DIFFIO_L11n	DIFFIO_L39n	AD1	LCD_DATA1
HSMA_RX_D_P10	L2	DIFFIO_L22p(x/NC/x)	DIFFIO_L40p/DQ3L(x/x/47n)	AA4	LCD_DATA0
HSMA_RX_D_N10	L1	DIFFIO_L22n/DQ0L	DIFFIO_L40n(x/x/IO)	AA3	HSMA_TX_LED
HSMA_TX_D_P14	F5	DIFFIO_L5p/DQ2L	DIFFIO_L41p/DQ3L(x/x/49n)	AE2	LCD_DATA4
HSMA_TX_D_N14	F4	DIFFIO_L5n/DATA1/ASDO	DIFFIO_L41n(x/x/49p)	AE1	HSMA_RX_LED
HSMA_TX_D_P15	E2	DIFFIO_L8p/FLASH_nCE/nCSO	DIFFIO_L42p(NC/NC/x)	V6	LCD_DATA6
HSMA_TX_D_N15	E1	DIFFIO_L8n(x/x/11p)	DIFFIO_L42n(NC/NC/39p)	V5	LCD_DATA5
HSMA_RX_D_P11	K2	DIFFIO_L12p/DQS0L(x/x/IO)			
HSMA_RX_D_N11	K1	DIFFIO_L12n/DQ0L	DIFFIO_L43n(NC/NC/45p)	V7	LCD_E_RDn
HSMA_TX_D_P16	D3	DIFFIO_L1p	DIFFIO_L44p(NC/NC/36n)	W4	ENET_TXD0
HSMA_TX_D_N16	C2	DIFFIO_L1n/DQ2L	DIFFIO_L44n(IO/NC/36p)	W3	ENET_TXD3
			DIFFIO_L45p(NC/NC/38n)	Y6	ENET_RXD3
HSMA_RX_D_P12	J6	DIFFIO_L16p(NC/NC/10n)	DIFFIO_L45n(NC/NC/38p)	Y5	ENET_TXD2
HSMA_RX_D_N12	J5	DIFFIO_L16n(NC/NC/6p)			
HSMA_RX_D_P13	H4	DIFFIO_L7p	DIFFIO_L46p(NC/NC/x)	W8	ENET_RXD0
HSMA_RX_D_N13	H3	DIFFIO_L7n	DIFFIO_L46n(NC/NC/x)	Y7	HSMA_CLK_OUT0
HSMA_RX_D_P14	G4	DIFFIO_L6p/DQ2L	DIFFIO_L47p(NC/NC/40n)	AA6	ENET_RXD1
HSMA_RX_D_N14	G3	DIFFIO_L6n	DIFFIO_L47n(NC/NC/50p)	AA5	ENET_TXD1
			DIFFIO_L48p/DQS3L(x/IO/IO)	AE3	HSMA_D2
HSMA_RX_D_P15	F2	DIFFIO_L9p/DM2L	DIFFIO_L48n/DM3L(x/33p/x)	AF2	HSMA_D1
HSMA_RX_D_N15	F1	DIFFIO_L9n/DQ0L			
HSMA_RX_D_P16	E3	DIFFIO_L4p/DQS2L			
HSMA_RX_D_N16	F3	DIFFIO_L4n/DQ2L	DIFFIO_L49p(x/NC/x)	AC5	HSMA_D3
GND	AC2	DIFFIO_L37p/DQ3L(x/x/43n)	DIFFIO_L49n(x/NC/52p)	AC4	LCD_WEn
HSMA_SDA	AC1	DIFFIO_L37n/DQ3L	DIFFIO_L50p(IO/NC/x)	AB6	HSMA_D0
			DIFFIO_L50n(IO/NC/x)	AB5	LCD_DATA3
	U7	RUP1			
	U8	RDN1	IO(NC/NC/40p)	AA7	ENET_TX_EN

U20F
Cyclone III, Bank 6A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

GND	L26	DM2R(x/x/14p)			
USB_REN	G23		DIFFIO_R42p/DQ1R	AB27	HSMB_RX_D_P15
HSMB_D0	G24	DIFFIO_R1p(NC/NC/x)	DIFFIO_R42n/DM1R	AB28	HSMB_RX_D_N15
USB_FULL	F24	DIFFIO_R1n(NC/NC/25p)			
USB_EMPTY	F25	DIFFIO_R2p(x/NC/15n)	DIFFIO_R35p(NC/NC/43n)	V21	HSMB_TX_D_P16
HSMB_D2	G25	DIFFIO_R2n(x/NC/4p)	DIFFIO_R35n(NC/NC/47p)	W21	HSMB_TX_D_N16
USB_FD5	G26	DIFFIO_R3p(x/NC/10n)	DIFFIO_R39p/DQ1R	W28	HSMB_RX_D_P13
HSMB_D1	H23	DIFFIO_R3n(x/NC/x)	DIFFIO_R39n/DQ1R	W27	HSMB_RX_D_N13
HSMB_D3	H24	DIFFIO_R4p(x/NC/13n)	DIFFIO_R31p(NC/NC/x)	W22	HSMB_TX_D_P15
		DIFFIO_R4n(x/x/11p)	DIFFIO_R31n(NC/NC/x)	Y22	HSMB_TX_D_N15
USB_FD3	K21	DIFFIO_R5p(NC/NC/x)	DIFFIO_R34p(NC/NC/x)	U22	HSMB_RX_D_P12
USB_FD1	K22	DIFFIO_R5n(NC/NC/x)	DIFFIO_R34n(NC/NC/IO)	V22	HSMB_RX_D_N12
USB_FD6	J23	DIFFIO_R6p(NC/NC/18n)	DIFFIO_R48n/DQ3R	AE28	HSMB_TX_D_N14
USB_FD4	J24	DIFFIO_R6n(NC/NC/x)	DIFFIO_R32p(26n/IO/x)	U27	HSMB_TX_D_P11
			DIFFIO_R32n/DQ1R(x/x/36p)	U28	HSMB_RX_D_N11
USB_FD2	L22	DIFFIO_R7n(NC/NC/23p)	DIFFIO_R46p	Y23	HSMB_TX_D_P13
USB_FD7	D26	DIFFIO_R8p(x/x/1n)	DIFFIO_R46n/DQ3R	Y24	HSMB_TX_D_N13
HSMB_RX_LED	F26	DIFFIO_R10p/DQ2R(x/x/IO)	IO(x/x/26p)	L25	GND
USB_WEN	E26	DIFFIO_R10n(6p/NC/x)	IO(x/NC/28p)	M24	GND
HSMB_SCL	H25	DIFFIO_R11p(6n/NC/19n)	IO(NC/NC/22p)	M23	GND
HSMB_SDA	H26	DIFFIO_R11n	IO(NC/NC/11n)	H22	SPEAKER_OUT
GND	E27	DIFFIO_R12p/DQ2R(x/x/6n)			

OLED DISPLAY INTERFACE
LCD_DATA[7:0] — LCD_DATA[7:0] 6,16
LCD_CSn — LCD_CSn 16
LCD_D_Cn — LCD_D_Cn 16
LCD_WEn — LCD_WEn 16
LCD_E_RDn — LCD_E_RDn 16

2x16 LED DISPLAY INTERFACE
LCD_EN — LCD_EN 16

USER I/O
CPU_RESETn — CPU_RESETn 8,16

HSMC PORT A

HSMA_SDA	HSMA_SDA 14
HSMA_SCL	HSMA_SCL 14
HSMA_CLK_OUT0	HSMA_CLK_OUT0 14
HSMA_RX_LED	HSMA_RX_LED 16
HSMA_TX_LED	HSMA_TX_LED 16
HSMA_CLK_OUT_P[2:1]	HSMA_CLK_OUT_P[2:1] 14
HSMA_CLK_OUT_N[2:1]	HSMA_CLK_OUT_N[2:1] 14
HSMA_D[3:0]	HSMA_D[3:0] 14
HSMA_TX_D_P[16:0]	HSMA_TX_D_P[16:0] 6,14
HSMA_TX_D_N[16:0]	HSMA_TX_D_N[16:0] 14
HSMA_RX_D_P[16:0]	HSMA_RX_D_P[16:0] 14,15
HSMA_RX_D_N[16:0]	HSMA_RX_D_N[16:0] 14,15

HSMC PORT B

HSMB_SCL	HSMB_SCL 14
HSMB_SDA	HSMB_SDA 14
HSMB_RX_LED	HSMB_RX_LED 16
HSMB_TX_LED	HSMB_TX_LED 16
HSMB_CLK_OUT_P[2:1]	HSMB_CLK_OUT_P[2:1] 14
HSMB_CLK_OUT_N[2:1]	HSMB_CLK_OUT_N[2:1] 14
HSMB_D[3:0]	HSMB_D[3:0] 14
HSMB_TX_D_P[16:0]	HSMB_TX_D_P[16:0] 6,14
HSMB_TX_D_N[16:0]	HSMB_TX_D_N[16:0] 14
HSMB_RX_D_P[16:0]	HSMB_RX_D_P[16:0] 14,15
HSMB_RX_D_N[16:0]	HSMB_RX_D_N[16:0] 14,15

ETHERNET INTERFACE

ENET_TXD[3..0]	ENET_TXD[3..0] 13
ENET_RXD[3..0]	ENET_RXD[3..0] 6,13
ENET_TX_EN	ENET_TX_EN 13
ENET_RESETn	ENET_RESETn 13
ENET_LED_LINK1000	ENET_LED_LINK1000 13

USB 2.0 INTERFACE

USB_FD[7:0]	USB_FD[7:0] 6,8
USB_CMD_DATA	USB_CMD_DATA 8
USB_REN	USB_REN 8
USB_WEN	USB_WEN 8
USB_EMPTY	USB_EMPTY 8
USB_FULL	USB_FULL 8
SPEAKER_OUT	SPEAKER_OUT 16

U20P
Cyclone III, Bank 6B
EP3C120
(EP3C80/EP3C55/EP3C40)
EP3C120F780

USB_CMD_DATA	C27	DIFFIO_R8n/PADD20/DQS2R	
LCD_D_Cn	D27	DIFFIO_R9p/PADD21/DQ2R	
HSMB_TX_LED	D28	DIFFIO_R9n/PADD22	
GND	E28	DIFFIO_R12n/PADD23/DQ2R	
HSMB_RX_D_P16	AC27	DIFFIO_R45p/DQ3R(x/x/46n)	
HSMB_RX_D_N16	AC28	DIFFIO_R45n/DQ3R	
HSMB_RX_D_P14	V23	DIFFIO_R36p(x/NC/36n)	
HSMB_RX_D_N14	V24	DIFFIO_R36n(x/NC/x)	
HSMB_RX_D_P10	T25	DIFFIO_R30p/DQS1R	
HSMB_RX_D_N10	T26	DIFFIO_R30n(26p/NC/35p)	
HSMB_RX_D_P9	R22	DIFFIO_R26p(NC/NC/x)	
HSMB_RX_D_N9	R23	DIFFIO_R26n(NC/NC/x)	

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Cyclone III Banks 3, 4, 7 & 8

U20C — Cyclone III, Bank 3
EP3C120 (EP3C80 / EP3C55 / EP3C40) — EP3C120F780

USER_PB0	AD7	DQS1B(x/x/6p)	DIFFIO_B18p/DQ5B	AE11	DDR2_DQ16
GND	AF6	DQ1B			
			DIFFIO_B14p(x/x/5n)	AE8	FSA15
SEVEN_SEG_A	AD5	DIFFIO_B1p(x/x/53n)	DIFFIO_B14n/DM5B(x/x/19p)	AF8	DDR2_DM2
SEVEN_SEG_G	AE6	DIFFIO_B1n/DM1B	DIFFIO_B15p/DQS3B	AE10	DDR2_DQS3
SEVEN_SEG_DP	AD4	DIFFIO_B2p(x/x/IO)	DIFFIO_B20p/DQ5B(x/x/23n)	AG11	DDR2_DQ17
FSA7	AF4	DIFFIO_B2n/DQ1B(x/x/3p)	DIFFIO_B16p/DQ5B	AG10	DDR2_DQ18
DDR2BOT_A14	AE12	DIFFIO_B17n	DIFFIO_B16n	AH10	FSA1
FSA22	AG3	DIFFIO_B3n/DQ1B			
			DIFFIO_B20n/DQ5B(x/x/24p)	AH11	DDR2_DQ19
USER_PB2	AH3	DIFFIO_B4p/DQ1B	DIFFIO_B5n/DQ1B	AH4	DDR2BOT_BA2
DDR2BOT_A10	AE4	DIFFIO_B3p	DQ5B(x/x/20p)	AE9	DDR2_DQ20
DDR2BOT_A6	AD12	IO(*/NC/2p)	DIFFIO_B18n/DQS5B	AF11	DDR2_DQS2
DDR2BOT_A11	AF21	DIFFIO_B47n(x/x/47p)			
FSA8	AD8	DIFFIO_B6p/DQ1B(x/x/9n)	DIFFIO_B19n(NC/NC/9p)	AC10	FSA3
DDR2BOT_CKE	AG4	DIFFIO_B5p			
DDR2BOT_A12	Y12	DIFFIO_B25p(NC/NC/6n)	DIFFIO_B17p/DQ5B(x/x/22n)	AE12	DDR2_DQ21
FSA10	AH6	DIFFIO_B7n/DQ1B(x/x/11p)	DIFFIO_B15n/DQ5B(x/x/21p)	AE10	DDR2_DQ22
			DIFFIO_B21p/DQ5B	AE13	DDR2_DQ23
			DIFFIO_B21n(x/NC/x)	AF13	FSA16
DDR2_DQ24	AC8	DIFFIO_B10n/DQ3B(x/x/14p)	DIFFIO_B22p(NC/NC/x)	AC12	USER_PB1
FSA12	AF9	DQ3B(x/x/18p)	PLL1_CLKOUTn	AF5	DDR2BOT_BA1
DDR2_DM3	AB9	DIFFIO_B8p/DM3B	DIFFIO_B23p(x/NC/x)	AE14	DDR2_CK_P0
DDR2BOT_BA0	AF3	DIFFIO_B4n	DIFFIO_B23n(x/NC/x)	AF14	DDR2_CK_N0
DDR2_DQ25	AH7	DIFFIO_B9n/DQ3B(x/x/IO)	DIFFIO_B24p(x/NC/x)	AC11	FSA0
DDR2_DQ26	AG8	DIFFIO_B12p/DQ3B	DIFFIO_B24n(x/NC/x)	AD11	GND
FSA24	AB7	DIFFIO_B10p	DIFFIO_B30p(NC/NC/IO)	Y14	DDR2BOT_A13
DDR2_DQ27	AH8	DIFFIO_B12n/DQ3B			
			DIFFIO_B22n(NC/NC/x)	AB12	DDR2BOT_A4
FSA13	AA8	DIFFIO_B11p	DIFFIO_B26n(NC/NC/x)	AA13	FSA2
DDR2_DQ28	AG7	DIFFIO_B9p/DQ3B			
DDR2_DQ29	AA10	DIFFIO_B11n/DQ3B	DIFFIO_B27n(NC/NC/x)	AB14	FSA17
DDR2_DQ30	AF7	DIFFIO_B13n/DQ3B(x/x/17p)	DIFFIO_B28p/DQ5B	AG12	FSA19
DDR2BOT_A7	AB8	DIFFIO_B8n(x/x/IO)	DIFFIO_B13p	AE7	DDR2BOT_A3
DDR2_DQ31	AD10	DQ3B(x/x/12n)	DIFFIO_B29p(NC/NC/25n)	AC14	USER_DIPSW0
			DIFFIO_B29n(NC/NC/x)	AD14	USER_DIPSW4
DDR2BOT_A9	AB10	DIFFIO_B19p(NC/NC/VCCIO3)	DIFFIO_B7p/DQ1B	AG6	DDR2BOT_A1
			DIFFIO_B30n(NC/NC/x)	Y15	FSA4

U20D — Cyclone III, Bank 4
EP3C120 (EP3C80 / EP3C55 / EP3C40) — EP3C120F780

			DQ0B	AD18	USER_DIPSW1
DDR2_DM1	AC15	DIFFIO_B31p/DM4B(x/x/28n)	DIFFIO_B46p(x/x/45n)	AE20	USER_LED1
USER_LED0	AD15	DIFFIO_B31n(x/x/29p)	DIFFIO_B46n/DQ0B	AF20	SRAM_BEn0
USER_LED4	AE15	DIFFIO_B32p(x/x/29n)	PLL1_CLKOUTp	AE5	DDR2BOT_WEn
DDR2_DQ8	AG18	DIFFIO_B37p/DQ4B(x/x/34n)	DIFFIO_B54n/DQ0B(x/40p/51p)	AE24	DDR2BOT_ODT
DDR2_DQ9	AG17	DIFFIO_B33p/DQ4B(x/x/30n)	DIFFIO_B48p/DQ0B(x/x/47n)	AE25	SRAM_WEn
DDR2_DQ10	AH18	DIFFIO_B37n/DQ4B(x/x/35p)	DIFFIO_B48n/DQS0B	AF26	FSA6
FSA23	AE16	DIFFIO_B34p(IO/IO/33n)	DIFFIO_B49p	AG25	FLASH_RDYBSYn
DDR2_DQ11	AH17	DIFFIO_B33n/DQ4B(x/x/31p)	DIFFIO_B49n/DQ0B	AH25	SRAM_WAIT1
DDR2BOT_CSn	AC21	DIFFIO_B55p(x/NC/x)	DIFFIO_B50p(NC/NC/x)	AC19	USER_DIPSW3
DDR2_DQ12	AF15	DIFFIO_B32n/DQ4B(x/x/30p)	DIFFIO_B50n(NC/NC/45p)	AD19	USER_LED3
DDR2_DQ13	AE17	DIFFIO_B36p/DQ4B			
DDR2_DQS1	AF17	DIFFIO_B36n/DQS4B			
			DIFFIO_B52p(x/NC/52n)	AE22	SRAM_BEn2
DDR2_DQ14	AF16	DIFFIO_B34n/DQ4B(IO/IO/32p)	DIFFIO_B52n/DQ0B(x/IO/x)	AF22	FSA5
DDR2_DQ15	AB16	DIFFIO_B35n/DQ4B(x/x/33p)	DIFFIO_B53p(NC/NC/46n)	AB19	SRAM_CSn
USER_LED6	AG19	DIFFIO_B38p(x/x/39n)	DIFFIO_B53n(NC/NC/44p)	AB18	FSA20
DDR2_DM0	AH19	DIFFIO_B38n/DM2B	DIFFIO_B54p(x/NC/IO)	AD25	SRAM_OEn
USER_LED5	AC17	DIFFIO_B39p(x/x/37n)	DIFFIO_B55n(x/NC/IO)	AD21	DDR2BOT_CASn
DDR2_DQ0	AG22	DIFFIO_B42p/DQ2B(x/x/38n)			
DDR2_DQ1	AH21	DIFFIO_B40n/DQ2B(x/x/38p)	DIFFIO_B26p(NC/NC/13n)	Y13	DDR2BOT_A2
DDR2_DQ2	AH22	DIFFIO_B42n/DQ2B(x/x/39p)	DIFFIO_B28n	AH12	DDR2BOT_A8
DDR2_DQS0	AE18	DIFFIO_B41p/DQS2B(x/x/IO)	DIFFIO_B56p(IO/NC/x)	Y19	FSA21
USER_LED2	AF18	DIFFIO_B41n	DIFFIO_B56n(NC/NC/x)	AA19	SRAM_ADVn
DDR2_DQ3	AG21	DIFFIO_B40p/DQ2B	DIFFIO_B6n	AC7	DDR2BOT_A5
DDR2_DQ4	AD17	DIFFIO_B39n/DQ2B(x/x/36p)	DIFFIO_B57n(NC/NC/53p)	AB21	SRAM_BEn3
USER_DIPSW2	AG23	DIFFIO_B43p	DIFFIO_B58p(NC/NC/53n)	AC22	FSA14
DDR2_DQ5	AH23	DIFFIO_B43n/DQ2B(x/x/40p)	DIFFIO_B58n(NC/NC/52p)	AD22	SRAM_CLK
DDR2_DQ6	AE19	DIFFIO_B44p/DQ2B(x/x/40n)	DIFFIO_B59p/DQ0B(x/x/51n)	AG26	FSA9
USER_LED7	AF19	DIFFIO_B44n	DIFFIO_B59n(x/x/IO)	AH26	SRAM_BEn1
DDR2_DQ7	AF24	DIFFIO_B45p/DQ2B			
USER_DIPSW7	AF25	DIFFIO_B45n/DM0B(x/x/42p)			
			IO(x/40n/53p)	AD24	FSA11
			IO(NC/NC/28p)	AB15	USER_DIPSW6
RUP2	AA17	RUP2	IO(NC/NC/56n)	AA21	FLASH_WEn
RDN2	AB17	RDN2			

U20R — Cyclone III, Bank 8B
EP3C120 (EP3C80/EP3C55/EP3C40) — EP3C120F780

MAX2_CLK	D14	DIFFIO_T30p/PADD15	
DDR2_DQ36	D15	DIFFIO_T32p/PADD14/DQ5T	
DDR2_DQS4	D12	DIFFIO_T29p/PADD17/DQS5T	
DDR2TOP_A14	B12	DIFFIO_T27p	
FSD17	G13	DIFFIO_T22n/PADD19	
DDR2_DQ39	D13	DIFFIO_T31p/DQ5T	
FSD22	B11	DIFFIO_T25p/DATA3/DQ5T	
DDR2_DM4	B10	DIFFIO_T23p/DATA4/DM5T	
DDR2_DQ45	B6	DIFFIO_T17p/DATA6/DQ3T	
DDR2_DQ46	H13	DIFFIO_T22p/DATA15/DQ3T	
DDR2_DQ47	D10	DIFFIO_T21p/DQ3T(x/x/15n)	
FSD27	D9	DIFFIO_T14p/DATA8	
DDR2_DM5	A8	DIFFIO_T11n/DATA9/DM3T	
DDR2TOP_A10	A17	DIFFIO_T35n/PADD11	
DDR2TOP_A0	J13	DIFFIO_T24n(NC/NC/VCCIO8)	
SRAM_PSn	B4	DIFFIO_T4p/DATA12/DQS1T	
FSD11	F12	DIFFIO_T20p/DATA13	
DDR2_DQS5	E12	DIFFIO_T20n/DATA14/DQS3T	
DDR2_DQ40	B7	DIFFIO_T18p/DATA5/DQ3T	

U20G — Cyclone III, Bank 7A
EP3C120 (EP3C80 / EP3C55 / EP3C40) — EP3C120F780

DDR2_DQ68	A26	DIFFIO_T59n/DQ0T	DIFFIO_T53n/DQ2T	A22	DDR2_DQ59
DDR2_DM6	E15	DIFFIO_T33p/DM4T(IO/IO/28n)	DIFFIO_T47p	D19	DDR2TOP_BA1
DDR2TOP_A11	D8	DIFFIO_T10p/DQ1T(x/x/IO)	DIFFIO_T45p/PADD6/DQ4T	B19	DDR2_DQ49
			DIFFIO_T48p(29n/NC/16n)	E25	MAX_OEn
DDR2TOP_A7	J16	DIFFIO_T37n(NC/NC/34p)	DIFFIO_T48n(29p/NC/3p)	E24	FSD13
			DIFFIO_T46n/PADD3/DQ4T	C17	DDR2_DQ48
DDR2TOP_BA2	C26	DIFFIO_T61n(x/x/1p)	DIFFIO_T49n/DM2T	C20	DDR2_DM7
DDR2TOP_A4	D7	DIFFIO_T9p/DATA11			
DDR2_DQ54	A19	DIFFIO_T45n/PADD5/DQ4T	DIFFIO_T51n/DQ2T(x/x/42p)	E18	DDR2_DQ63
GND	F17	DIFFIO_T38n(x/NC/x)	DIFFIO_T54p/DQ2T(x/x/45n)	D21	DDR2_DQ62
FSD6	H17	DIFFIO_T39p(NC/NC/x)	DIFFIO_T52p/DQ2T(x/x/42n)	B21	DDR2_DQ61
FSD9	G16	DIFFIO_T39n(30p/NC/x)			
DDR2TOP_BA0	C23	PLL2_CLKOUTn	DIFFIO_T55n/DQ2T	C24	DDR2_DQ60
SEVEN_SEG_MINUS	G19	DIFFIO_T40n(NC/NC/x)	DIFFIO_T52n/DQ2T(x/x/43p)	A21	DDR2_DQ58
			DIFFIO_T54n/DQ2T(x/x/IO)	C22	DDR2_DQ57
FSD10	G22	DIFFIO_T41p(NC/NC/x)	DIFFIO_T34n(NC/NC/IO)	H15	DDR2TOP_A6
FSD14	H21	DIFFIO_T41n(NC/NC/6p)	DQ2T(x/x/44n)	C21	DDR2_DQ56
DDR2_CK_P2	J19	DIFFIO_T42p(NC/NC/x)	DIFFIO_T60n/DQ0T(x/x/52p)	D22	DDR2_DQ71
DDR2_CK_N2	H19	DIFFIO_T42n(NC/NC/x)	DIFFIO_T56p/DM0T	B23	DDR2_DM8
GND	G21	DIFFIO_T43p(NC/NC/IO)	DIFFIO_T61p/DQ0T(x/x/52n)	B26	DDR2_DQ70
USER_DIPSW5	G20	DIFFIO_T43n(NC/NC/50p)	DIFFIO_T9n/DATA10/DQ1T	C7	DDR2TOP_CSn
			DIFFIO_T58p/DQ0T(x/x/48n)	F21	DDR2_DQ69
			DIFFIO_T23n/PADD18	A10	DDR2TOP_WEn
FSD2	J17	IO(NC/NC/33n)	DIFFIO_T59p/DQS0T	A25	DDR2_DQS8
			DQ0T	B25	DDR2_DQ67
			DIFFIO_T56n/DQ0T(x/x/IO)	A23	DDR2_DQ66
RUP4	F19	RUP4	DIFFIO_T57p/DQ0T	C25	DDR2_DQ65
RDN4	E19	RDN4	DIFFIO_T60p/DQ0T(x/x/51n)	E22	DDR2_DQ64
			DIFFIO_T36p/PADD10	D16	DDR2TOP_A9

U20Q — Cyclone III, Bank 7B
EP3C120 (EP3C80/EP3C55/EP3C40) — EP3C120F780

FSD23	B22	DIFFIO_T53p/PADD0	
FSD7	C18	DIFFIO_T50n/PADD1	
FSD8	D18	DIFFIO_T50p/PADD2	
DDR2_DQ50	B18	DIFFIO_T44p/PADD8/DQ4T	
DDR2_DQS7	D17	DIFFIO_T46p/PADD4/DQS2T	
DDR2_DQ51	C19	DIFFIO_T47n/DQ4T(x/x/39p)	
DDR2_DQ52	D20	DIFFIO_T49p/DQ4T(x/x/39n)	
FSD24	A18	DIFFIO_T44n/PADD7	
DDR2_DQ53	C16	DIFFIO_T36n/PADD9/DQ4T	
DDR2_DQ55	E17	DIFFIO_T38p/DQ4T(IO/IO/34n)	
DDR2TOP_A15	H16	DIFFIO_T37p(NC/NC/x)	
DDR2TOP_A1	G18	DIFFIO_T40p(x/NC/x)	
DDR2_DQS6	B17	DIFFIO_T35p/PADD12/DQS4T	
MAX_WEn	C15	DIFFIO_T32n/PADD13	
DDR2_DQ32	A12	DIFFIO_T27n/DQ5T	

U20H — Cyclone III, Bank 8A
EP3C120 (EP3C80 / EP3C55 / EP3C40) — EP3C120F780

FSD5	C6	DQ1T(x/x/2p)			
SEVEN_SEG_E	E5	DIFFIO_T1p(4n/NC/x)	DIFFIO_T15p(x/x/IO)	D11	FSD12
SEVEN_SEG_SEL3	E4	DIFFIO_T1n(IO/IO/x)	DIFFIO_T16p(NC/NC/21n)	H12	DDR2_CK_P1
SEVEN_SEG_D	D4	DIFFIO_T2p/DM1T(x/x/IO)	DIFFIO_T16n(NC/NC/x)	G11	DDR2_CK_N1
SEVEN_SEG_C	C4	DIFFIO_T2n/DQ1T(x/x/1p)	DIFFIO_T34p(NC/NC/VCCIO7)	J15	DDR2TOP_A5
SEVEN_SEG_B	A3	DIFFIO_T3p/DQ1T(x/x/2n)			
SEVEN_SEG_SEL1	B3	DIFFIO_T3n	DIFFIO_T19n/DQ3T	E11	DDR2_DQ44
FSD16	A4	DIFFIO_T4n/DQ1T	DIFFIO_T21n/DQ3T(x/x/17p)	C10	DDR2_DQ43
FSD21	F7	DIFFIO_T5p(NC/NC/x)			
FSD3	G7	DIFFIO_T5n(NC/NC/x)	DIFFIO_T18n/DQ3T	A7	DDR2_DQ42
DDR2TOP_ODT	A6	DIFFIO_T17n	DIFFIO_T15n/DATA7/DQ3T	C11	DDR2_DQ41
FSD25	G8	DIFFIO_T6n(NC/NC/IO)			
DDR2TOP_A12	D25	DIFFIO_T57n	DIFFIO_T24p(NC/NC/x)	J12	FSD26
DDR2TOP_RASn	F8	DIFFIO_T7p(x/NC/9n)			
			DIFFIO_T26p/DQ5T(x/x/IO)	E14	DDR2_DQ38
FSD1	D6	DIFFIO_T8p/DQ1T(IO/4n/IO)	DIFFIO_T58n(x/x/46p)	E21	DDR2TOP_CKE
FSD29	E7	DIFFIO_T8n(4p/NC/13p)	DIFFIO_T26n(x/x/22p)	F14	DDR2TOP_CASn
			DIFFIO_T29n/PADD16/DQ5T	C12	DDR2_DQ37
DDR2TOP_A8	H8	DIFFIO_T6p(NC/NC/1n)	DIFFIO_T28p(NC/NC/x)	J14	FSD0
FSD20	C8	DIFFIO_T10n/DQ1T(x/x/5p)	DIFFIO_T28n(NC/NC/x)	H14	FSD18
FSD19	B8	DIFFIO_T11p(x/x/17n)			
			DIFFIO_T31n/DQ5T	C13	DDR2_DQ35
FSD31	J10	DIFFIO_T12p(NC/NC/x)	DIFFIO_T25n/DATA2/DQ5T	A11	DDR2_DQ34
FSD30	H10	DIFFIO_T12n(NC/NC/7p)	DIFFIO_T30n/DQ5T	C14	DDR2_DQ33
GND	G10	DIFFIO_T13p(NC/NC/x)			
GND	F10	DIFFIO_T13n(6p/NC/15p)	IO(NC/NC/x)	C3	SEVEN_SEG_SEL4
			IO(6n/NC/13n)	E10	DDR2TOP_ACTIVE
FSD28	C9	DIFFIO_T14n/DQ3T			

1.8V_B3_B4

R195	49.9	RUP2
R196	49.9	RDN2

1.8V_B7_B8

R145	49.9	RUP4
R146	49.9	RDN4

SEVEN-SEG INTERFACE

SEVEN_SEG_SEL[4:1]	SEVEN_SEG_SEL[4:1]	7,16
SEVEN_SEG_A	SEVEN_SEG_A	16
SEVEN_SEG_B	SEVEN_SEG_B	16
SEVEN_SEG_C	SEVEN_SEG_C	16
SEVEN_SEG_D	SEVEN_SEG_D	16
SEVEN_SEG_E	SEVEN_SEG_E	16
SEVEN_SEG_G	SEVEN_SEG_G	16
SEVEN_SEG_MINUS	SEVEN_SEG_MINUS	16
SEVEN_SEG_DP	SEVEN_SEG_DP	16

MAX_OEn	MAX_OEn	8
MAX_WEn	MAX_WEn	8
MAX2_CLK	MAX2_CLK	8

SHARED BUS

FSD[31:0]	FSD[31:0]	6,8,11
FSA[24:0]	FSA[24:0]	7,8,11

FLASH INTERFACE

FLASH_WEn	FLASH_WEn	8,11
FLASH_RDYBSYn	FLASH_RDYBSYn	8,11

DDR2 INTERFACE

DDR2BOT_A[15:0]	DDR2BOT_A[15:0]	7,9,10
DDR2BOT_BA[2:0]	DDR2BOT_BA[2:0]	9,10
DDR2TOP_A[15:0]	DDR2TOP_A[15:0]	6,7,9,10
DDR2TOP_BA[2:0]	DDR2TOP_BA[2:0]	9,10
DDR2BOT_CASn	DDR2BOT_CASn	9,10
DDR2BOT_WEn	DDR2BOT_WEn	9,10
DDR2BOT_CSn	DDR2BOT_CSn	9,10
DDR2BOT_ODT	DDR2BOT_ODT	9,10
DDR2BOT_CKE	DDR2BOT_CKE	9,10
DDR2TOP_RASn	DDR2TOP_RASn	9,10
DDR2TOP_CASn	DDR2TOP_CASn	9,10
DDR2TOP_WEn	DDR2TOP_WEn	9,10
DDR2TOP_CSn	DDR2TOP_CSn	9,10
DDR2TOP_ODT	DDR2TOP_ODT	9,10
DDR2TOP_CKE	DDR2TOP_CKE	9,10
DDR2TOP_ACTIVE	DDR2TOP_ACTIVE	9
DDR2_CK_P[2:0]	DDR2_CK_P[2:0]	9
DDR2_CK_N[2:0]	DDR2_CK_N[2:0]	9
DDR2_DM[8:0]	DDR2_DM[8:0]	9,10
DDR2_DQ[71:0]	DDR2_DQ[71:0]	9,10
DDR2_DQS[8:0]	DDR2_DQS[8:0]	9,10

PSRAM INTERFACE

SRAM_BEn[3:0]	SRAM_BEn[3:0]	11
SRAM_CLK	SRAM_CLK	11
SRAM_CSn	SRAM_CSn	8,11
SRAM_ADVn	SRAM_ADVn	11
SRAM_OEn	SRAM_OEn	11
SRAM_PSn	SRAM_PSn	11
SRAM_WAIT0	SRAM_WAIT0	7,11
SRAM_WAIT1	SRAM_WAIT1	11
SRAM_WEn	SRAM_WEn	11

USER I/O's

USER_PB[3:0]	USER_PB[3:0]	6,16
USER_DIPSW[7:0]	USER_DIPSW[7:0]	16
USER_LED[7:0]	USER_LED[7:0]	16

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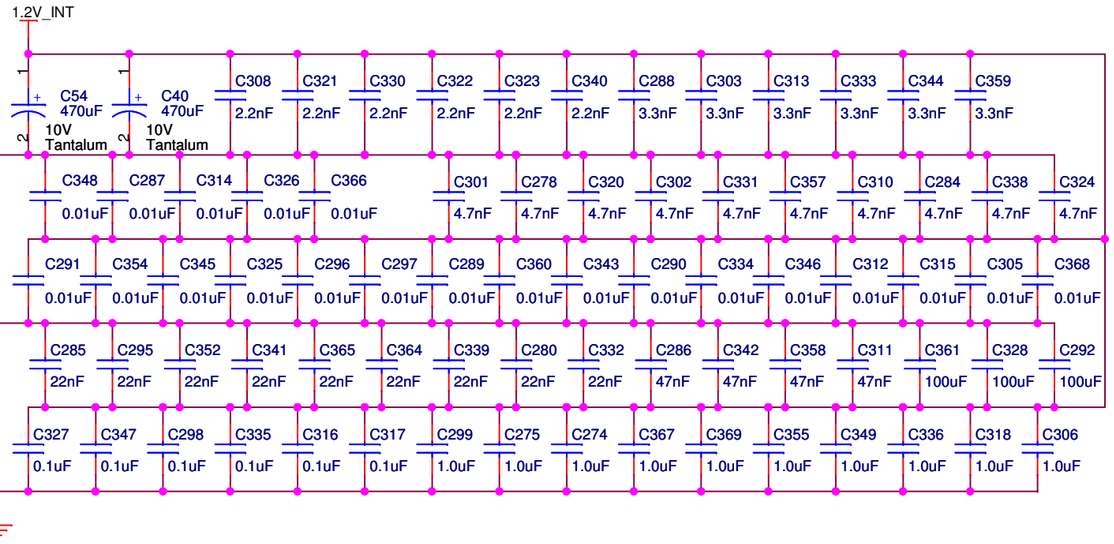
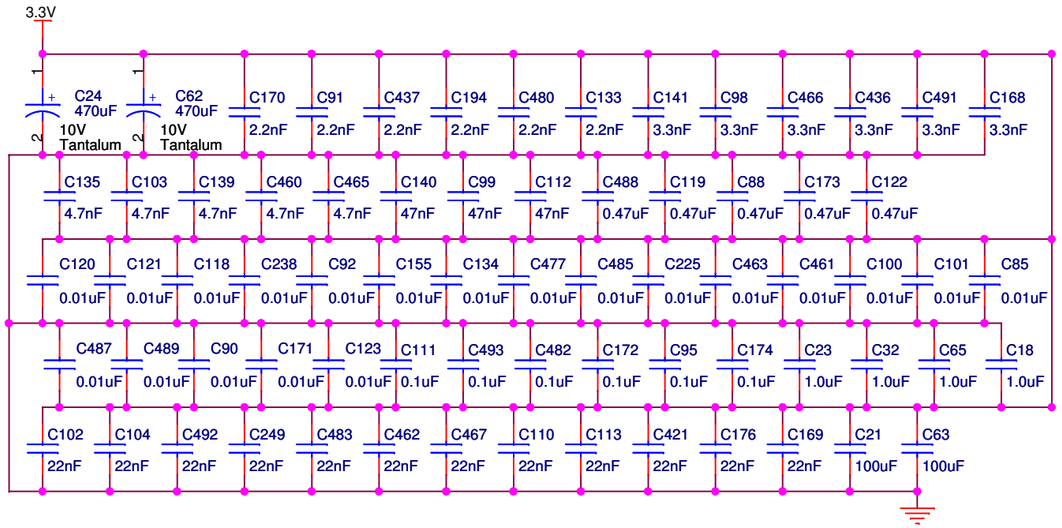
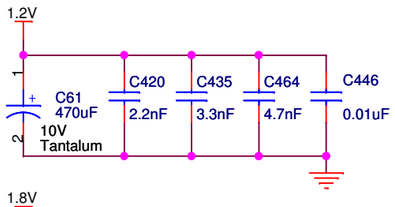
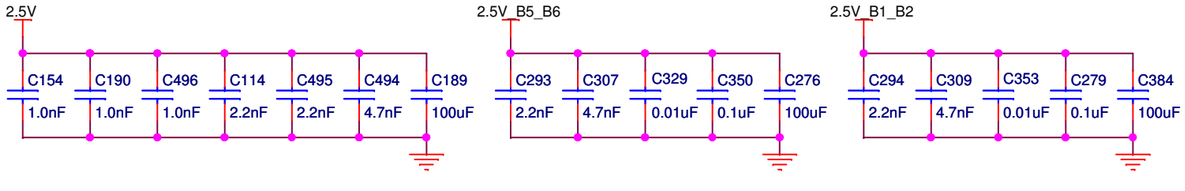
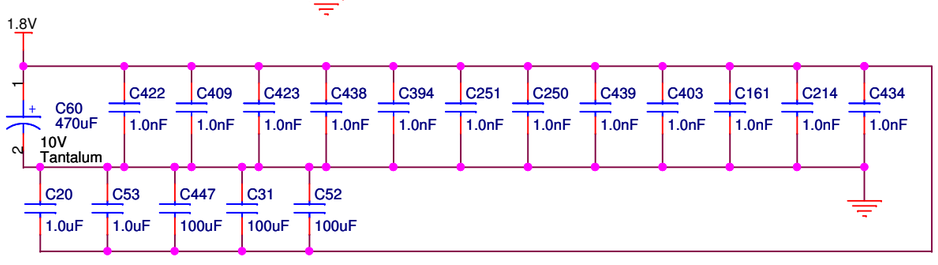
Decoupling

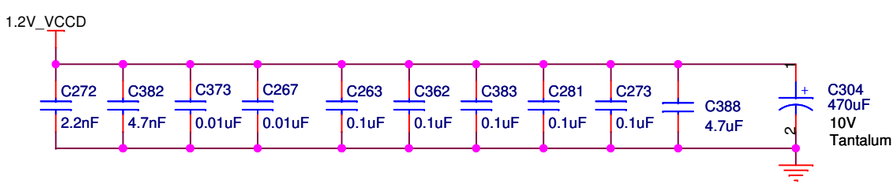


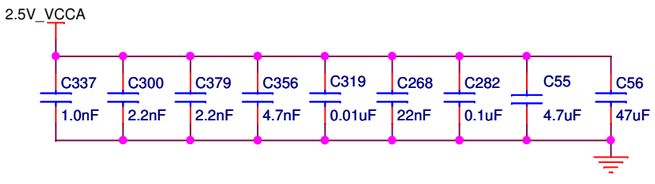


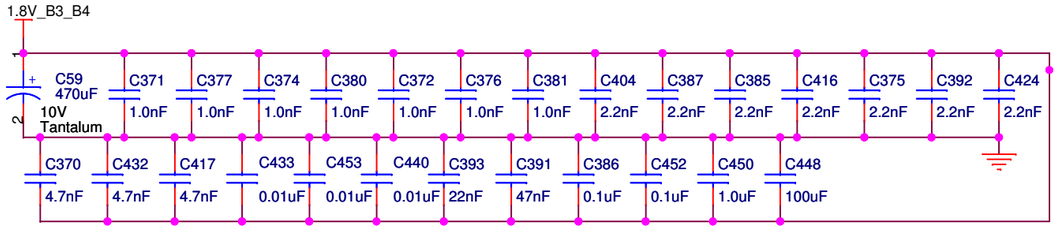


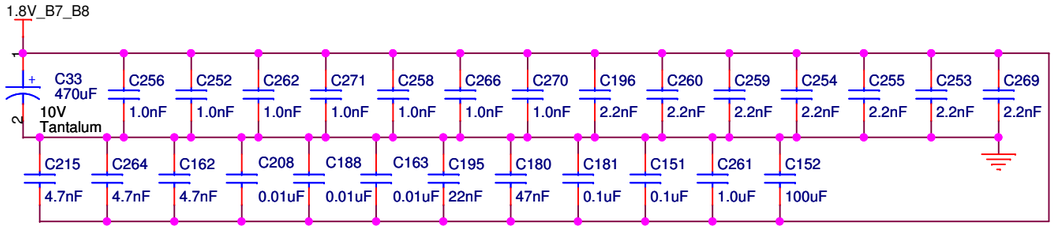












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