

Altera IP

Release Notes

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These release notes include versions 14.1, 14.0 Arria® 10 Edition, 14.0, 13.1 Arria 10 Edition, and 13.1 of Altera® IP cores, including the Altera MegaCore IP Library IP and other IP cores.

Related Information

- [Introduction to Altera IP Cores](#)
- [Altera Software Installation and Licensing](#)

Errata

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

For full information on errata and the versions affected by errata, refer to the Knowledge Base page of the Altera website.

Related Information

[Altera Knowledge Base](#)

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1G/10GbE and Backplane Ethernet 10GBASE-KR PHY Revision History

2

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1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP Core v14.0 Revision History

Table 2-1: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for 1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP Core v13.1 Revision History

Table 2-2: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for 1G/10GbE and Backplane Ethernet 10GBASE-KR PHY IP core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

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10-Gbps Ethernet (10GbE) MAC Revision History

3

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10-Gbps Ethernet (10GbE) MAC v14.0

Table 3-1: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added support for clause 66 of IEEE 802.3—synthesis option.	This change is optional. If you do not upgrade your IP core, it does not have this new feature.

Related Information

- [Introduction to Altera IP Cores](#)
- [10-Gbps Ethernet \(10GbE\) MAC MegaCore Function User Guide](#)
- [Errata for 10-Gbps Ethernet \(10GbE\) MAC MegaCore Function in the Knowledge Base](#)

10-Gbps Ethernet (10GbE) MAC v13.1

Table 3-2: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none">• Arria GX• HardCopy IV GX• Stratix II GX	-
Removed 1G/10GbE MAC and 10M-10GbE MAC with IEEE 1588v2 design examples from the directory.	-

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Description	Impact
The 10GbE MAC with 10GBASE-R PHY and IEEE 1588v2 configuration supports only Arria V GT device with speed grade 3_H3.	-
Increased the width for path delay interface signals such as tx_path_delay_10g_data (16 bits), tx_path_delay_1g_data (22 bits), rx_path_delay_10g_data (16 bits), and rx_path_delay_1g_data (22 bits)	-

Related Information

- [Introduction to Altera IP Cores](#)
- [10-Gbps Ethernet \(10GbE\) MAC MegaCore Function User Guide](#)
- [Errata for 10-Gbps Ethernet \(10GbE\) MAC MegaCore Function in the Knowledge Base](#)

10GBASE-R PHY IP Core v14.1 Revision History

Table 4-1: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for 10GBASE-R PHY in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

10GBASE-R PHY IP Core v14.0 Revision History

Table 4-2: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added OpenCore Plus evaluation feature support for IEEE 1588 Precision Time Protocol.	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for 10GBASE-R PHY in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

10GBASE-R PHY IP Core v13.1 Revision History

Table 4-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for 10GBASE-R PHY in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core Revision History

5

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40- and 100-Gbps Ethernet MAC and PHY IP Core v14.1

Table 5-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1		

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0 Update 2

Table 5-2: Version 14.0 Update 2 September 2014

Description	Impact	Notes
Fixed an issue in which incoming runt Ethernet packets of size one byte to eight bytes caused the 40GbE IP core to hang instead of handling the error.	If you upgrade to version 14.0 Update 2 of the Quartus II software, you must upgrade your 40-100GbE IP core to incorporate this fix. The fix has no effect on 100GbE IP cores, which did not have the issue. However, the previous versions of the 40-100GbE IP core require upgrade with the Quartus II software.	

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

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40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0

Table 5-3: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	Upgrading your IP core for this change is optional.	
Added OpenCore Plus support for 40GBASE-KR4 variations.	Upgrading your IP core for this change is optional.	

Related Information

- [Introduction to Altera IP Cores](#)
- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v13.1

Table 5-4: Version 13.1 November 2013

Description	Impact	Notes
Added 40GBASE-KR4 option with FEC and with auto-negotiation and link training mode options.		
Added Synchronous Ethernet clock support option in Stratix V devices. The option separates the TX PLL and RX CDR input reference clocks (<code>tx_ref_clk</code> and <code>rx_ref_clk</code> signals replace <code>ref_clk</code> for these variations) and exposes the RX recovered clock.		
Exposed link fault signals <code>remote_fault_status</code> and <code>local_fault_status</code> in duplex variations.		
Exposed PHY status signals <code>tx_lanes_stable</code> and <code>lanes_deskewed</code> in MAC&PHY variations.		
Updated and simplified the example design and testbench. The testbench stimulus is simpler and the user no longer needs to configure the DUT with a specific name and clock rate.		

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v13.0

Table 5-5: Version 13.0 May 2013

Description	Impact	Notes
Added preamble pass-through option.		
Added transmitter average inter-packet gap (IPG) adjustment option.		

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v12.1

Table 5-6: Version 12.1 November 2012

Description	Impact	Notes
Verified with the Quartus II software v12.1.		

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

50G Interlaken IP Core v14.1

Table 6-1: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	IYou must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Information

- [50G Interlaken MegaCore Function User Guide](#)
- [Errata for 50G Interlaken IP core in the Knowledge Base](#)

50G Interlaken IP Core v14.0 Arria 10 Edition

Table 6-2: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition.		

Related Information

- [50G Interlaken MegaCore Function User Guide](#)
- [Errata for 50G Interlaken IP core in the Knowledge Base](#)

50G Interlaken IP Core v14.0

Table 6-3: Version 14.0 June 2014

Description	Impact	Notes
New required frequency for input clock signals <code>tx_usr_clk</code> and <code>rx_usr_clk</code> is 250 MHz, and the two clocks must be driven at the same frequency. If you provide a clock with a different frequency, it must be in the range of 200 MHz to 300 MHz, and you must modify the new hidden (RTL) parameter <code>TX_USR_CLK_MHZ</code> to the new value in the files <code><instance_name>/ilk_core_50g.sv</code> for synthesis and <code><instance_name>_sim/ilk_core_50g.sv</code> for simulation.		
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .		
Improved resource utilization by 20% and latency by 55%.		

Related Information

- [Introduction to Altera IP Cores](#)
- [50G Interlaken MegaCore Function User Guide](#)
- [Errata for 50G Interlaken IP core in the Knowledge Base](#)

50G Interlaken IP Core v13.1 Arria 10 Edition

Table 6-4: Version 13.1 Arria 10 Edition December 2013

Description	Impact	Notes
Added support for Arria 10 devices. IP core variations that target an Arria 10 device have additional interfaces and design requirements.		

Table 6-5: 50G Interlaken IP Core Signal Changes

Signals added or modified in version 13.1 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	<code>tx_serial_clk</code>	New interface to external TX PLL. Relevant for Arria 10 variations only.
—	<code>tx_pll_locked</code>	
—	<code>tx_pll_powerdown</code>	
—	<code>tx_cal_busy</code>	

Old Signal Name	New Signal Name	Notes
—	reconfig_clk	New Arria 10 transceiver reconfiguration interface. Relevant for Arria 10 variations only.
—	reconfig_reset	
—	reconfig_read	
—	reconfig_write	
—	reconfig_address[12:0]	
—	reconfig_readdata[31:0]	
—	reconfig_waitrequest	
—	reconfig_writedata[31:0]	Transceiver reconfiguration interface for Arria V and Stratix V variations. This interface is present only in Arria V and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_to_xcvr	Not present in Arria 10 variations.	
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Information

- [50G Interlaken MegaCore Function User Guide](#)
- [Errata for 50G Interlaken IP core in the Knowledge Base](#)

50G Interlaken IP Core v13.1

Table 6-6: Version 13.1 November 2013

Description	Impact	Notes
Verified in the Quartus II software v13.1.		

Related Information

- [50G Interlaken MegaCore Function User Guide](#)
- [Errata for 50G Interlaken IP core in the Knowledge Base](#)

50G Interlaken IP Core v13.0

Table 6-7: Version 13.0 May 2013

Description	Impact	Notes
Initial release.		

Related Information

- [50G Interlaken MegaCore Function User Guide](#)
- [Errata for 50G Interlaken IP core in the Knowledge Base](#)

100G Interlaken IP Core v14.1

Table 7-1: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Information

- [100G Interlaken MegaCore Function User Guide](#)
- [Errata for 100G Interlaken IP core in the Knowledge Base](#)

100G Interlaken IP Core v14.0 Arria 10 Edition

Table 7-2: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition.		

Related Information

- [100G Interlaken MegaCore Function User Guide](#)
- [Errata for 100G Interlaken IP core in the Knowledge Base](#)

100G Interlaken IP Core v14.0

Table 7-3: Version 14.0 June 2014

Description	Impact	Notes
Removed <code>mm_clk_locked</code> input signal.	Port change.	
Removed hidden parameter <code>CNTR_BITS</code> from top level RTL files.		
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .		

Related Information

- [Introduction to Altera IP Cores](#)
- [100G Interlaken MegaCore Function User Guide](#)
- [Errata for 100G Interlaken IP core in the Knowledge Base](#)

100G Interlaken IP Core v13.1 Arria 10 Edition

Table 7-4: Version 13.1 Arria 10 Edition December 2013

Description	Impact	Notes
Added support for Arria 10 devices. IP core variations that target an Arria 10 device have additional interfaces and design requirements.		

Table 7-5: 100G Interlaken IP Core Signal Changes

Signals added or modified in version 13.1 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	<code>tx_serial_clk</code>	New interface to external TX PLL. Relevant for Arria 10 variations only.
—	<code>tx_pll_locked</code>	
—	<code>tx_pll_powerdown</code>	
—	<code>tx_cal_busy</code>	

Old Signal Name	New Signal Name	Notes
—	reconfig_clk	New Arria 10 transceiver reconfiguration interface. Relevant for Arria 10 variations only.
—	reconfig_reset	
—	reconfig_read	
—	reconfig_write	
—	reconfig_address[13:0] or reconfig_address[14:0]	
—	reconfig_readdata[31:0]	
—	reconfig_waitrequest	
—	reconfig_writedata[31:0]	Transceiver reconfiguration interface for Arria V and Stratix V variations. This interface is present only in Arria V and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_to_xcvr	Not present in Arria 10 variations.	
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Information

- [100G Interlaken MegaCore Function User Guide](#)
- [Errata for 100G Interlaken IP core in the Knowledge Base](#)

100G Interlaken IP Core v13.1

Table 7-6: Version 13.1 November 2013

Description	Impact	Notes
Added optional ECC feature on M20K blocks in Stratix V devices.		
Added bit error injection testing feature to check CRC24 error detection.		
Changed implementation of single segment mode: <ul style="list-style-type: none"> • Changed parameter name from Received data format to Data format. • If you select Single segment mode, the IP core can no longer handle incoming dual segment traffic on the TX client data interface. 		

Description	Impact	Notes
Added four new parameters to optionally include advanced error reporting and handling, Stratix V M20K block ECC feature, diagnostic features, and in-band flow control functionality. Excluding the features improves resource utilization.		
Changed the behavior of the management interface during read operations. The IP core asserts the <code>mm_rddata_valid</code> signal two <code>mm_clk</code> cycles after the <code>mm_read</code> signal is asserted, instead of one <code>mm_clk</code> cycle as in previous versions of the IP core.		

Related Information

- [100G Interlaken MegaCore Function User Guide](#)
- [Errata for 100G Interlaken IP core in the Knowledge Base](#)

100G Interlaken IP Core v13.0

Table 7-7: Version 13.0 May 2013

Description	Impact	Notes
Added dual segment mode.		
Added packet mode option in parameter editor.		
Improved error handling.		
Added PRBS capability.		
Added CRC-32 error injection capability.		

Related Information

- [100G Interlaken MegaCore Function User Guide](#)
- [Errata for 100G Interlaken IP core in the Knowledge Base](#)

Arria V GZ Hard IP for PCI Express IP Core Revision History

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Arria V Hard IP for PCI Express IP Core v14.1

Table 8-1: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- [Introduction to Altera IP Cores](#)
- [Arria V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Arria V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Arria V Hard IP for PCI Express in the Knowledge Base](#)

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Arria V GZ Hard IP for PCI Express IP Core v14.0

Table 8-2: v14.0 June 2014

Description	Impact
<p>Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core):</p> <ul style="list-style-type: none"> • Revised programming model and optimized the performance of the Descriptor Controller. • Added support for either 128- or 256-bit interface to the Application Layer. • Added support for 64-bit addressing, making address translation unnecessary. • Added support for optional bursting RX Master for BAR2. • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. • Due to the many changes, the support level has reverted to preliminary. 	<p>The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to the 14.0 version. Altera will no longer support the 13.1 version</p>
<p>Made the following changes to the Avalon-MM Arria V GZ Hard IP for PCI Express IP core :</p> <ul style="list-style-type: none"> • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. • Added support for 64-bit addressing, making address translation unnecessary. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM. • Increased CRA address to 14 bits from 12 bits. 	<p>All of these new features are optional. If you choose to include an optional feature that changes the port signature of your IP core, you must regenerate your design and connect the signals.</p>
<p>Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i></p>	

Related Information

- [Introduction to Altera IP Cores](#)
- [Arria V GZ Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Arria V GZ Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Arria V GZ Hard IP for PCI Express in the Knowledge Base](#)

Arria V GZ Hard IP for PCI Express IP Core v13.1

Table 8-3: v13.1 November 2013

Description	Impact
Support for Avalon-MM 256-Bit Hard IP for PCI Express Gen3 ×8 with DMA is final.	-
Support for Gen2 CvP is removed.	

Related Information

- [Introduction to Altera IP Cores](#)
- [Arria V GZ Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Arria V GZ Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Arria V GZ Hard IP for PCI Express in the Knowledge Base](#)

Arria V Hard IP for PCI Express IP Core Revision History

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Arria V Hard IP for PCI Express IP Core v14.1

Table 9-1: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- [Introduction to Altera IP Cores](#)
- [Arria V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Arria V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Arria V Hard IP for PCI Express in the Knowledge Base](#)

Arria V Hard IP for PCI Express IP Core v14.0

Table 9-2: v14.0 June 2014

Description	Impact
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Upgraded Arria V Hard IP for PCI Express IP core to support the new IP Catalog.	-
Added support for new, V-Series PCIe with Avalon-MM DMA Interface IP Core.	-

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Description	Impact
<p>Arria V Avalon-MM Hard IP for PCI Express IP core. :</p> <ul style="list-style-type: none"> Added access to selected Configuration Space and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. 	<p>All of these new features are optional. If you include either the hard IP status bus or status extension bus in your design, you must regenerate your design and connect the new bus</p>

Related Information

- [Introduction to Altera IP Cores](#)
- [Arria V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Arria V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Arria V Hard IP for PCI Express in the Knowledge Base](#)

Arria V Hard IP for PCI Express IP Core v13.1

Table 9-3: v13.1 November 2013

Description	Impact
Added support for Gen2 Configuration via Protocol (CvP) using an .ini file. Contact your sales representative for more information.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Arria V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Arria V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Arria V Hard IP for PCI Express in the Knowledge Base](#)

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Revision History 10

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Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v14.1 Revision History

Table 10-1: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v14.0 Revision History

Table 10-2: v14.0 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Removed the following parameters from the Link Training tab: <ul style="list-style-type: none">• Enable daisy chain mode.• Enable microprocessor interface.	-

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Description	Impact
<p>Changed the default values of the following PMA parameters under the Link Training tab:</p> <ul style="list-style-type: none"> • VMAXRULE • VMINRULE • VODMINRULE • VPOSTRULE • VPRERULE • PREMAINVAL • INITMAINVAL • INITPOSTVAL • INITPREVAL 	-
Changed Avalon Memory-Mapped (AVMM) clock frequency from 125 MHz to 161 MHz to support NIOS II. The AVMM slave interface provides access to the IP core registers.	-
IEEE 1588 Precision Time Protocols are not supported in backplane applications.	-
Link Training takes more time in simulation as NIOS command processing is slower.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v13.1 Revision History

Table 10-3: v13.1 December 2013

Description	Impact
Initial release	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 External Memory Interface IP Revision History 11

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Arria 10 External Memory Interface IP 14.1

Table 11-1: v14.1 December 2014

Description	Impact
Several new features are added in v14.1: <ul style="list-style-type: none">• Support for the QDR-IV memory protocol.• Ping Pong PHY support for DDR3 and DDR4.• Compact pin placement for x4 groups for DDR3 and DDR4.• Simulation, compilation, and timing closure support for DDR4 RDIMMs.• Compilation and timing closure support for DDR3 RDIMMs, and LRDIMMs, and DDR4 LRDIMMs.• Half-rate controller and PHY support for quarter-rate DDR3 and DDR4 interfaces.	-
DDR3 and DDR4 interfaces with x4 groups are now generated with two DQS groups per I/O lane. In previous releases, interfaces with x4 groups required one I/O lane per DQS group, causing inefficient I/O pin usage. (For devices with a name prefixed with 10AX090, 10AX115, 10AT090, or 10AT115, x4 support is available only for ES2 and newer silicon revisions. For other devices, x4 support is available for all silicon revisions including ES.)	v14.1 allows more compact pin placement.
For quarter-rate DDR3 and DDR4 interfaces using hard memory controller, the hard memory controller and the PHY can now run at half-rate (that is, at 2x the frequency of user clock domain). This feature is enabled automatically for interfaces and FPGA devices that can support it. In previous releases, the hard memory controller and the PHY always ran at quarter-rate for quarter-rate interfaces.	Running at half-rate allows better efficiency and improved latency.
In PHY-only mode for multi-rank interfaces, new signals <code>afi_rrank</code> and <code>afi_wrack</code> have been introduced for shadow register selection.	Shadow registers now are supported for Arria 10.

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Description	Impact
DDR4 3DS / ChipID is not supported by Arria 10. The option to use it has been removed.	Option is no longer available.

Related Information

[External Memory Interface Handbook](#)

Arria 10 External Memory Interface IP 14.0 Arria 10 Edition

Table 11-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for QDR II/II+/II+ Xtreme and RLDRAM 3.	-
Added I/O and Diagnostics Settings tab to the parameter editor for DDR3 and DDR4.	-
Added optional signal <code>mem_alert_n</code> , which is enabled by default for DDR4. This port is used to enable address and command deskew for calibration.	-
Added support for PHY-only mode for DDR3 and DDR4.	-
Added error correction code (ECC) and memory-mapped configuration and status register (MMR) support for DDR3 and DDR4.	-

Related Information

[External Memory Interface Handbook](#)

Arria 10 External Memory Interface IP 13.0 Arria 10 Edition

Table 11-3: v13.0 Arria 10 Edition December 2013

Description	Impact
Initial release.	-

Related Information

[External Memory Interface Handbook](#)

Arria 10 FPLL IP Core Revision History 12

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Arria 10 FPLL IP Core Revision History v14.1 Revision History

Table 12-1: v14.1 December 2014

Description	Impact
Changed the default FPLL Mode to Transceiver TX PLL.	-
FPLL does not allow the bandwidth setting of "high" in fractional mode.	
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 FPLL IP Core Revision History v14.0 Revision History

Table 12-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

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Description	Impact
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the Dynamic Reconfiguration tab.	-
Changed the FPLL Parameter Editor graphic user interface (GUI) to show the available FPLL modes. You can use the FPLL in the following three modes: <ul style="list-style-type: none"> Core Cascade Source Transceiver 	-
Removed the option for automatic bandwidth setting. The following bandwidth settings are available: <ul style="list-style-type: none"> Low Medium High 	-
Enhanced user warnings and information messages.	-
The fPLL IP in 13.1 Arria 10 edition, allowed simultaneous selection of FPLL to be used in core and transceiver PLL modes. However, in the FPLL IP in 14.0 Arria 10 edition, only one mode (transceiver PLL or core PLL) can be selected at a time. If you have selected both (transceiver PLL and core PLL) modes in 13.1 Arria 10 edition, then FPLL IP will fail automatic upgrade for 14.0 Arria 10 edition. In this case, you will have to manually upgrade the FPLL IP after selecting one legal FPLL usage mode.	-
The Master Clock Generation Block tab in IP Parameter Editor is not visible when "Core" is selected as the FPLL mode. The Master Clock Generation Block tab appears only when "Transceiver" is selected as the FPLL mode.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 FPLL IP Core Revision History v13.1 Revision History

Table 12-3: v13.1 Arria 10 Edition

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Hard IP for PCI Express IP Core Function

Revision History

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Arria 10 Hard IP for PCI Express IP Core Function v14.1

Table 13-1: 14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.
Added support for Single-Root I/O Virtualization (SR-IOV) interface.	If you choose to use the SR-IOV interface, you will need to redesign your Application Layer.
Added support for dynamically generated Qsys example designs that reflects the parameters that you selected in the Parameter Editor.	If you choose the Avalon-ST interface, the automatically generated testbench has the parameters that you specified.
Added support for Configuration Space Bypass Mode when using the Avalon-ST interface.	If you choose to use Configuration Space Bypass Mode, you will need to redesign your Application Layer.
Added Quartus II compilation support for the Avalon-MM with DMA interface.	You can now compile for the Avalon-MM with DMA interface and download the Programmer Object File .pof to a development board.
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	If you generate your IP core outside a Quartus II project, you must ensure that you specify a device for your Arria 10 IP core variation and regenerate it in the Quartus II software v14.1.

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Related Information

- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface](#)
- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface](#)
- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface](#)
- [Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base](#)

Arria 10 Hard IP for PCI Express IP Core Function v14.0 Arria 10 Edition

Table 13-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Changed the PIPE interface to 32 bits for all data rates.	This change requires you to recompile your v13.1 variant in 14.0a10 release
Added simulation log file, <code>altpcie_monitor_<dev>_dlhip_tlp_file_log.log</code> in your simulation directory. Generation of the log file requires the following simulation file, <code><install_dir>altera/altera_pcie/altera_pcie_a10_hip/altpcie_monitor_a10_dlhip_sim.sv</code> , that was not present in earlier releases of the Quartus II software.	
Added option to enable 62.5 MHz application clock for Gen1 x1 data rate.	If you choose this option, you must regenerate your IP core.
Added third interface option, Avalon-MM with DMA, that includes a high performance DMA. If you choose this option, you must regenerate your IP core.	
Added option to integrate the Descriptor Controller in the variant for the Avalon-MM with DMA interface.	-

Related Information

- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface](#)
- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface](#)
- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface](#)
- [Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base](#)

Arria 10 Hard IP for PCI Express IP Core Function v13.1 Arria 10 Edition

Table 13-3: v13.1 Arria 10 Edition December 2013

Description	Impact
Initial release.	-

Related Information

- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Streaming Interface](#)
- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface](#)
- [Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped DMA Interface](#)
- [Errata for the Arria 10 Hard IP for PCI Express MegaCore Function in the Knowledge Base](#)

Arria 10 Transceiver ATX PLL IP Core Revision History 14

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Arria 10 Transceiver ATX PLL IP Core v14.1 Revision History

Table 14-1: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1.	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver ATX PLL IP Core v14.0 Revision History

Table 14-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added support for fractional mode. Fractional mode provides support for a wider range of output frequencies than integer mode. This feature is available under the Output Frequency tab.	-

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Description	Impact
Added support for Embedded Debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the Dynamic Reconfiguration tab.	-
Added the following presets for GT and GX modes: <ul style="list-style-type: none"> • GT 25781.25 Mbps Single Channel • GX 2500 Mbps Bonded • GX 2500 Mbps Single Channel • GX 2500 Mbps xN Non-Bonded 	-
Changed the documentation link in IP Parameter Editor to refer to the <i>Arria 10 Transceiver PHY User Guide</i> .	-
Enhanced user warnings and information messages.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver ATX PLL IP Core v13.1 Revision History

Table 14-3: v13.1 Arria 10 Edition December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver CMU PLL IP Core Revision History 15

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Arria 10 Transceiver CMU PLL IP Core v14.1 Revision History

Table 15-1: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver CMU PLL IP Core v14.0 Revision History

Table 15-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the Dynamic Reconfiguration tab.	-
Added preset GX 2500 Mbps Single Channel for GX mode.	-

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Description	Impact
Changed the IP core to expose the <code>pll_cal_busy</code> port to the top level.	-
Changed the documentation link in IP Parameter Editor to refer to the <i>Arria 10 Transceiver PHY User Guide</i> .	-
Enhanced user warnings and information messages.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver CMU PLL IP Core v13.1 Revision History

Table 15-3: v13.1 Arria 10 Edition December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver Native PHY IP Core Revision History 16

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Arria 10 Transceiver Native PHY IP Core v14.1 Revision History

Table 16-1: 14.1 December 2014

Description	Impact
Added support for multiple silicon revisions supported for ACDS 14.1 version of the Quartus II software.	-
Added a new parameter for Interlaken protocol implementation called Enable Interlaken TX random disparity bit . When enabled, a random number is used as a disparity bit.	
Changed the option "Manual (PLD controlled)" to "Manual (FPGA fabric controlled)" for the RX word aligner mode parameter.	-
Changed the option "SATA" to "SATA/SAS" for PMA configuration rules parameter.	-
Changed the descriptions of parameters CTLE adaptation mode and DFE adaptation mode .	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Arria 10 Transceiver Native PHY IP Core v14.0 Revision History

Table 16-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

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Description	Impact
Added support for PCS-Direct mode. The PCS-Direct mode enables you to bypass all the internal PCS blocks.	-
Changed the maximum data rate supported by GT channels to 28300 Mbps.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the Dynamic Reconfiguration tab.	-
Changed Enable embedded JTAG AVMM Master parameter to Enable Altera Debug Master Endpoint parameter.	-
Added the following parameters: <ul style="list-style-type: none"> • PMA Configuration Rules. • Enable fast sync status reporting for deterministic latency SM under the Word Aligner and Bitslip tab. Use this parameter for implementing CPRI (Auto) protocol. 	-
Added Faster Register mode for PCS TX and RX FIFO.	-
Changed the parameter Enable Reconfiguration between Standard and Enhanced PCS to Enable Datapath and Interface Reconfiguration .	-
Changed the one-time option for CTLE and DFE adaptation mode to Triggered mode.	-
Removed Enable tx_enh_fifo_cnt port and Enable rx_enh_fifo_cnt port parameters from the IP Parameter Editor .	-
Removed the parameter Device Speed Gradeselection .	-
Removed 62.5, 125, 200, and 250 values for PPM detector threshold.	-
Enhanced user warnings and information messages.	-

Description	Impact
Added the following presets: <ul style="list-style-type: none">• 3G SDI NTSC• 3G SDI PAL• HD SDI NTSC• HD SDI PAL• Low Latency GT• SAS Gen1• SAS Gen1.1• SAS Gen2• SATA Gen1• SATA Gen2• SATA Gen3• SFI-S 64:64 4x11.3Gbps• SONET/SDH OC-12• SONET/SDH OC-48• SONET/SDH OC-96• Serial Rapid IO 1.25Gbps	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Arria 10 Transceiver Native PHY IP Core v13.1 Revision History

Table 16-3: v13.1 Arria 10 Edition

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

CIC IP Core Revision History 17

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CIC IP Core v14.1

Table 17-1: v14.1 December 2014

Description	Impact
Added final support for Arria 10 devices	-

Related Information

- [CIC MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for CIC IP core in the Knowledge Base](#)

CIC IP Core v14.0 Arria 10 Edition

Table 17-2: 14.0 Arria 10 Edition August 2014

Description	Impact
Added two new buses, <code>av_st_in_data</code> and <code>av_st_out_data</code> , which includes all Avalon-ST compliant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- [CIC MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for CIC IP core in the Knowledge Base](#)

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CIC IP Core v14.0

Table 17-3: 14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices.	-
Added support for IP Catalog. For more information about IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [CIC MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for CIC IP core in the Knowledge Base](#)

CIC IP Core v13.1

Table 17-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX 	-

Related Information

- [CIC MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for CIC IP core in the Knowledge Base](#)

CPRI IP Core Revision History 18

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CPRI IP Core v14.1

Table 18-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1.		

Related Information

- [CPRI MegaCore Function User Guide](#)
- [Errata for CPRI IP core in the Knowledge Base](#)

CPRI IP Core v14.0

Table 18-2: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .		
Renamed Include Vendor Specific Space (VSS) access through CPU interface parameter to Include all control word access through CPU interface to better explain the function of the parameter. The parameter functionality remains as it was in the 13.1 and 13.0 releases.		

Related Information

- [Introduction to Altera IP Cores](#)
- [CPRI MegaCore Function User Guide](#)
- [Errata for CPRI IP core in the Knowledge Base](#)

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CPRI IP Core v13.1

Table 18-3: Version 13.1 November 2013

Description	Impact	Notes
Removed support for HardCopy IV GX device family.		
Improved the demonstration testbench.		
Improved resource utilization.		

Related Information

- [CPRI MegaCore Function User Guide](#)
- [Errata for CPRI IP core in the Knowledge Base](#)

CPRI IP Core v13.0

Table 18-4: Version 13.0 May 2013

Description	Impact	Notes
Added new parameter for user control of inclusion or exclusion of software interface to full control words.		
Added new parameter for user control of inclusion or exclusion of round-trip delay calibration feature.		
Reduced resource utilization in 28-nm devices.		

Related Information

- [CPRI MegaCore Function User Guide](#)
- [Errata for CPRI IP core in the Knowledge Base](#)

Cyclone V Hard IP for PCI Express IP Core Revision History 19

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Cyclone V Hard IP for PCI Express IP Core v14.1

Table 19-1: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- [Introduction to Altera IP Cores](#)
- [Cyclone V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Cyclone V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base](#)

Cyclone V Hard IP for PCI Express IP Core v14.0

Table 19-2: v14.0 June 2014

Description	Impact
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added support for new V-Series PCIe with Avalon-MM DMA Interface IP Core.	-

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Description	Impact
<p>Added the following features to the Cyclone V Avalon-MM Hard IP for PCI Express IP core:</p> <ul style="list-style-type: none"> Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. 	<p>All of these new features are optional. If you include either the hard IP status bus or status extension bus in your design, you must regenerate your design and connect the new bus.</p>

Related Information

- [Introduction to Altera IP Cores](#)
- [Cyclone V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Cyclone V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base](#)

Cyclone V Hard IP for PCI Express IP Core v13.0 SP1

Table 19-3: v13.0 SP1 July 2013

Description	Impact
Verified in the Quartus II software v13.0 SP1.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Cyclone V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Cyclone V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Cyclone V Hard IP for PCI Express in the Knowledge Base](#)

DDR2 and DDR3 SDRAM Controller with UniPHY Revision History 20

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DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v14.1

Table 20-1: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-

Related Information

- [External Memory Interface Handbook](#)
- [Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base](#)

DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v14.0

Table 20-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Removed support for Cyclone III, Cyclone III LS, and Stratix III devices	-

Related Information

- [External Memory Interface Handbook](#)
- [Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base](#)

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DDR2 and DDR3 SDRAM Controller with UniPHY IP Core v13.1

Table 20-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-
Removed support for HardCopy III and HardCopy IV devices	-

Related Information

- [External Memory Interface Handbook](#)
- [Errata for DDR3 SDRAM Controller with UniPHY IP core in the Knowledge Base](#)

DisplayPort IP Core Revision History 21

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DisplayPort IP Core v14.1

Table 21-1: v14.1 December 2014

Description	Impact
Added multi-stream support (MST, 1 to 4 source and sink streams). You can access this feature using these parameters: <ul style="list-style-type: none">• Support MST• Max stream count	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for 4Kp60 resolution.	
Removed support for double reference clocks—162MHz and 270MHz—for transceiver clocking.	
Updated the design example with pixel clock recovery feature and 4Kp60 support.	
Added new signals.	



Description	Impact
<p>Added new registers:</p> <ul style="list-style-type: none"> Source registers <ul style="list-style-type: none"> 0x00a0 (DPTX_MST_CONTROL1) 0x00a2 (DPTX_MST_VCPTAB0) 0x00a3 (DPTX_MST_VCPTAB 0x00a3 (DPTX_MST_VCPTAB1) 0x00a4 (DPTX_MST_VCPTAB2) 0x00a5 (DPTX_MST_VCPTAB3) 0x00a6 (DPTX_MST_VCPTAB4) 0x00a7 (DPTX_MST_VCPTAB5) 0x00a8 (DPTX_MST_VCPTAB6) 0x00a9 (DPTX_MST_VCPTAB7) 0x00aa (DPTX_MST_TAVG_TS) Sink registers <ul style="list-style-type: none"> 0x0006 (DPRX_BER_CNTI0) 0x0007 (DPRX_BER_CNTI1) 0x00a0 (DPRX_MST_CONTROL1) 0x00a1 (DPRX_MST_STATUS1) 0x00a2 (DPRX_MST_VCPTAB0) 0x00a3 (DPRX_MST_VCPTAB1) 0x00a4 (DPRX_MST_VCPTAB2) 0x00a5 (DPRX_MST_VCPTAB3) 0x00a6 (DPRX_MST_VCPTAB4) 0x00a7 (DPRX_MST_VCPTAB5) 0x00a8 (DPRX_MST_VCPTAB6) 0x00a9 (DPRX_MST_VCPTAB7) 	
<p>Changed the value of the following register bits:</p> <ul style="list-style-type: none"> Source register <ul style="list-style-type: none"> 0x0000 - Bits RX_LINK_RATE 0x0001 - Bits RX_LINK_RATE 0x0002 - Bits RSTI3, RSTI2, RSTI1, RSTI0 Sink register <ul style="list-style-type: none"> 0x0000 - Bits TX_LINK_RATE and ENHANCED_FRAME 	

Table 21-2: DisplayPort IP Core Signal Changes

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	clk_cal	Calibration clock for transceiver management interface
—	tx_link_rate_8bits	Main link rate expressed in multiples of 270Mbps
—	rx_link_rate_8bits	
—	txN_video_in (N=1,2,3)	TX signals for Stream 1, 2 and 3
—	txN_vid_clk (N=1,2,3)	
—	txN_audio (N=1,2,3)	
—	txN_audio_clk (N=1,2,3)	
—	txN_ss (N=1,2,3)	
—	txN_msa_conduit (N=1,2,3)	
—	rxN_video_out (N=1,2,3)	RX signals for Stream 1, 2 and 3
—	rxN_vid_clk (N=1,2,3)	
—	rxN_audio (N=1,2,3)	
—	rxN_ss (N=1,2,3)	
—	rxN_msa_conduit (N=1,2,3)	
—	rxN_stream (N=1,2,3)	
tx_xcvr_clkout	tx_ss_clk	—
rx_xcvr_clkout	rx_ss_clk	—

Related Information

- [Introduction to Altera IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

DisplayPort IP Core v14.0

Table 21-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added PHY Presets for Arria V, Cyclone V, and Stratix V device families.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added single clock reference (135MHz) for source and sink.	
Removed Native PHY from the IP core.	-
Updated register map and API functions.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

DisplayPort IP Core v13.1

Table 21-4: v13.1 November 2013

Description	Impact
Added support for Cyclone V devices.	-
Added HBR2 support for Arria V devices.	-
Added dual and quad pixel mode support.	-
Added quad symbol (40-bit) transceiver data interface support.	-
Added fast link training support.	-
Enhanced hardware demonstration designs: <ul style="list-style-type: none"> • Arria V device hardware demonstration design now demonstrates HBR2 functionality. • Hardware demonstration designs now demonstrate fast link training. • Hardware demonstration designs are now available for the Arria V FPGA Starter Kit development board and the Cyclone V GT development board 	-
Updated register map and API functions.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

FIR II IP Core Revision History 22

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FIR II IP Core v14.1

Table 22-1: v14.1 December 2014

Description	Impact
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- [FIR II IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FIR II IP core in the Knowledge Base](#)

FIR II IP Core v14.0 Arria 10 Edition

Table 22-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition	-

Related Information

- [FIR II IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FIR II IP core in the Knowledge Base](#)

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FIR II IP Core v14.0

Table 22-3: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Added support for IP Catalog. For more information about IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [FIR II IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FIR II IP core in the Knowledge Base](#)

FIR II IP Core v13.1

Table 22-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX 	-
Added full support for Arria V and Stratix V devices	-

Related Information

- [FIR II IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FIR II IP core in the Knowledge Base](#)

FFT IP Core Revision History 23

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FFT IP Core v14.1

Table 23-1: v14.1 December 2014

Description	Impact
Added hard-ffloating point option for Arria 10 devices.	-

Related Information

- [FFT MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FFT IP core in the Knowledge Base](#)

FFT IP Core v14.0 Arria 10 Edition

Table 23-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Added two new buses, <code>source_data</code> and <code>sink_data</code> , which includes all Avalon-ST compliant data signals, when you instantiate the IP core as part of a Qsys system.	-
Removed global clock enable signal, <code>clk_ena</code>	-

Related Information

- [FFT MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FFT IP core in the Knowledge Base](#)

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FFT IP Core v14.0

Table 23-3: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Added support for IP Catalog. For more information about IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [FFT MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FFT IP core in the Knowledge Base](#)

FFT IP Core v13.1

Table 23-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX 	-
Added full support for Arria V and Stratix V devices	-

Related Information

- [FFT MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FFT IP core in the Knowledge Base](#)

HDMI IP Core Revision History 24

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HDMI IP Core v14.1

Table 24-1: v14.1 December 2014

Description	Impact
Initial release.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Altera High-Definition Multimedia Interface User Guide](#)
- [Errata for HDMI IP core in the Knowledge Base](#)

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Interlaken PHY IP Core Revision History 25

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Interlaken PHY IP Core v14.1 Revision History

Table 25-1: v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for Interlaken PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Interlaken PHY IP Core v14.0 Revision History

Table 25-2: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for Interlaken PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

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Interlaken PHY IP Core v13.1 Revision History

Table 25-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for Interlaken PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Interlaken IP Core Revision History 26

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Caution: The Interlaken IP core is scheduled for product obsolescence and discontinued support as described in [PDN1410](#). Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's [Intellectual Property](#) website.

Interlaken IP Core v14.1

Table 26-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1.		

Related Information

- [Interlaken MegaCore Function User Guide](#)
- [Errata for Interlaken IP core in the Knowledge Base](#)

Interlaken IP Core v14.0

Table 26-2: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .		

Related Information

- [Introduction to Altera IP Cores](#)
- [Interlaken MegaCore Function User Guide](#)
- [Errata for Interlaken IP core in the Knowledge Base](#)

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Interlaken IP Core v13.1

Table 26-3: Version 13.1 November 2013

Description	Impact	Notes
Verified in the Quartus II software v13.1.		

Related Information

- [Interlaken MegaCore Function User Guide](#)
- [Errata for Interlaken IP core in the Knowledge Base](#)

Interlaken IP Core v13.0

Table 26-4: Version 13.0 May 2013

Description	Impact	Notes
Verified in the Quartus II software v13.0.		

Related Information

- [Interlaken MegaCore Function User Guide](#)
- [Errata for Interlaken IP core in the Knowledge Base](#)

IP Compiler for PCI Express Revision History 27

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IP Compiler for PCI Express v14.1

Table 27-1: Version 14.1 December 2014

Description	Impact	Notes
Verified in the Quartus II software v14.1.		

Related Information

- [IP Compiler for PCI Express User Guide](#)
- [Errata for IP Compiler for PCI Express in the Knowledge Base](#)

IP Compiler for PCI Express v14.0

Table 27-2: Version 14.0 June 2014

Description	Impact	Notes
Removed support for Cyclone III, Cyclone III LS, and Stratix III device families.	If your IP core variation targets one of these device families, and you choose to upgrade it to version 14.0, this change requires that you revise your IP core variation and regenerate it.	
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	Upgrading your IP core for this change is optional.	

Related Information

- [Introduction to Altera IP Cores](#)
- [IP Compiler for PCI Express User Guide](#)

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- [Errata for IP Compiler for PCI Express in the Knowledge Base](#)

IP Compiler for PCI Express v13.1

Table 27-3: Version 13.1 November 2013

Description	Impact	Notes
Removed support for the Arria GX, Cyclone II, HardCopy II, HardCopy III, HardCopy IV, Stratix II, and Stratix II GX device families.	If your IP core variation targets one of these device families, and you choose to upgrade it to version 14.0, this change requires that you revise your IP core variation and regenerate it.	

Related Information

- [Introduction to Altera IP Cores](#)
- [IP Compiler for PCI Express User Guide](#)
- [Errata for IP Compiler for PCI Express in the Knowledge Base](#)

IP Compiler for PCI Express v13.0

Table 27-4: Version 13.0 May 2013

Description	Impact	Notes
Removed support for the SOPC Builder design flow.		

Related Information

- [Introduction to Altera IP Cores](#)
- [IP Compiler for PCI Express User Guide](#)
- [Errata for IP Compiler for PCI Express in the Knowledge Base](#)

JESD204B IP Core Revision History 28

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JESD204B IP Core v14.1

Table 28-1: 14.1 December 2014

Description	Impact
Revised the parameter name of Enable PLL/CDR Dynamic Reconfiguration to Enable Transceiver Dynamic Reconfiguration .	–
Added a new parameter— Altera Debug Master Endpoint . Enable this feature to access the reconfiguration space of the Transceiver Native PHY IP Core.	This feature is available only for Arria 10 device family.
Added new register bits: <ul style="list-style-type: none">TX core:<ul style="list-style-type: none">Bit: <code>csr_reinit_w_rxsynchn_rise</code> in the <code>dll_ctrl</code> register (offset 0x50).Description: This bit controls the Code Group Synchronization (CGS) state exit behavior during link re-initialization.RX core:<ul style="list-style-type: none">Bit: <code>csr_synchn_delay</code> in the <code>synchn_sysref_ctrl</code> register (offset 0x54).Description: This bit extends the <code>SYNC_N</code> assertion (low state) by delaying the deassertion.	The new register bits are available when you upgrade the IP core in your design to v14.1.
Updated the <code>test_ilas_loop</code> bit behavior in the <code>dll_ctrl</code> register (offset 0x50).	Upgrade the IP core in your design to v14.1 to implement this new behavior.
Changed the JESD204B Avalon-MM slave interface <i>readLatency</i> value from 0 to 1.	Upgrade the IP core in your design to v14.1 to implement this new behavior.

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Description	Impact
	If you upgrade your IP core in your design, you have to reconnect the IP core in your design due to port change.
Changed the interface type of the <code>jesd204_rx_int</code> and <code>jesd204_tx_int</code> signals from conduit to interrupt.	–
Changed signal type of <code>pll_locked</code> , <code>tx_cal_busy</code> , <code>rx_cal_busy</code> , and <code>rx_is_lockedtoata</code> .	–
New simulation flow for the IP core design example testbench. Changed the link bring up sequence by powering up the JESD204B TX link and JESD204B RX link independently.	Regenerate the design example from the IP Parameter Editor to obtain this change.
Changed the default value of the 8B/10B encoder to /K28.5/ control word during reset assertion to resolve the CDR lock issue in the receiver. This change only affects design that select Enabled Soft PCS for the PCS Option parameter.	If you use Enabled Soft PCS for the PCS Option parameter, you must upgrade the IP core in your design to v14.1.

Related Information

- [JESD204B IP Core User Guide](#)
- [Errata for JESD204B IP core in the Knowledge Base](#)

JESD204B IP Core 14.0 Arria 10 Edition Update 1

Table 28-2: 14.0 Arria 10 Edition Update 1 September 2014

Description	Impact
<p>An optional upgrade is available for the JESD204B IP core in this release of the Altera Complete Design Suite. However, neither the IP Components window in the Project Navigator nor the IP Upgrade dialog box indicate that the upgrade is available.</p> <p>For information on features included in this optional upgrade, refer to the Altera Complete Design Suite Version 14.0 Arria 10 Edition Update Release Notes.</p>	To upgrade your IP core, use the IP Parameter Editor for the JESD204B IP core to regenerate the core. Automatic upgrade is not available.

Related Information

- [JESD204B IP Core User Guide](#)
- [Errata for JESD204B IP core in the Knowledge Base](#)

JESD204B IP Core 14.0 Arria 10 Edition

Table 28-3: 14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.
<p>New <code>pll_locked</code> signal behavior:</p> <ul style="list-style-type: none"> Changed the signal direction from output to input. Changed the signal width to follow the number of lanes selected instead of fixed at 1 bit. 	<p>If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition, this change requires that you regenerate the IP core manually and reconnect it in your design.</p>
<p>Added the following signals for JESD204B IP core variations that target an Arria 10 device:</p> <ul style="list-style-type: none"> <code>tx_bonding_clocks</code> signal on the transmitter path if you select <i>bonded</i> for the Bonded Mode option <code>tx_serial_clk0</code> signal on the transmitter path if you select <i>non-bonded</i> for the Bonded Mode option. <code>reconfig_clk</code>, <code>reconfig_reset</code>, <code>reconfig_avmm_address</code>, <code>reconfig_read</code>, <code>reconfig_readdata</code>, <code>reconfig_avmm_waitrequest</code>, <code>reconfig_write</code>, and <code>reconfig_writedata</code> if you turn on Enable PLL/CDR Dynamic Reconfiguration. 	
<p>Removed the following signals for JESD204B IP core variations that target an Arria 10 device:</p> <ul style="list-style-type: none"> <code>reconfig_to_xcvr</code> <code>reconfig_from_xcvr</code> <code>pll_ref_clk</code> on the transmitter path <code>pll_powerdown</code> on the transmitter path 	

Related Information

- [JESD204B IP Core User Guide](#)
- [Errata for JESD204B IP core in the Knowledge Base](#)

JESD204B IP Core 14.0

Table 28-4: 14.0 June 2014

Description	Impact
Initial release.	-

Related Information

- [JESD204B IP Core User Guide](#)
- [Errata for JESD204B IP core in the Knowledge Base](#)

LDPC IP Core Revision History 29

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LDPC IP Core v14.1

Table 29-1: v14.1 December 2014

Description	Impact
Initial release	-

Related Information

- [LDPC IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for FIR II IP core in the Knowledge Base](#)

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Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core Revision History 30

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Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v14.1

Table 30-1: Version 14.1 December 2014

Arria 10 support for this IP core is available in the Altera MegaCore IP Library. Stratix V support is available only through the Self-Service Licensing center.

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added optional 40GBASE-KR4 support in LL 40GbE IP core variations. Turning on the Enable KR4 parameter makes many additional 40GBASE-KR4 specific parameters available. 40GBASE-KR4 variations have many additional registers but no additional signals.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
All statistics increment vectors are now available and functional whether or not you include the relevant statistics counters in your IP core variations. Previously, the statistics increment vectors were functional only in IP core variations that included the relevant statistics module.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	

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Description	Impact	Notes
Added option to move the TX MAC PLL outside the IP core. Turning on the Use external TX MAC PLL parameter adds an input clock that drives the <code>clk_txmac</code> internal clock. This option adds no additional registers or register fields.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core unless you turn on the Use external TX MAC PLL parameter.	Refer to LL 40-100GbE IP Core Signal Changes table.
Added two new 64-bit statistics counters RXOctets_OK at offset 0x960 and TXOctets_OK at offset 0x860 to count the payload bytes (octets) in received and transmitted frames with no FCS errors, undersized, oversized, or payload length errors. The two registers each have two associated new signals.	Upgrading the IP core to incorporate this feature is optional. If you upgrade the IP core to the v14.1 version, this feature adds top-level signals and therefore requires that you reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes table.
Added new <code>CFG_PLEN_CHECK</code> register at offset 0x50A to support bit[4] of the new six-bit RX error signal.	If you upgrade your IP core to the v14.1 version and wish to use the new length checking status flag, you must ensure that user logic turns on the enable bit in this new register. In addition, the register supports a new RX error status flag signal that requires that you reconnect the IP core in your design.	
Changed handling of received malformed packet. If the IP core detects an incoming unexpected control character, it generates an EOP for the packet. Previously the IP core did not terminate (generate an EOP for) an incoming packet if it received an unexpected control character. In addition the IP core signals an error on the new six-bit RX error status signal when appropriate.	If you upgrade your IP core to the v14.1 version, you must be aware of this behavior change.	
Newly generated IP cores do not have top-level signals that interface to modules that the IP core does not include. This change applies to the TX MAC input clock, link fault signals, pause signals, and PTP signals.	Because of the backward compatibility feature described in the Notes column, if you upgrade your IP core to the v14.1 version, this feature has no effect on the top-level signals and does not require any additional actions. Note that this feature applies only to IP core variations that do not instantiate the relevant module or modules.	For backward compatibility, if you upgrade an IP core variation, link fault signals, pause top-level signals, and PTP signals in the earlier release of the IP core variation remain available in the 14.1 version after upgrade.

Description	Impact	Notes
<p>Updated PTP module behavior and modified parameter name. If you turn on Enable 1588 PTP, the PTP module has the following new features and requirements:</p> <ul style="list-style-type: none"> You must instantiate a time-of-day (TOD) module and connect it to the IP core. Added new PTP signals to receive the timestamps the TOD module generates in the two clock domains. Refer to LL 40-100GbE IP Core Signal Changes table. Removed TX PTP module TOD calculation registers at offsets 0xB06 through 0xB08. The TOD module now provides the functionality the registers supported in previous versions of the IP core. Added support for resetting the TCP checksum to zero of the application does not recalculate it. Added two new signals with which the application communicates such a request to the IP core. Refer to LL 40-100GbE IP Core Signal Changes table. 	<p>Upgrading the IP core to incorporate this feature is optional. If you upgrade the IP core to the v14.1 version, and the PTP module is included in your original IP core variation, this feature adds top-level signals and therefore requires that you reconnect the IP core in your design.</p>	
<p>Improved RX skew tolerance to 1900 bits for LL 40GbE IP core variations and to 1000 bits for LL 100GbE IP core variations. Altera LL 40-100GbE IP cores exceed the IEEE 802.3-2012 Ethernet Standard Clause 82.2.12 requirements of 1856 bits skew tolerance for 40GbE IP cores and 928 bits skew tolerance for 100GbE IP cores.</p>		

Table 30-2: LL 40-100GbE IP Core Signal Changes

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	clk_txmac_in	Input clock to drive the clk_txmac internal clock. This signal is available if you turn on Use external TX MAC PLL in the LL 40-100GbE parameter editor.

Old Signal Name	New Signal Name	Notes
l<n>_rx_error (1 bit)	l<n>_rx_error[5:0] (Avalon-ST client interface)	New six-bit RX error status signal.
—	rx_error[5:0] (custom client interface)	
—	unidirectional_en	Signals that provide status from the LINK_FAULT_CONFIG register.
—	link_fault_gen_en	
—	tx_inc_octetsOK[15:0]	Signals that provide per-frame information associated with the new RxOctets_OK and TXOctets_OK registers. These signals are present and functional whether or not you turn on Enable TX statistics or Enable RX statistics in the parameter editor.
—	tx_inc_octetsOK_valid	
—	rx_inc_octetsOK{15:0}	
—	rx_inc_octetsOK_valid	
—	tx_in_zero_tcp	Signals for application to direct the IP core to reset the TCP checksum field.
—	tx_in_tcp_offset[15:0]	
—	tod_txmac_in[95:0]	Signals to receive TOD values from new external TOD module.
—	tod_rxmac_in[95:0]	

Link fault signals are present in new IP core variations you generate in the Quartus II v14.1 IP Catalog only if you turn on **Enable link fault generation** in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.

Pause signals are present in new IP core variations that you generate in the Quartus II v14.1 IP Catalog only if you set **Flow control mode** to standard flow control or priority-based flow control in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.

PTP interface signals are present in new IP core variations that you generate in the Quartus II v14.1 IP Catalog only if you turn on **Enable 1588 PTP** in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.

Related Information

- [Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0 Arria 10 Edition

Table 30-3: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Initial release in the Altera MegaCore IP Library.		

Related Information

- [Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

Low Latency Ethernet 10G MAC IP Core Revision History 31

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Low Latency Ethernet 10G MAC IP Core v14.1

Table 31-1: v14.1 December 2014

Description	Impact
Added new parameter options: <ul style="list-style-type: none">• Enable 10GBASE-R register mode• Time of Day Format.	If you do not upgrade your IP core, it does not have this new feature.
Added new signals to support 10GBASE-R register mode: <ul style="list-style-type: none">• tx_xcvr_clk• rx_xcvr_clk• xgmii_tx_valid• xgmii_rx_valid	

Related Information

- [Introduction to Altera IP Cores](#)
- [Low Latency Ethernet 10G MAC MegaCore Function User Guide](#)
- [Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base](#)

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Low Latency Ethernet 10G MAC IP Core v14.0 Arria 10 Edition

Table 31-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition, all of the changes require that you regenerate the IP core manually and reconnect it in your design.

Related Information

- [Introduction to Altera IP Cores](#)
- [Low Latency Ethernet 10G MAC MegaCore Function User Guide](#)
- [Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base](#)

Low Latency Ethernet 10G MAC IP Core v14.0

Table 31-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added support for unidirectional feature.	The following changes are optional. If you do not upgrade your IP core, it does not have these new features.
Modified the reset behavior—TX and RX reset signals changed from asynchronous reset to synchronous reset.	
Resource improvement with no impact to performance.	

Related Information

- [Introduction to Altera IP Cores](#)
- [Low Latency Ethernet 10G MAC MegaCore Function User Guide](#)
- [Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base](#)

Low Latency Ethernet 10G MAC IP Core v13.1 Arria 10 Edition

Table 31-4: v13.1 Arria 10 Edition December 2013

Description	Impact
Added support for Arria 10 devices.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Low Latency Ethernet 10G MAC MegaCore Function User Guide](#)
- [Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base](#)

Low Latency Ethernet 10G MAC IP Core v13.1

Table 31-5: v13.1 November 2013

Description	Impact
Initial release. <ul style="list-style-type: none">• Lowest latency 10-Gbps Ethernet MAC with 32-bit user interface mode.• Final support for Arria V GZ and Stratix V devices.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Low Latency Ethernet 10G MAC MegaCore Function User Guide](#)
- [Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base](#)

Nios II Processor Revision History 32

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Note: Unless otherwise noted, the Nios II processor supports new device families as they are supported by the Quartus II software.

Table 32-1: Product Revision History

Version	Date	Description
14.1	December 2014	Verified in the Quartus II software v14.1.
14.0a10	August 2014	The Nios II Gen2 processor supports 14.0 Arria 10 Edition.
14.0	June 2014	<ul style="list-style-type: none">Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i>.Fixed issue concerning instruction cache operation with ECCAdded Nios II Gen2 core<ul style="list-style-type: none">Improved Nios II/f core.ECC support for data cache and TCMs.Optional 32-bit addressing.Faster arithmetic instructions.Optional uncached peripheral memory region.More flexible debugging options.Avalon streaming interface for trace.Includes Nios II/f and Nios II/e. Nios II/s processor core not supported.Simpler, more flexible parameter editor in Qsys.Removed support for the following devices:<ul style="list-style-type: none">Stratix IIICyclone IIICyclone III LS
13.1 A10	December 2013	Verified in the Quartus II software v13.1 A10

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Version	Date	Description
13.1	November 2013	<ul style="list-style-type: none"> Enhanced floating point custom instruction support Added ECC support Added RTL Nios II processor trace simulation support Verified in the Quartus II software v13.1 Removed support for the following devices: <ul style="list-style-type: none"> Arria GX Cyclone, Cyclone II HardCopy II, HardCopy III, and HardCopy IV Stratix, Stratix II, Stratix GX, and Stratix II GX

Related Information

- [Introduction to Altera IP Cores](#)
For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor*.
- [Nios II Processor Reference Handbook](#)
- [Nios II Embedded Design Suite Release Notes](#)
- [Errata for Nios II processor in the Knowledge Base](#)

What's New in v14.0 Arria 10 Edition

Arria 10 FPGA devices are supported by the Nios II Gen2 processor, but not by the classic Nios II processor. To implement a Nios II system on an Arria 10 device, you must use the Nios II Gen2 processor core.

What's New in v14.0

The Nios II Gen2 Processor Core

In v14.0, the Nios II processor core includes a preview implementation of the Nios II Gen2 processor core, supporting Altera's latest device families. The Nios II Gen2 processor core delivers size and performance similar to the original Nios II processor, and is compatible with classic Nios II processor code at the binary level.

The tool flow and HAL include options to support Gen2 features. The workflow for generating BSPs and building software is the same, but BSPs generated for the classic Nios II processor must be regenerated.

Differences Between Classic and Gen2 Nios II Processors

Differences between the Nios II Gen2 core and the classic Nios II core include:

- Improved Nios II/f core
- Optional 32-bit addressing
- Improved parameter editor in Qsys

The Nios II/s core option is not available with the Nios II Gen2 core. You can create a processor configuration identical to the Nios II/s by configuring the Nios II/f Gen2 core appropriately.

Differences Between Classic and Gen2 Nios II/f Processors

Feature	Classic Nios II/f	Nios II/f Gen2
32-bit addressing	No	Optional
Configurable-size uncached peripheral memory region	No	Optional
Uncached write updates cached data	Yes	No
Static branch prediction	No	Optional
ECC	Starting in v13.1, optional on: <ul style="list-style-type: none"> Processor core RAMs Instruction cache 	Optional on: <ul style="list-style-type: none"> Processor core RAMs Instruction cache Data cache Tightly-coupled memories (instruction and data)
32-bit multiply performance	5 cycles	1 cycle
64-bit multiply support	Devices with DSP blocks	All devices
Low-cost shifter	1 bit/cycle	4 bits/cycle

The Nios II/f Gen2 processor core also features the following improvements over the classic Nios II/f core:

- Divide performance is higher on average, and more deterministic.
- The JTAG debug options offer more flexibility in the number of hardware breakpoints and triggers.

On the Nios II/f Gen2 processor core, off-chip trace appears as an Avalon Streaming (Avalon-ST) interface. Therefore, off-chip trace requires the addition of an IP core to bridge between the Avalon-ST interface and the trace probe connection. Consult the supplier of your trace tool for the appropriate IP core.

Uncached Writes in the Nios II/f Gen2 Core

On an uncached write, if the data to be written happens to be cached, the classic Nios II processor updates the cache. On an uncached write, the Nios II/f Gen2 processor updates memory, but ignores the cache. Software must take this behavior into account.

Differences Between Classic and Gen2 Nios II/e Processors

The Nios II/e Gen2 core optionally supports 32-bit addressing.

Nios II Gen2 Processor Cores and MAX 10 FPGA Support

MAX 10 FPGA devices are supported by the Nios II Gen2 processor, but not by the classic Nios II processor. To implement a Nios II system on a MAX 10 device, you must use the Nios II Gen2 processor core.

The Altera On-chip Flash memory component, introduced in 14.0, enables Avalon-MM access to on-chip MAX 10 user flash memory. With this component, the Nios II boot copier can copy code to RAM from the MAX 10 user flash memory.

Upgrading to the Nios II Gen2 Processor

Existing Qsys systems containing the classic Nios II processor can be automatically upgraded to the Nios II Gen2 processor by running a TCL script.

Related Information

[Altera Knowledge Base](#)

Information about migrating from the classic Nios II processor to the Nios II Gen2 processor, including the `nios2_gen2_migration.tcl` script.

Nios II Processor Core ECC Fixes in 14.0

In v13.1, when configured with ECC protection, the Nios II processor could manifest invalid instruction cache operation with ECC errors. This issue is fixed in v14.0.

What's New in v13.1

Enhanced Floating Point Custom Instruction Support

In v13.1, Qsys adds an option to select a new floating point custom instruction set component, Floating Point Hardware 2. The component consists of the following custom instructions:

- One combinatorial custom instruction—implements comparison, minimum, maximum, negate, and absolute operations
- One multi-cycle custom instruction—implements add, subtract, multiply, divide, square root, and conversion operations

These custom instructions are binary compatible with the original Nios II floating point custom instructions. They offer better performance, with fewer cycles per operation.

Note: Floating point calculation results made with the Floating Point Hardware 2 custom instructions may differ slightly from those calculated by the original custom instructions, because the new instructions use a different rounding algorithm to increase performance.

Floating Point Hardware 2 appears in the Embedded Processor section in Qsys.

The Floating Point Hardware 2 instructions are available in VHDL only. They are IEEE 754-2008 compliant with the following exceptions:

- Simplified rounding.
- Simplified NaN handling.
- No exceptions generated. Exception conditions are indicated by a specific result, such as NaN.
- No status flags.
- Subnormal supported only on a subset of operations.

To take advantage of software support for the Floating Point Hardware 2 instructions, include `altera_nios_custom_instr_floating_point_2.h`, which forces GCC to call newlib math functions (rather than GCC built-in math functions). Altera recommends that you recompile newlib with for optimum performance.

Note: Do not use the `-mcustom -fpu-cfg` command-line option for GCC. This option does not support the Floating Point Hardware 2 instructions.

The Nios II software build tools (SBT) add individual `-mcustom` commands to the makefile to support the Floating Point Hardware 2 custom instructions.

ECC Support

Starting in v13.1, the Nios II Processor parameter editor lets you enable ECC protection for the RAMs in the processor core and the instruction cache. Single-bit soft errors are corrected, and dual-bit soft errors cause either an instruction cache flush or processor exception. ECC support is only available on the Nios II/f core without the data cache.

When ECC protection is selected, an Avalon-ST source is added to the processor core to provide ECC status information to external logic. By default, ECC is not enabled on reset. Therefore, software must enable ECC protection. Software can also inject ECC errors into RAM data bits to support testing of the ECC exception handler and event bus.

The Nios II Hardware Abstraction Layer (HAL) is extended to support ECC initialization and exception handling.

Note: ECC is not supported with the data cache.

RTL Nios II Processor Trace Simulation Support

Starting in v13.1, the Nios II processor adds RTL trace simulation support. This feature enables Nios II processor instruction execution to be recorded during RTL simulation in ModelSim™. Events are recorded and time-stamped during RTL simulation. Examples of recorded events:

- Instruction execution
- Instruction address
- Data address
- Data value
- Interrupts
- Exceptions
- Resets
- Control register changes

The time stamp lets you align hardware simulation data with software execution.

This feature is enabled by selecting the appropriate option in the Nios II processor parameter editor. When trace simulation support is enabled, Qsys adds RTL to the Nios II testbench to support the generation of a trace (*.tr) file. The *.tr file can be converted to human readable format with the `nios2-display-rtl` conversion tool.

NCO IP Core Revision History 33

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NCO IP Core v14.1

Table 33-1: v14.1 December 2014

Description	Impact
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- [NCO MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for NCO IP Core in the Knowledge Base](#)

NCO IP Core v14.0 Arria 10 Edition

Table 33-2: v14.0 Arria 10 Edition

Description	Impact
Added two new buses, <code>in_data</code> and <code>out_data</code> , which includes all Avalon-ST compliant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- [NCO MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for NCO IP Core in the Knowledge Base](#)

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NCO IP Core v14.0

Table 33-3: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Fixed a bug where the incorrect output frequency is generated when the accumulator precision is greater than or equal to 56 in single-channel configuration.	-
Fixed a mismatch between the C model and RTL when angular precision is less than or equal to 10 in serial CORDIC architecture.	-
Added support for IP Catalog. For more information about IP Catalog, refer to <i>IP Catalog and Parameter Editor in Introduction to Altera IP Cores</i> .	-

Related Information

- [NCO MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for NCO IP Core in the Knowledge Base](#)

NCO IP Core v13.1

Table 33-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX 	-
Added full support for Arria V and Stratix V devices	-

Related Information

- [NCO MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for NCO IP Core in the Knowledge Base](#)

PCI Compiler Revision History 34

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Caution: The PCI Compiler is scheduled for product obsolescence and discontinued support as described in [PDN1410](#). Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's [Intellectual Property](#) website.

PCI Compiler v14.0

Table 34-1: v14.0 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Removed support for Cyclone III and Stratix III devices.	

Related Information

- [Introduction to Altera IP Cores](#)
- [PCI Compiler IP Core User Guide](#)
- [Errata for PCI Compiler IP Core in the Knowledge Base](#)

PCI Compiler v13.1

Table 34-2: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none">• Arria GX• Cyclone and Cyclone II• HardCopy II, HardCopy III, and HardCopy IV• Stratix, Stratix GX, Stratix II, and Stratix II GX	-

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Description	Impact
Removed support for <code>pci_mt64</code> and <code>pci_t64</code> variations.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [PCI Compiler IP Core User Guide](#)
- [Errata for PCI Compiler IP Core in the Knowledge Base](#)

POS-PHY Level 4 IP Core Revision History 35

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Caution: The POS-PHY level 4 IP core is scheduled for product obsolescence and discontinued support as described in [PDN1410](#). Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's [Intellectual Property](#) website.

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QDR II and QDR II+ SRAM Controller with UniPHY

Revision History

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QDR II and QDR II+ SRAM Controller with UniPHY v14.1

Table 36-1: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-

Related Information

- [External Memory Interfaces Handbook](#)
- [Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base](#)

QDR II and QDR II+ SRAM Controller with UniPHY v14.0

Table 36-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor in Introduction to Altera IP Cores</i> .	-
Removed support for Cyclone III, Cyclone III LS, and Stratix III devices	-

Related Information

- [External Memory Interfaces Handbook](#)
- [Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base](#)

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QDR II and QDR II+ SRAM Controller with UniPHY v13.1

Table 36-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-
Removed support for HardCopy III and HardCopy IV devices	-

Related Information

- [External Memory Interfaces Handbook](#)
- [Errata for QDR II and QDR II+ SRAM Controller with UniPHY in the Knowledge Base](#)

RapidIO IP Core Revision History 37

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RapidIO IP Core v14.1

Table 37-1: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Information

- [RapidIO MegaCore Function User Guide](#)
- [Errata for RapidIO IP core in the Knowledge Base](#)

RapidIO IP Core v14.0 Arria 10 Edition

Table 37-2: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices). RapidIO IP core variations that target an Arria 10 device have the following differences from the variations that target earlier device families.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition	

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Description	Impact	Notes
	software and reconnect it in your design.	
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core and a reset controller in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in Table 37-3 .
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, if you turn on the new parameter Enable transceiver dynamic reconfiguration , these variations have an internal reconfiguration controller that the user accesses through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in Table 37-3 .
<p>If a RapidIO IP core that targets an Arria 10 device includes an I/O Logical layer Avalon-MM slave interface or an I/O Logical layer Avalon-MM master interface, the following conditions apply:</p> <ul style="list-style-type: none"> • The IP core must include both an I/O Logical layer slave interface and an I/O Logical layer master interface. It cannot include one but not the other. • The I/O Logical layer slave module preserves transaction ordering between read and write operations. • The number of RX address translation windows is 16. • The number of TX address translation windows is 16. 	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Description	Impact	Notes
<p>If a RapidIO IP core that targets an Arria 10 device includes an I/O Maintenance Logical layer module, the following conditions apply:</p> <ul style="list-style-type: none"> The module has both master and slave ports. The number of Maintenance transmit address translation windows is 16. The module supports both reception and transmission of <code>port-write</code> requests, or supports neither. 	<p>Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.</p>	
<p>A RapidIO IP core that targets an Arria 10 device supports both outbound and inbound <code>DOORBELL</code> messages, or it supports neither.</p>	<p>Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.</p>	
<p>If a RapidIO IP core that targets an Arria 10 device supports <code>DOORBELL</code> messages, it preserves transaction order between <code>DOORBELL</code> messages and I/O write request transactions.</p>	<p>Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.</p>	

Description	Impact	Notes
A RapidIO IP core that targets an Arria 10 device automatically synchronizes transmitted ackIDs.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In a RapidIO IP core that targets an Arria 10 device, the number of <code>link-request</code> attempts before declaring a fatal error is tied to 7.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In a RapidIO IP core that targets an Arria 10 device, the Physical layer receive and transmit buffers are 32 Kbytes each.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Description	Impact	Notes
In the parameter editor for RapidIO IP core variations that target an Arria 10 device, the Disable Destination ID checking by default parameter is not available. Arria 10 variations do not check destination IDs, by default. However, support for controlling this feature through the IP core registers is available in all RapidIO IP core variations, as it was in the previous release.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Table 37-3: RapidIO IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_bonded_clocks_ch<n>[5:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. Individual transceiver channel clock signals. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_clk_ch<n>	New Arria 10 transceiver reconfiguration interface. This interface is available if you turn on Enable transceiver dynamic reconfiguration in the RapidIO parameter editor. Relevant for Arria 10 variations only. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_reset_ch<n>	
—	reconfig_read_ch<n>	
—	reconfig_write_ch<n>	
—	reconfig_address_ch<n>[9:0]	
—	reconfig_readdata_ch<n>[31:0]	
—	reconfig_waitrequest_ch<n>	
—	reconfig_writedata_ch<n>[31:0]	

Old Signal Name	New Signal Name	Notes
—	tx_analogreset[N-1:0]	New interface to external reset controller. Relevant for Arria 10 variations only. N is the number of RapidIO lanes.
—	rx_analogreset[N-1:0]	
—	tx_digitalreset[N-1:0]	
—	rx_digitalreset[N-1:0]	
reconfig_togxb	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V, Cyclone V, and Stratix V variations. This interface is present only in Arria V, Cyclone V, and Stratix V variations (as supported in past and future versions of the Quartus II software). These signals are not present in Arria 10 variations.
reconfig_fromgxb	Not present in Arria 10 variations.	

Related Information

- [RapidIO MegaCore Function User Guide](#)
- [Errata for RapidIO IP core in the Knowledge Base](#)

RapidIO IP Core v14.0

Table 37-4: Version 14.0 June 2014

Description	Impact	Notes
Removed support for Cyclone III, Cyclone III LS, and Stratix III device families. The Quartus II software v14.0 does not support these device families.	If your IP core variation targets one of these device families, this change requires that you revise your IP core variation and regenerate it.	
Removed support for Physical-layer only variations.	If your IP core variation is no longer supported, and you choose to upgrade the IP core, this change requires that you revise your IP core variation and regenerate it.	
Removed support for external transceivers. All supported variations include configuration of the high-speed transceivers on the target device.	If your IP core variation is no longer supported, and you choose to upgrade the IP core, this change requires that you revise your IP core variation and regenerate it.	
Removed naming differences between Qsys-generated and non-Qsys-generated IP core variations. New variations generated in	If your IP core was generated in the MegaWizard Plug-In Manager flow, and you choose to upgrade the IP	

Description	Impact	Notes
the 14.0 software, whether in Qsys or outside Qsys, use the port names previously identified with the Qsys variations.	core, this change requires that you revise your IP core variation, upgrade it, and reconnect your IP core in your design.	
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	This change is optional for v13.1 IP cores. However, IP upgrade is required for IP cores v13.0 and earlier.	

Related Information

- [Introduction to Altera IP Cores](#)
- [RapidIO MegaCore Function User Guide](#)
- [Errata for RapidIO IP core in the Knowledge Base](#)

RapidIO IP Core v13.1

Table 37-5: Version 13.1 November 2013

Description	Impact	Notes
Removed support for the Arria GX, Cyclone II, HardCopy II, HardCopy III, HardCopy IV E, HardCopy IV GX, Stratix II, and Stratix II GX device families.		

Related Information

- [RapidIO MegaCore Function User Guide](#)
- [Errata for RapidIO IP core in the Knowledge Base](#)

RapidIO IP Core v13.0

Table 37-6: Version 13.0 May 2013

Description	Impact	Notes
Added 2x mode for Arria V, Cyclone V, and Stratix V devices.		
Removed support for SOPC Builder design flow.		

Related Information

- [RapidIO MegaCore Function User Guide](#)
- [Errata for RapidIO IP core in the Knowledge Base](#)

RapidIO II IP Core Revision History 38

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RapidIO II IP Core v14.1

Table 38-1: Version 14.1 December 2014

Description	Impact	Note
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added <code>io_error_response_set</code> input port. The IP core sets the <code>IO_ERROR_RSP</code> field in bit [31] of the Logical/Transport Layer Error Detect CSR at offset 0x308 when this signal changes value from 0 to 1.	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, you must reconnect the IP core in your design so the new input signal does not float.	
Changed behavior of individual baud rate <code>_ENABLE</code> and <code>_SUPPORT</code> fields of Port 0 Control 2 CSR at offset 0x154. Instead of all being set to the value of 1, now the <code>_ENABLE</code> and <code>_SUPPORT</code> fields for baud rates less than or equal to the value of the Maximum baud rate parameter have the value of 1, and the <code>_ENABLE</code> and <code>_SUPPORT</code> fields for baud rates greater than the value of the Maximum baud rate parameter have the value of 0.	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, the Port 0 Control 2 CSR fields are set as expected to indicate the supported and enabled baud rates.	To modify the IP core to run at a different baud rate than the Maximum baud rate value, you must turn on Enable transceiver dynamic reconfiguration in the parameter editor, and user logic must reconfigure the transceiver to the new baud rate. As indicated by the values of the Port 0 Control 2 CSR fields, you can only reconfigure the IP core to a baud rate equal or slower than the Maximum baud rate value.

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Description	Impact	Note
<p>Made changes to Port 0 Control CSR at offset 0x15C:</p> <ul style="list-style-type: none"> Added new field <code>PORT_ERR_IRQ_EN</code> that controls whether an interrupt is generated when an error is flagged in the Port 0 Error Detect register at offset 0x340. The new field is in bit [6] of the Port 0 Control CSR. Moved <code>DIS_DEST_ID_CHK</code> field from bit [7] to bit [8]. Moved <code>LOG_TRANS_ERR_IRQ_EN</code> field from bit [6] to bit [7]. 	<p>If you upgrade the RapidIO II IP core in your design to the IP core v14.1, your IP core implements the new behavior. You can use the new register field to force an interrupt in this case.</p>	

Related Information

- [RapidIO II MegaCore Function User Guide](#)
- [Errata for RapidIO II IP core in the Knowledge Base](#)

RapidIO II IP Core v14.0 Arria 10 Edition

Table 38-2: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Note
<p>Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).</p>	<p>Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.</p>	

Description	Impact	Note
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in Table 38-3 .
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, if you turn on the new parameter Enable transceiver dynamic reconfiguration , these variations have an internal reconfiguration controller that the user accesses through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in Table 38-3 .

Table 38-3: RapidIO II IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_bonded_clocks_ch<n>[5:0]	<p>New interface to external TX PLL. Relevant for Arria 10 variations only.</p> <p>Individual transceiver channel clock signals. One signal (_ch<n>) for each RapidIO lane <n>.</p>

Old Signal Name	New Signal Name	Notes
—	reconfig_clk_ch<n>	New Arria 10 transceiver reconfiguration interface. This interface is available if you turn on Enable transceiver dynamic reconfiguration in the RapidIO II parameter editor. Relevant for Arria 10 variations only.
—	reconfig_reset_ch<n>	
—	reconfig_read_ch<n>	
—	reconfig_write_ch<n>	
—	reconfig_address_ch<n>[9:0]	
—	reconfig_readdata_ch<n>[31:0]	
—	reconfig_waitrequest_ch<n>	
—	reconfig_writedata_ch<n>[31:0]	
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface signals for specific non-Arria 10 device families (as supported in past and future versions of the Quartus II software). These signals are not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	
pll_locked	Not present in Arria 10 variations.	
pll_powerdown	Not present in Arria 10 variations.	

Related Information

- [RapidIO II MegaCore Function User Guide](#)
- [Errata for RapidIO II IP core in the Knowledge Base](#)

RapidIO II IP Core v14.0

Table 38-4: Version 14.0 June 2014

Description	Impact	Note
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor in Introduction to Altera IP Cores</i> .	This change is optional for v13.1 IP cores. However, IP upgrade is required for IP cores v13.0 and earlier.	

Description	Impact	Note
In case of MAINTENANCE Response with Error status, the ADDRESS field of the Logical/Transport Layer Address Capture CSR captures the config_offset value from the original request.	None. This change is optional. If you do not upgrade your IP core, it does not have this new feature.	
Added new allowed value IMPLEMENTATION SPECIFIC for INFO_TYPE field of Port 0 Attributes Capture CSR.	None. This change is optional. If you do not upgrade your IP core, it does not have this new feature.	

Related Information

- [Introduction to Altera IP Cores](#)
- [RapidIO II MegaCore Function User Guide](#)
- [Errata for RapidIO II IP core in the Knowledge Base](#)

RapidIO II IP Core v13.1

Table 38-5: Version 13.1 November 2013

Description	Impact	Note
Verified in the Quartus II software v13.1.		

Related Information

- [RapidIO II MegaCore Function User Guide](#)
- [Errata for RapidIO II IP core in the Knowledge Base](#)

RapidIO II IP Core v13.0

Table 38-6: Version 13.0 May 2013

Description	Impact	Note
Verified in the Quartus II software v13.0.		

Related Information

- [RapidIO II MegaCore Function User Guide](#)
- [Errata for RapidIO II IP core in the Knowledge Base](#)

Reed-Solomon IP Core Revision History 39

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Caution: The Reed-Solomon IP core is scheduled for product obsolescence and discontinued support as described in [PDN1410](#). Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's [Intellectual Property](#) website.

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Reed-Solomon II IP Core Revision History 40

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Reed-Solomon II IP Core v14.1

Table 40-1: v14.1 December 2014

Description	Impact
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- [Reed-Solomon II MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Reed-Solomon II IP core in the Knowledge Base](#)

Reed-Solomon II IP Core v14.0 Arria 10 Edition

Table 40-2: v14.0 Arria 10 edition August 2014

Description	Impact
Added two new buses, <code>in_data</code> and <code>out_data</code> , which includes all Avalon-ST compliant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- [Reed-Solomon II MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Reed-Solomon II IP core in the Knowledge Base](#)

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Reed-Solomon II IP Core v14.0

Table 40-3: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices	-
Added preliminary support for MAX 10 FPGAs	-
Added variable decoding and encoding	-
Improved compilation time for large bits-per-symbol codes	-
Added support for IP Catalog. For more information about IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Reed-Solomon II MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Reed-Solomon II IP core in the Knowledge Base](#)

Reed-Solomon II IP Core v13.1

Table 40-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX 	-
Added full support for Arria V and Stratix V devices	-
Added support for erasures-supporting decoders	-

Related Information

- [Reed-Solomon II MegaCore Function User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Reed-Solomon II IP core in the Knowledge Base](#)

RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core Revision History 41

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RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v14.1

Table 41-1: v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-

Related Information

- [External Memory Interface Handbook](#)
- [Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base](#)

RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v14.0

Table 41-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor in Introduction to Altera IP Cores</i> .	-
Removed support for Cyclone III, Cyclone III LS, and Stratix III devices	-

Related Information

- [External Memory Interface Handbook](#)
- [Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base](#)

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RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core v13.1

Table 41-3: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-
Removed support for HardCopy III and HardCopy IV devices	-

Related Information

- [External Memory Interface Handbook](#)
- [Errata for RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP in the Knowledge Base](#)

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SDI v14.0

Table 42-1: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Removed support for Cyclone III and Stratix III devices.	

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI IP Core User Guide](#)
- [Errata for SDI IP Core in the Knowledge Base](#)

SDI v13.1

Table 42-2: v13.0 November 2013

Description	Impact
Verified in the Quartus II software v13.0	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI IP Core User Guide](#)
- [Errata for SDI IP Core in the Knowledge Base](#)

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SDI II IP Core Revision History 43

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SDI II IP Core v14.1

Table 43-1: v14.1 December 2014

Description	Impact
The run_sim script for each simulator is now located in its respective folder.	-
rx_format signal now reports video transport format instead of picture format. The signal reports 3G Level A RGB or YCbCr 4:4:4 format.	If you update to the Quartus II software version 14.1, you must update your SDI II IP core to incorporate this fix.
Changed the names of the following parameters: <ul style="list-style-type: none">• Convert Level A to Level B (SMPTE 372M) changed to Convert HD-SDI dual link to 3G-SDI (level B)• Convert Level B to Level A (SMPTE 372M) changed to Convert 3G-SDI (level B) to HD-SDI dual link	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI II IP Core User Guide](#)
- [Errata for SDI II IP Core in the Knowledge Base](#)

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SDI II IP Core v14.0 Update 2

Table 43-2: v14.0 Update 2 September 2014

Description	Impact
Fixed an issue in which RX cannot lock to HD-SDI standard in certain seed.	If you update to the Quartus II software version 14.0 Update 2, you must update your SDI II IP core to incorporate this fix.

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI II IP Core User Guide](#)
- [Errata for SDI II IP Core in the Knowledge Base](#)

SDI II IP Core v14.0 Arria 10

Table 43-3: v14.0 Arria 10 August 2014

Description	Impact
Added support for Arria 10 devices.	If you update your SDI II IP core to the the Quartus II software v14.0 Arria 10 Edition, all of the changes require that you regenerate the IP core manually and reconnect it in your design.
Removed the transceiver PHY and TX PLL from the SDI II IP core. You must generate the transceiver and the TX PLL separately.	
You will need to update your design if you are migrating to Arria 10 from a 28nm device family because the IP ports have changed.	
<p>The Arria 10 variations include the following new signals:</p> <ul style="list-style-type: none"> • Transceiver signals: rx_ready, gxb_ltr, gxb_ltd, trig_rst_ctrl, rx_ready_b, gxb_ltr_b, and gxb_ltd_b. • Transceiver Reconfiguration Controller signals: xcvr_reconfig_clk, xcvr_reconfig_rst, xcvr_reconfig_write, xcvr_reconfig_read, xcvr_reconfig_address, xcvr_reconfig_writedata, xcvr_reconfig_readdata, xcvr_reconfig_waitrequest, cdr_reconfig_sel, cdr_reconfig_req, cdr_reconfig_busy, pll_sel, pll_sw_req, pll_busy, external_avmm_master_req, reconfig_write_from_ext_avmm_master, reconfig_read_from_ext_avmm_master, reconfig_address_from_ext_avmm_master, reconfig_writedata_from_ext_avmm_master, reconfig_readdata_from_ext_avmm_master, and reconfig_waitrequest_from_ext_avmm_master. • Connecting input signals: rx_manual and rx_is_lockedtodata. 	
Added Example Design options in the SDI II parameter editor.	

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI II IP Core User Guide](#)
- [Errata for SDI II IP Core in the Knowledge Base](#)

SDI II IP Core v14.0

Table 43-4: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Updated reconfiguration logic for enhanced rate switching stability.	-
Increased HD Dual Link timing difference requirement between links, in compliance with SMPTE372.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI II IP Core User Guide](#)
- [Errata for SDI II IP Core in the Knowledge Base](#)

SDI II IP Core v13.1

Table 43-5: v13.1 November 2013

Description	Impact
Added support for segmented frame video format.	-
Added option for easier HD-SDI single-rate only reference clock selection.	-
Added ATX and CMU PLL selections for Arria V GZ and Stratix V devices.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI II IP Core User Guide](#)
- [Errata for SDI II IP Core in the Knowledge Base](#)

SDI Audio IP Cores Revision History 44

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SDI Audio IP Cores v14.0

Table 44-1: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Removed support for Cyclone III and Stratix III devices.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SDI Audio IP Cores User Guide](#)
- [Errata for SDI IP Core in the Knowledge Base](#)

SDI Audio IP Cores v13.1

Table 44-2: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none">• Arria GX• Cyclone and Cyclone II• HardCopy III and HardCopy IV• Stratix, Stratix GX, Stratix II, and Stratix II GX	-

Related Information

- [Introduction to Altera IP Cores](#)

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- [SDI Audio IP Cores User Guide](#)
- [Errata for SDI IP Core in the Knowledge Base](#)

SerialLite II Revision History 45

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SerialLite II v14.0

Table 45-1: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SerialLite II IP Core User Guide](#)
- [Errata for SerialLite II IP Core in the Knowledge Base](#)

SerialLite II v13.1

Table 45-2: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none">• Arria GX• HardCopy IV• Stratix GX and Stratix II GX	-
OpenCore Plus feature will not be supported for Arria V, Arria V GX, Cyclone V, and Stratix V devices.	-

Related Information

- [Introduction to Altera IP Cores](#)

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- [SerialLite II IP Core User Guide](#)
- [Errata for SerialLite II IP Core in the Knowledge Base](#)

SerialLite III Streaming IP Core Revision History 46

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SerialLite III Streaming IP Core v14.1

Table 46-1: Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added support for 17.4 Gbps data rate in variations that target an Arria 10 device. In the parameter editor, added support for the value of 17.4 Gbps for the Transceiver data rate per lane parameter in variations that target an Arria 10 device.		

Related Information

- [SerialLite III Streaming MegaCore Function User Guide](#)
- [Errata for SerialLite III Streaming IP core in the Knowledge Base](#)

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SerialLite III Streaming IP Core v14.0 Arria 10 Edition

Table 46-2: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
<p>Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).</p> <p>SerialLite III IP core variations that target an Arria 10 device have the following differences from the variations that target earlier device families.</p>	<p>This IP core requires manual regeneration and reconnection in your design. You cannot use the standard process in the Quartus II IP Upgrade tool to upgrade this IP core. Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your SerialLite III IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.</p>	
<p>Arria 10 variations have a new IP core name in the IP Catalog. Instead of SerialLite III Streaming, the Arria 10 IP core name is Arria 10 SerialLite III Streaming.</p>	<p>When you begin the regeneration process by selecting the IP core, note the change in IP core name in the IP Catalog.</p>	
<p>Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core in your design.</p>	<p>Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.</p>	<p>The new interface signals are listed in Table 46-3.</p>
<p>Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, these variations have an internal reconfiguration controller that you access through an Avalon-MM interface.</p>	<p>Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.</p>	<p>The new interface signals are listed in Table 46-3.</p>
<p>You must select the value for the Transceiver reference clock frequency parameter from a drop-down menu. The SerialLite III Streaming parameter editor does not automatically set the value for Arria 10 variations.</p>		<p>Parameter editor change.</p>

Description	Impact	Notes
The Device speed grade parameter is not available in the SerialLite III parameter editor for variations that target an Arria 10 device.		Parameter editor change.
If you specify the Source direction, you must set the value of the Transceiver reference clock frequency parameter to none . Arria 10 Source variations do not receive the transceiver TX reference clock as an input signal, and therefore this parameter does not modify the SerialLite III IP core.		Parameter editor change.
Currently, Arria 10 variations do not provide support for Transceiver data rate per lane greater than 15.625 Gbps.		
Currently, Altera does not provide a hardware design example for Arria 10 variations.		
The testbench you can generate from the SerialLite III parameter editor for Arria 10 variations is only available for Sink and Duplex directions. If your IP core has the value of the Direction parameter set to Source , the testbench does not simulate correctly with the IP core.		Testbench availability change.
The testbench you can generate from the SerialLite III parameter editor for Arria 10 variations automatically forces the DUT meta frame length to 200 words. If you specify a different value for the Meta frame length parameter, your IP core retains the value you specify, but when the testbench runs it simulates with the IP core meta frame length set to 200 words.		Testbench behavior change.

Table 46-3: SerialLite III Streaming IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_serial_clk[N-1:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. N is the number of IP core lanes.
—	tx_pll_locked	

Old Signal Name	New Signal Name	Notes
phy_mgmt_clk	phy_mgmt_clk	In Arria 10 variations, this interface provides access to control Arria 10 transceiver reconfiguration, by connecting directly to the reconfiguration interface of the included Arria 10 Native PHY IP core. In Arria 10 variations, the width of <code>phy_mgmt_addr</code> is a value in the range of 11 to 16, depending on the number of lanes. (M is 10 to 15).
phy_mgmt_clk_reset	phy_mgmt_clk_reset	
phy_mgmt_read	phy_mgmt_read	
phy_mgmt_write	phy_mgmt_write	
phy_mgmt_addr[8:0]	phy_mgmt_addr[M:0]	
phy_mgmt_readdata[31:0]	phy_mgmt_readdata[31:0]	
phy_mgmt_waitrequest	phy_mgmt_waitrequest	
phy_mgmt_writedata[31:0]	phy_mgmt_writedata[31:0]	
reconfig_busy	reconfig_busy	Arria 10 variations of the IP core ignore this input signal.
xcvr_pll_ref_clk	xcvr_pll_ref_clk	Arria 10 Source-only variations of the IP core ignore this input signal.
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V GZ and Stratix V variations. This interface is present only in Arria V GZ and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Information

- [SerialLite III Streaming MegaCore Function User Guide](#)
- [Errata for SerialLite III Streaming IP core in the Knowledge Base](#)

SerialLite III Streaming IP Core v14.0

Table 46-4: Version 14.0 June 2014

Description	Impact	Notes
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .		
Changed component subfolder name from <code>seriallite_iii</code> to <code>seriallite_iii_sv</code> .		

Related Information

- [Introduction to Altera IP Cores](#)
- [SerialLite III Streaming MegaCore Function User Guide](#)
- [Errata for SerialLite III Streaming IP core in the Knowledge Base](#)

SerialLite III Streaming IP Core v13.1

Table 46-5: Version 13.1 November 2013

Description	Impact	Notes
Added support for CRC-32 error injection.		
Added support for FIFO ECC protection.		

Related Information

- [SerialLite III Streaming MegaCore Function User Guide](#)
- [Errata for SerialLite III Streaming IP core in the Knowledge Base](#)

SerialLite III Streaming IP Core v13.0

Table 46-6: Version 13.0 May 2013

Description	Impact	Notes
Initial release.		

Related Information

- [SerialLite III Streaming MegaCore Function User Guide](#)
- [Errata for SerialLite III Streaming IP core in the Knowledge Base](#)

SmartVID Controller IP Core Revision History 47

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SmartVID Controller v14.1

Table 47-1: v14.1 December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [SmartVID Controller User Guide](#)
- [Errata for SmartVID Controller IP core in the Knowledge Base](#)

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Stratix V Hard IP for PCI Express IP Core Revision History **48**

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Stratix V Hard IP for PCI Express IP Core v14.1

Table 48-1: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Related Information

- [Introduction to Altera IP Cores](#)
- [Stratix V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Stratix V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Stratix V Hard IP for PCI Express in the Knowledge Base](#)

Stratix V Hard IP for PCI Express IP Core v14.0

Table 48-2: v14.0 June 2014

Description	Impact
Added preliminary support for Stratix V Hard IP for PCI Express with SR-IOV (Single Root I/O Virtualization).	-

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Description	Impact
<p>Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core).</p> <ul style="list-style-type: none"> • Revised programming model and optimized the performance of the Descriptor Controller. • Added support for either 128- or 256-bit interface to the Application Layer. • Added support for 64-bit addressing, making address translation unnecessary. • Added support for optional bursting RX Master for BAR2. • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. • Due to the many changes, the support level has reverted to preliminary. 	<p>The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to v14.0. Altera no longer support v13.1.</p>
<p>Made the following changes to the Avalon-MM Stratix V Hard IP for PCI Express IP core:</p> <ul style="list-style-type: none"> • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. • Added support for 64-bit addressing, making address translation unnecessary. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM. • Increased CRA address to 14 bits from 12 bits. 	<p>All of these new features are optional. If you include an optional feature that changes the port signature of your IP core, you must regenerate your design and connect the signals</p>
<p>Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i>.</p>	<p>-</p>

Related Information

- [Introduction to Altera IP Cores](#)
- [Stratix V Avalon-ST Interface for PCIe Solutions User Guide](#)

- [Stratix V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Stratix V Hard IP for PCI Express in the Knowledge Base](#)

Stratix V Hard IP for PCI Express IP Core v13.1

Table 48-3: v13.1 November 2013

Description	Impact
Support for a Avalon-MM 256-Bit Hard IP for PCI Express Gen3 ×8 with DMA is final.	-
Support for Gen2 CvP is removed.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Stratix V Avalon-ST Interface for PCIe Solutions User Guide](#)
- [Stratix V Avalon-MM Interface for PCIe Solutions User Guide](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for Stratix V Hard IP for PCI Express in the Knowledge Base](#)

Triple Speed Ethernet IP Core Revision History 49

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Triple Speed Ethernet IP Core v14.0 Arria 10 Edition

Table 49-1: v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition , all of the changes require that you regenerate the IP core manually and reconnect it in your design.

Related Information

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

Triple Speed Ethernet IP Core v14.0

Table 49-2: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added ECC support for M20K blocks.	Optional changes. If you do not upgrade your IP core, it does not have these new features:
Added 1588v2 support for LVDS variant.	

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Related Information

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

Triple Speed Ethernet IP Core v13.1 Arria 10 Edition

Table 49-3: v13.1 Arria 10 Edition December 2014

Description	Impact
Added support for Arria 10 devices.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

Triple Speed Ethernet IP Core v13.1

Table 49-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix II and Stratix II GX 	-
Added 1588v2 support for Arria V, Arria V SoC, Cyclone V, Cyclone V SoC and Stratix V devices.	-
Added 1588v2 support for MAC-only variants	-
Added ATX and CMU Tx PLL options for variations that include the PCS block targeting Arria V GZ and Stratix V devices.	-
Added SyncE support by separating Tx PLL and Rx PLL reference clock.	-
The period in nanosecond for csr registers: tx_period, rx_period, Period, and AdjustPeriod, was changed from bit 16 to 19 to bit 16 to 24.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

Video and Image Processing Suite Revision History 50

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Caution: The Clipper, Test Pattern Generator, and 2D Median Filter IP cores are scheduled for product obsolescence and discontinued support as described in [PDN1410](#). Therefore, Altera does not recommend use of these IP cores in new designs. For more information about Altera's current IP offering, refer to Altera's [Intellectual Property](#) website.

Video and Image Processing Suite v14.1

Table 50-1: v14.1 December 2014

Description	Impact
Updated the parameters for Clocked Video Input II and Clocked Video Output II IP cores. <ul style="list-style-type: none">Edited the function of the Use control port parameter. The control ports will now only appear when you turn on this parameter.Removed the Generate Display Port output parameter.	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Video and Image Processing Suite User Guide](#)
- [Errata for the Video and Image Processing Suite in the Knowledge Base](#)

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Video and Image Processing Suite v14.0 Arria 10 Edition

Table 50-2: v14.0 Arria 10 Edition August 2014

Description	Impact
<p>Added support for Arria 10 devices only in the following IP cores:</p> <ul style="list-style-type: none"> • Avalon-ST Video Monitor • Broadcast Deinterlacer • Clipper II • Clocked Video Input II • Clocked Video Output II • Color Space Converter II • Deinterlacer II • Frame Buffer II • Mixer II • Scaler II • Switch II • Test Pattern Generator II 	-

Related Information

- [Introduction to Altera IP Cores](#)
- [Video and Image Processing Suite User Guide](#)
- [Errata for the Video and Image Processing Suite in the Knowledge Base](#)

Video and Image Processing Suite v14.0

Table 50-3: v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. You can instantiate the VIP Suite IP cores only from the Qsys IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added new IP cores: Clocked Video Output II, Clocked Video Input II, Color Space Converter II, Mixer II, Frame Buffer II, Test Pattern Generator II, and Switch II.	-
Removed support for Cyclone III and Stratix III devices.	-

Related Information

- [Introduction to Altera IP Cores](#)

- [Video and Image Processing Suite User Guide](#)
- [Errata for the Video and Image Processing Suite in the Knowledge Base](#)

Video and Image Processing Suite v13.1

Table 50-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none">• Arria GX• Cyclone II• HardCopy II, HardCopy III, and HardCopy IV• Stratix, Stratix II, Stratix GX, and Stratix II GX	-
Improved the Broadcast Deinterlacer video-over-film mode scene change.	

Related Information

- [Introduction to Altera IP Cores](#)
- [Video and Image Processing Suite User Guide](#)
- [Errata for the Video and Image Processing Suite in the Knowledge Base](#)

Viterbi IP Core Revision History 51

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Viterbi IP Core v14.1

Table 51-1: v14.1 December 2014

Description	Impact
Added support for multiple codesets for Arria 10 devices.	-
Added final support for Arria 10 and MAX 10 devices	-

Related Information

- [Viterbi IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Viterbi IP core in the Knowledge Base](#)

Viterbi IP Core v14.0 Arria 10 Edition

Table 51-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Added two new buses, <code>sink_data</code> and <code>out_data</code> , which includes all Avalon-ST compliant data signals, when you instantiate the IP core as part of a Qsys system.	-

Related Information

- [Viterbi IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Viterbi IP core in the Knowledge Base](#)

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Viterbi IP Core v14.0

Table 51-3: v14.0 June 2014

Description	Impact
Removed support for Cyclone III and Stratix III devices.	-
Added preliminary support for MAX 10 FPGAs	-
Added support for IP Catalog. For more information about IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Viterbi IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Viterbi IP core in the Knowledge Base](#)

Viterbi IP Core v13.1

Table 51-4: v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix, Stratix II, Stratix GX, and Stratix II GX 	-
Added full support for Arria V and Stratix V devices	-

Related Information

- [Viterbi IP Core User Guide](#)
- [Introduction to Altera IP Cores](#)
- [Errata for Viterbi IP core in the Knowledge Base](#)

V-Series Avalon-MM DMA for PCI Express IP Core

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V-Series Avalon-MM DMA PCI Express IP Core v14.1

Table 52-1: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.
Added support for 128-Bit Avalon-MM RX master.	If you add this Avalon-MM RX master to your design, you must regenerate your IP core.

Related Information

- [Introduction to Altera IP Cores](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for V-Series Avalon-MM DMA Interface for PCI Express in the Knowledge Base](#)

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V-Series Avalon-MM DMA PCI Express IP Core v14.0

Table 52-2: v14.0 December 2014

Description	Impact
<p>Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core).</p> <ul style="list-style-type: none"> Revised programming model and optimized the performance of the Descriptor Controller. Added support for either 128- or 256-bit interface to the Application Layer. Added support for 64-bit addressing, making address translation unnecessary. Added support for optional bursting RX Master for BAR2. Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. Due to the many changes, the support level has reverted to preliminary. 	<p>The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to v14.0. Altera no longer support v13.1.</p>

Related Information

- [Introduction to Altera IP Cores](#)
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
- [Errata for V-Series Avalon-MM DMA Interface for PCI Express in the Knowledge Base](#)

XAUI PHY IP Core v14.1 Revision History

Table 53-1: v14.1 December 2014

Description	Impact
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.
Added the Enable phase compensation FIFO parameter.	-
Added the <code>xgmii_rx_inclk</code> port, which is available when Enable phase compensation FIFO is enabled.	-
Added the <code>pll_cal_busy_i</code> port, which connects to the <code>pll_cal_busy</code> output port of the external PLL.	-
Added a new Arria 10 SDC constraint requirement. Refer to the "XAUI PHY TimeQuest SDC Constraint" section of the <i>Arria 10 Transceiver PHY User Guide</i> .	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

XAUI PHY IP Core v14.0 Arria 10 Revision History

Table 53-2: v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices. To use the XAUI PHY IP core for Arria 10 devices, you must instantiate an external transmit PLL. You can only use the ATX PLL IP core with the XAUI PHY IP core for Arria 10 devices.	-
Added Enable dynamic reconfiguration parameter.	-
Removed the following parameters: <ul style="list-style-type: none"> • PLL type. • External PMA control and configuration. 	-
Added new port to enable connectivity with an external transmit PLL and with the dynamic reconfiguration interface. Refer to the <i>Arria 10 Transceiver PHY User Guide</i> parameter and port descriptions.	-
The XAUI PHY IP core does not support NCSIM simulator. You will see an error message during elaboration.	-
The XAUI PHY IP core does not support VHDL. You will get a compilation error when you simulate the XAUI PHY IP core generated in VHDL. You must generate this IP core in Verilog.	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

XAUI PHY IP Core v14.0 Revision History

Table 53-3: v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)

- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

XAUI PHY IP Core v13.1 Revision History

Table 53-4: v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Information

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Other IP Cores Product Revision History 54

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ALTERA_FP_MATRIX_MULT v14.1

Table 54-1: v14.1 December 2014

Description	Impact
Added support for Arria 10 device hard floating-point blocks.	Only for new IP cores.
Changed reset port. It is no longer optional and is always present	
Removed option to add an enable port	
Changed performance. Specify twice the number of memory blocks compared to previous version for the equivalent performance	
Changed the signals to use Avalon-ST interfaces.	Only for new IP cores. Any existing IP cores continue to have the same signals even when you edit and regenerate the IP core.
Changed <code>reset</code> to active low	

Related Information

- [Floating-Point Megafunctions User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera Advanced SEU Detection IP Core v14.1

Table 54-2: v14.1 December 2014

Description	Impact
Added support for double-adjacent SEU sensitivity processing.	Initiates an <code>.smh</code> lookup for correctable double-adjacent EDCRC errors instead of identifying such SEU as critical.

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Description	Impact
Added <code>critical_clear</code> signal to errors interface	-
Added <code>busy</code> signal to errors interface	For on-chip processing configuration only.

Related Information

- [Advanced SEU Detection IP Core User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera Dual Configuration v14.0 Update 2

Table 54-3: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- [MAX 10 FPGA Configuration User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera EMR Unloader IP Core v14.1

Table 54-4: v14.1 December 2014

Description	Impact
Fixed an issue with synchronization the of <code>CRCERROR</code> signal, which comes from the EDCRC circuitry that the internal oscillator drives.	-

Related Information

- [Advanced SEU Detection IP Core User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera OCT IP Core v14.0 Arria 10 Edition

Table 54-5: v14.0 Arria 10 Edition August 2014

Description	Impact
<ul style="list-style-type: none"> Changed signal names Added user mode OCT 	

Table 54-6: Signal Name Changes

Old Name	New Name	Notes
core_rzqin_export	rzqin	-
core_series_termination_control_expor	oct_#_series_termination_control	-
core_parallel_termination_control_export	oct_#_parallel_termination_control	-

Related Information

- [Altera OCT Megafunction User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera GPIO IP Core v14.0 Arria 10 Edition

Table 54-7: v14.0 Arria 10 Edition August 2014

Description	Impact
Changed signal names	-

Table 54-8: Signal Name Changes

Old Name	New Name	Notes
core_ck_fr_in_export	ck_fr_in	
core_ck_fr_out_export	ch_fr_out	
core_ck_hr_in_export	ch_hr_in	
core_ck_hr_out_export	ch_hr_out	
core_dout_export	dout	
core_din_export	din	
core_oe_export	oe	

Old Name	New Name	Notes
core_pad_io_export	pad_io	
core_pad_io_b_export	pad_io_b	
core_aclr_export	aclr	
core_sclr_export	sclr	
core_cke_export	cke	
core_ck_export	ck	
core_ck_in_export	ck_in	
core_ck_out_export	ck_out	
core_ck_fr_export	ck_fr	
core_ck_hr_export	ck_hr	
core_pad_in_export	pad_in	
core_pad_in_b_export	pad_in_b	
core_pad_out_export	pad_out	
core_pad_out_b_export	pad_out_b	
core_aset_export	aset	
core_sset_export	sset	

Related Information

- [Altera GPIO Megafunction User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera GPIO Lite IP Core v14.0 Update 2

Table 54-9: v14.0 Update 2 September 2014

Description	Impact
Initial release.	

Related Information

- [MAX 10 General Purpose I/O User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera Modular ADC IP Core v14.0 Update 2

Table 54-10: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- [MAX 10 Analog to Digital Converter User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera LVDS SERDES IP Core v14.1

Table 54-11: v14.1 December 2014

Description	Impact
Added internal PLL additional clock export parameter	-

Related Information

- [Altera LVDS SERDES Megafunction User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera LVDS SERDES IP Core v14.0 Arria 10 Edition

Table 54-12: v14.0 Arria 10 Edition August 2014

Description	Impact
Added feature that creates .sdc file for generated designs (previously only for example designs)	-
Added support for external PLL mode	-
Added option to clock TX core registers using reference clock	-

Related Information

- [Altera LVDS SERDES Megafunction User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera PHYLite for Memory IP Core v14.1

Table 54-13: v14.1 December 2014

Description	Impact
Added internal PLL additional clock export parameter	-
Added setup delay constraint timing parameters in the Group tabs in the parameter editor	-

Related Information

- [Altera PHYLite for Memory Megafunction User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera PHYLite for Memory IP Core v14.0 Arria 10 Edition

Table 54-14: v14.0 Arria 10 Edition August 2014

Description	Impact
Added dynamic reconfiguration	-
Added I/O standard and OCT settings	-
Added complementary strobe type	-
Changed pll_locked port name to interface_locked	-

Related Information

- [Altera PHYLite for Memory Megafunction User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera On-Chip Flash IP Core v14.1

Table 54-15: v14.1 December 2014

Description	Impact
<p>Added new parameters:</p> <ul style="list-style-type: none"> • Data interface parameter. • Read burst count parameter. Adjusts the maximum burst count for Incrementing read mode. Also autoadjusts <code>burstcount</code> bus width. • Serial data interfaces • Flash Memory. Indicates the address mapping for each sector and adjusts the Access Mode for each sector individually 	-
Replaced Dual Images parameter with Configuration Scheme and Configuration Mode parameters which includes all supported configuration modes. Use CFM as UFM during single image configuration mode without memory initialization.	
Fixed a bug, which allows you to adjust the Read burst count from 1 to 2 or 4 while using WrappingRead burst mode .	

Related Information

- [MAX 10 User Flash Memory User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera On-Chip Flash IP Core v14.0 Update 2

Table 54-16: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-

Related Information

- [MAX 10 User Flash Memory User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Altera Soft LVDS IP Core v14.0 Update 2

Table 54-17: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-
Related Information	
<ul style="list-style-type: none">• MAX 10 High-Speed LVDS I/O User Guide• Errata for other IP cores in the Knowledge Base	

Arria 10 Native Fixed Point DSP IP Core v14.1

Table 54-18: v14.1 December 2014

Description	Impact
Initial release. Only supports Arria 10 device family.	-
Related Information	
<ul style="list-style-type: none">• Arria 10 Native Fixed Point DSP IP Core User Guide• Errata for other IP cores in the Knowledge Base	

Internal Oscillator IP Core v14.0 Update 2

Table 54-19: v14.0 Update 2 September 2014

Description	Impact
Initial release.	-
Related Information	
<ul style="list-style-type: none">• MAX 10 Clocking and PLL User Guide• Errata for other IP cores in the Knowledge Base	

RAM: 1-port and RAM: 2-port v14.0 Arria 10 Edition

Table 54-20: v14.0 Arria 10 Edition August 2014

Description	Impact
Changed GUI. When upgrading, you lose any value in Memory Initial Mode > File name . For the work around, refer to the Knowledge Base .	-

Related Information

- [Internal Memory \(ROM and RAM\) User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

SLD Hub Controller System v14.1

Table 54-21: v14.1 December 2014

Description	Impact
Enhanced the register map	The pre-v14.1 and v14.1 register maps are similar. Pre v14.1 register maps work unchanged with v14.1 hardware.

Related Information

[Errata for other IP cores in the Knowledge Base](#)

Other Transceiver IP Cores Product Revision History **55**

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Transceiver PHY Reset Controller IP Core v14.1 Revision History

Table 55-1: v14.1 December 2014

Description	Impact
Added an optional port <code>pll_cal_busy</code> . To enable <code>pll_cal_busy</code> select Enable pll_cal_busy input port parameter under the TX Channel option in the Reset Controller IP Core parameter editor. If not enabled, then by default, this port is connected to 1'b0.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

Transceiver PHY Reset Controller IP Core v14.0 Arria 10 Revision History

Table 55-2: v14.0 Arria 10 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

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Transceiver PHY Reset Controller IP Core v13.0 Arria 10 Revision History

Table 55-3: v13.0 Arria 10 December 2013

Description	Impact
Initial release for Arria 10 devices.	-

Related Information

- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for Transceiver IP Cores in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)