Nios II Performance Benchmarks

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Performance Benchmarks Overview

This data sheet lists the performance and logic element (LE) usage for the Nios® II soft processor and peripherals. The Nios II soft processor is configurable and designed for implementation in Altera® FPGAs. The following Nios II processors were used for these benchmarks:

- Nios II/f—The Nios II/f "fast" processor is designed for high performance while presenting the most configuration options which are unavailable in the other Nios II processors.
- Nios II/s—The Nios II/s "standard" processor is designed for small size while maintaining moderate performance.
- Nios II/e—The Nios II/e "economy" processor is designed for the smallest possible processor size while providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

Note: Results may vary slightly depending on the version of the Quartus® II software, the version of the Nios II processor, and the target device. Also, any changes to the system logic design might change the performance and LE usage. All results are generated using Qsys-based designs;

The *f_{max} for Nios II Processor System (MHz)* and *MIPS for Nios II Processor System* tables list the f_{max} and millions of instructions per second (MIPS) for a system with the following components:

- Nios II processor with JTAG debug module
- JTAG UART
- 64 KB On-chip memory (Cyclone® designs use 1MB of off-chip SDR SDRAM)
- Avalon® Memory-Mapped (Avalon-MM) pipeline bridge
- Timer

The MIPS reports were obtained using the MIPS* (*Dhrystones 2.1 benchmark). You can download the Dhrystones 2.1 benchmark software from the **Nios II Embedded Processor Design Examples** page on the Altera website. For more information about the Dhrystones 2.1 benchmark software, refer to the readme.txt file which is included in the Dhrystones 2.1 benchmark design example.

The Fast design example illustrates a system that has all the components listed. You can download the Fast design example from the **Nios II Embedded Processor Design Examples** page on the Altera website. For more information about the Fast design example, refer to the readme.txt file which is included in the Fast design example.

Table 1: f_{max} for Nios II Processor System (MHz)

Device Family	Device used	Nios II/f[1]	Nios II/s[1]	Nios II/e[1]
Stratix V	5SGXEA7N2F45C1	360	280	410
Stratix IV	EP4S100G5H40I1	240	240	280
Cyclone V	5CGXFC7D6F31C6	170	150	220
Cyclone IV	EP4CGX30CF19C6	160	120	170
Arria V GZ	5AGZME7K2F40C3	300	270	370
Arria V	5AGXFB5K4F40I3	170	180	250
Arria II GX	EP2AGX260FF35I3	170	170	300

Table 2: MIPS for Nios II Processor System

Device Family	Nios II/f[1][2]	Nios II/s[1][2]	Nios II/e[1][2]
Stratix V	407	179	62
Stratix IV	271	154	42
Cyclone V	192	96	33
Cyclone IV GX	181	77	26
Arria V GZ	339	173	56
Arria V	192	115	38
Arria II GX	192	109	45

Table 3: f_{max} for Nios II Gen 2 Processor System (MHz)

Device Family	Device used	Nios II/f[1]	Nios II/e[1]
Stratix V	5SGXEA7N2F45C1	350	430
Stratix IV	EP4S100G5H40I1	240	290
Cyclone V	5CGXFC7D6F31C6	170	220
Cyclone IV	EP4CGX30CF19C6	150	170
Arria V GZ	5AGZME7K2F40C3	280	370
Arria V	5AGXFB5K4F40I3	180	250
Arria II GX	EP2AGX260FF35I3	170	300

Table 4: MIPS for Nios II Gen 2 Processor System

Device Family	Nios II/f[1][2]	Nios II/e[1][2]
Stratix V	396	65

(1) Results were generated using push button Analysis, Synthesis and Fitter settings in the Quartus II software.
(2) All the MIPS results are based on estimations.

Device Family	Nios II/f[1][2]	Nios II/e[1][2]
Stratix IV	271	44
Cyclone V	192	33
Cyclone IV GX	170	26
Arria V GZ	316	56
Arria V	203	38
Arria II GX	192	45

Table 5: MIPS/MHz ratio for Nios II and Nios II Gen 2 Processor System on Various Device Families

Device Family	Nios II/F	Nios II/S	Nios II/E
Stratix V	1.13	0.64	0.15
Stratix IV	1.13	0.64	0.15
Cyclone V	1.13	0.64	0.15
Cyclone IV GX	1.13	0.64	0.15
Arria V GZ	1.13	0.64	0.15
Arria V	1.13	0.64	0.15
Arria II GX	1.13	0.64	0.15

The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. These results represent typical results. Your results may vary.

Table 6: LE Usage for Nios II Processor Cores and Peripherals - Stratix V and Stratix IV devices

Processor Core / Peripheral	Stratix V (ALMs)	Stratix IV (ALUTs)
Nios II/F[3]	766	1160
Nios II/S[4]	498	792
Nios II/E[5]	264	524
Nios II JTAG debug module	120	169
UART	61	95
JTAG UART	60	114
RAM Controller	2678[6]	3735
Timer	70	92

(3) The Nios II/f processor used has 512-byte instruction, 512-byte data caches, and hardware multiplier.
(4) The Nios II/s processor used has 512-bytes instruction, hardware multiplier and no data caches.
(5) The Nios II/e processor used has no instruction or data caches, and no hardware multiplier.
(6) The RAM controller for this device is based on DDR3 SDRAM Controller with UniPHY.

Table 7: LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Stratix V and Stratix IV devices

Processor Core / Peripheral	Stratix V (ALMs)	Stratix IV (ALUTs)
Nios II/f[7]	726	1127
Nios II/e[8]	271	541
Nios II JTAG debug module	117	170
UART	61	90
JTAG UART	59	116
RAM Controller	2715[6]	3773
Timer	71	97

Table 8: LE Usage for Nios II Processor Cores and Peripherals - Cyclone V and Cyclone IV GX

Processor Core / Peripheral	Cyclone V (ALMs)	Cyclone IV (ALUTs)
Nios II/f[3]	812	2200
Nios II/s[4]	572	1481
Nios II/e[5]	287	747
Nios II JTAG debug module	118	323
UART	61	144
JTAG UART	60	155
RAM Controller	2427[6]	441
Timer	70	141

Table 9: LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Cyclone V and Cyclone IV GX devices

Processor Core / Peripheral	Cyclone V (ALMs)	Cyclone IV GX
Nios II/f[7]	835	2229
Nios II/e[8]	289	786
Nios II JTAG debug module	118	328
UART	62	145
JTAG UART	59	160
RAM Controller	2438[6]	436
Timer	70	141

(7) The Nios II Gen2/f processor used has 512-byte instruction, 512-byte data caches and hardware multiplier.
(8) The Nios II Gen2/e processor used has no instruction or data caches, and no hardware multiplier.

Table 10: LE Usage for Nios II Processor Cores and Peripherals - Arria V GZ, Arria V, and Arria II GX devices

Processor Core / Peripheral	Arria V GZ (ALMs)	Arria V (ALMs)	Arria II (ALUTs)
Nios II/f[3]	766	752	1162
Nios II/s[4]	496	505	859
Nios II/e[5]	263	287	559
Nios II JTAG debug module	117	117	169
UART	55	56	98
JTAG UART	59	58	113
RAM Controller	2554[6]	2391	313
Timer	57	57	91

Table 11: LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Arria V GZ, Arria V and Arria II devices.

Processor Core / Peripheral	Arria V GZ (ALMs)	Arria V (ALMs)	Arria II (ALUTs)
Nios II/f[7]	748	763	1143
Nios II/e[8]	269	286	569
Nios II JTAG debug module	113	114	169
UART	55	56	94
JTAG UART	59	59	116
RAM Controller	2574[6]	2395	324
Timer	57	57	101

Additional performance benchmarking information for the Nios II processor can be found at the following links:

For more information about the Nios II interrupt latency performance, refer to the **Exception Handling** chapter of the Nios II Software Developer's Handbook.

For more information about the Nios II floating-point custom instruction performance, refer to the **Using Nios II Floating-Point Custom Instructions Tutorial**.

For more information about the Nios II networking applications performance, refer to **AN440: Accelerating Nios II Networking Applications**.

Document Revision History

Data	Version	Changes
August 2014	11.0	• Updated data and device families in Table 1: fmax for Nios II Processor System (MHz) • Updated data and device families in Table 2: MIPS for Nios II Processor System • Added Table 3: fmax for Nios II Gen 2 Processor System (MHz) • Added Table 4: MIPS for Nios II Gen 2 Processor System (MHz) • Updated data and device families for Table 5: MIPS/MHz Ratio for Nios II and Nios II Gen 2 Processor System on various Device Families • Updated data and device families for Table 6: LE Usage for Nios II Processor Cores and Peripherals - Stratix V and Stratix IV devices • Added Table 7:LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Stratix V and Stratix IV Devices • Updated data for Table 8: LE Usage for Nios II Processor Cores and Peripherals - Cyclone V and Cyclone IV GX • Added Table 9: LE Usage for Nios II Gen 2 Processor Cores and Peripherals - Cyclone V and Cyclone IV GX devices • Updated data for Table 10: LE Usage for Nios II Processor Cores and Peripherals - Arria V GZ, Arria V, and Arria II GX devices. • Added Table 11:LE Usage for Nios II Processor Cores and Peripherals - Arria V GZ, Arria V and Arria II devices.

Data	Version	Changes
Novemeber 2013	10.0	• Removed information for devices that Altera no longer supports: Arria, Cyclone, Cyclone II, Stratix, Stratix II, and all HardCopy series. • Updated performance and LE usage for Arria II GX, Arria V, Arria V GZ, Stratix IV, and Stratix V devices with the Quartus II version 13.1 software. • Added performance and LE usage for Cyclone V devices with the Quartus II version 13.1 software.
July 2013	9.0	• Measured performance and LE usage for Stratix V and Arria V devices with the Quartus II version 13.0 software • Updated new information for Stratix V and Arria V devices. • Added new information for Arria V GZ devices. • Removed information for Cyclone V devices.
December 2012	8.0	• Measured performance and LE usage with the Quartus II version 12.1 software and the Nios II version 12.1 processor. • Added new information for Cyclone V and Arria V devices. • Updated all tables with new data.
June 2011	7.0	• Measured performance and LE usage with the Quartus II version 11.0 software and the Nios II version 11.0 processor. • Updated all tables with new data.

Data	Version	Changes
July 2010	6.0	• Measured performance and LE usage with the Quartus II version 13.0 software and the Nios II version 10.0 processor. • Rearranged the logic element usage for Nios II processor cores and peripherals for HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix from table 5 to table 6. • Added new information for Stratix V device. • Updated all tables with new data.
February 2010	5.0	• Measured performance and LE usage with the Quartus II version 9.1 software and the Nios II version 9.1 processor. • Added new information for the Cyclone III LS, Cyclone IV GX, and HardCopy IV devices. • Updated information for Arria II GX devices. • Updated Table 1, Table 2, Table 3, Table 5, and Table 6 with new data.
June 2009	4.0	• Measured performance and LE usage with the Quartus II version 9.0 SP1 software and the Nios II version 9.0 SP1 processor. • Added information for the HardCopy III, Arria II GX, and Arria GX devices. • Updated Tables 1 and 2 with new data. • Added Table 6.

Data	Version	Changes
July 2008	3.0	• Measured performance and LE usage with the Quartus II version 8.0 software and the Nios II version 8.0 processor. • Added information for the Stratix IV device. • Added links for additional information on Nios II benchmark performance. • Updated Tables 1, 2, 4 and 5 with new data. • Added Table 3.
August 2007	2.0	• Measured performance and LE usage with the Quartus II version 6.1 software and the Nios II version 6.1 processor. • Added information for the Stratix III, HardCopy II, and Cyclone III devices. • Updated Tables 1, 2, and 3 with new data.
October 2004	1.0	Initial release