Artiza Networks Launches the Griffin SmartNIC Based on Intel Agilex® 7 FPGAs and Open FPGA Stack

Artiza Networks' PCIe*-based SmartNIC, the Griffin N6060/61, uses the latest Intel Agilex 7 FPGA F-Series and Open FPGA Stack (OFS) to address a wide range of applications, including virtualized radio access network (vRAN) and network function virtualization (NFV) acceleration, as well as multi-access edge computing (MEC).

Overview

- The Artiza Networks Griffin N6060/61, based on the Intel® FPGA SmartNIC N6000-PL Platform, is shipping today. It is the largest N6000-based SmartNIC supporting the OFS, with 2,692K logic elements (LEs) – twice as many as the N6000 Platform.

- The Griffin SmartNIC's Acceleration Functional Unit (AFU) or workload capability is up to 2.3X higher than the N6000 Platform

- Support for workload development using oneAPI on the Griffin N6061 is currently in planning

Executive Summary

The Intel FPGA SmartNIC N6000-PL Platform is Intel's third-generation SmartNIC, providing 2x100 Gbps Ethernet connectivity to accelerate communication and networking workloads. The Artiza Networks Griffin N6060/61 is the latest production-level N6000 Platform-based card solution. Using the N6000 Platform and OFS as a starting point, Artiza Networks customized the Griffin N6060/61 to incorporate twice as many LEs as the N6000 Platform, enabling larger, higher-performance workloads.

The AFU or 'workload region' can be easily ported from previous Intel programmable acceleration card (PAC) generations without any special modifications, including the Intel FPGA PAC D5005 AFU and Intel FPGA PAC N3000 AFU. By doubling the number of LEs, the AFU capability is also doubled from the N3000 and N6000 platforms.

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Background and Challenge

Artiza Networks is an industry leader in 3G, 4G, and 5G wireless networks, including the radio access network (RAN) and core network (CN) domains. For over 20 years, Artiza has collaborated with the network industry's top vendors and operators in testing the RAN and CN nodes of the world's most advanced mobile networks.

In 2021, Intel announced their latest Intel FPGA SmartNIC N6000-PL Platform, a development platform powered by the Intel Agilex® 7 FPGA F-Series. The N6000 Platform provided significant power and performance enhancements compared to its predecessor, the Intel FPGA PAC N3000. This development platform aimed to support communications and networking workloads over various applications, such as vRAN, virtual cell site router (vCSR), Cloud Native Contrail Networking (CN2), SMTE ST2110, and user plane function (UPF). The N6000 Platform also enhanced the Intel FPGA PAC N3000 forward error correction (FEC) acceleration solution.

Artiza's extensive engineering resources, including expertise in PCB, FPGA, and digital signal processing (DSP) development in wired and baseband formats, coupled with their industry leadership, allowed Artiza to develop their latest SmartNIC, the Griffin N6060/61. The Griffin N6060/61 is an Intel FPGA SmartNIC N6000-PL Platform derivative.

However, by solely providing the card, workload vendors who purchase the Griffin N6060/61 would be left with the burden of devoting resources toward FPGA workload development. This workflow would include hardware and software development, from hardware synthesis, compilation, routing, and timing enhancements to software driver development and orchestration/virtualization. This is a lengthy development cycle that would typically take 9 – 12 months.

Solution

To ease the custom FPGA board development process and the challenge of subsequent workload vendors who would eventually purchase their board, Artiza Networks adopted the OFS.

OFS is an open-source infrastructure that aims to reduce the development time of custom FPGA-based boards and workloads. It is a key foundational tool that enables FPGA developers to expedite and standardize this development by providing a completely open-source infrastructure with reference hardware. The OFS infrastructure includes an FPGA Interface Manager (FIM), commonly called a 'shell,' and an AFU region designated for workload development. Using OFS, board – or FIM – developers can leverage the open-source infrastructure – or base FIM – to quickly develop a tailored, customized FIM for their board based on the target application or industries.

By following the OFS workflow, Artiza Networks inherited an open-source hardware and software infrastructure that served as a starting point for their custom development, significantly reducing time to market. All source code and technical documentation intended for Intel Agilex FPGA-based development is validated and tested on the Intel FPGA SmartNIC N6000-PL Platform that Artiza leveraged. This means that by using OFS out of the box, developers immediately have access to a starting framework – a timing-closed FPGA shell ready to be compiled, working host exercisers, firmware/RTL, a running software and hardware connection, bandwidth, and board monitoring information. Once installed, the server can immediately check the status and functionality of the card.

Another benefit of OFS is that workload vendors now have a library of software drivers connecting the FPGA to the application layer. This frees up Artiza Networks from needing to develop their own FPGA sample designs. This also ensures workload vendors can concentrate on RTL development without significantly modifying the FPGA shell, I/O, or memory.

Results

The Griffin N6060/N6061 sample cards started shipping in June 2023 in Japan, the United States, China, India, and Finland. The card, with FH3/4L slots, is sized for GPU profiles and can be installed in servers with PCIe 4.0 x16. Since the card uses the same ATX 8-pin connectors as a GPU, it can also be installed in servers instead of a GPU.

Artiza Networks plans to continue supplying Griffin N6060/N6061 cards for at least seven years. They also intend to continue developing PCIe-based SmartNICs following the Griffin. The Griffin N6060/N6061 targets vRAN, NFV, and MEC networking applications.

Specification	Griffin N6060/N6061
FPGA	Intel Agilex 7 FPGA F-Series (AGFB027R25A2I2V)
Networking	100 GbE x 2 25 GbE x2 x2 10 GbE x 8
Memory	16 GB DDR4 (FPGA) and 2 GB DDR4 (FPGA embedded CPU)
Network Interface Chip	Intel E810 CAM2
Form Factor	FH3/4L, single slot
PCIe	4.0 x2 x8 bifurcation (N6060) 4.0 x 16 (N6061)
Time Synchronization Function	Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) compatible, with 1 PPS in/out SMA connector
Board Management	Intel MAX® 10 FPGA
Power Consumption	185 W
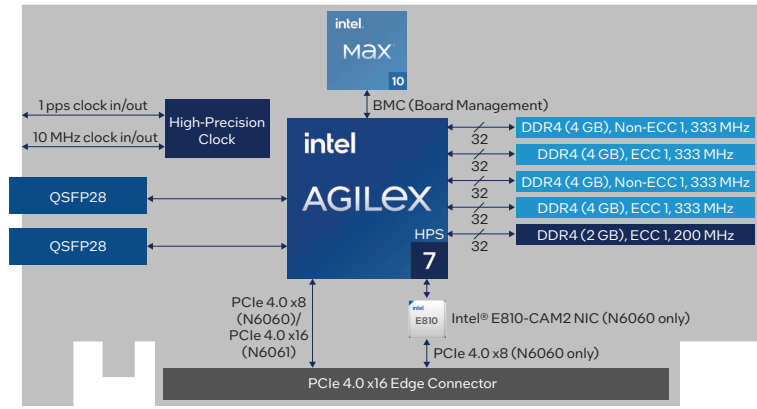
Griffin N6060/N6061 Block Diagram

How to Get Started with FPGA Acceleration Using OFS

FPGA developers can leverage Artiza Network's OFS-enabled Griffin N6060/N6061 SmartNIC and use open-source documentation and source code to get started building their custom workload.

The following table outlines how developers can start FPGA-based workload development using Artiza Network's acceleration board.

Leverage FPGA Acceleration for Your Workload	
Step 1: Choose a board	Browse Artiza Network's OFS-enabled board, the Griffin N6060/N6061 SmartNIC
Step 2: Evaluate OFS open-source resources	Artiza Networks will provide the corresponding version of the OFS technical documentation.
Step 3: Access open-source hardware and software code	Artiza Networks will provide the corresponding OFS software and hardware code. This is their specific distribution of the OFS base code provided by Intel.
Step 4: Develop workload using RTL or C/C++ (using oneAPI[1])	Follow the OFS RTL flow OR OFS enables the compilation of oneAPI kernels. Utilize the oneAPI development flow and build FPGA workloads in C/C++.

[1] oneAPI support is in planning for the Griffin N6061

Find the base Open FPGA Stack source code and documentation provided by Intel at https://github.com/OFS.

Note that all third-party OFS-enabled boards can be browsed in the OFS board catalog.

Learn More

- Learn more about Artiza Networks Griffin N6060/61 SmartNIC powered by the Intel Agilex FPGA
- Get OFS open-source code and documentation
- Learn more about OFS

Quote

"The presence of the PCIe driver and BMC included in OFS contributed to shortening the release time of our board." - Toshio Mitsui, Printed Circuit Board Development Group