AN 432: Using Different PLL Settings Between Stratix II and HardCopy II Devices

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This document describes the proper steps to design Stratix® II and HardCopy® II devices with different PLL settings to achieve a successful HardCopy II Companion Revision Comparison report.

When designing Stratix II devices that will be migrated to HardCopy II devices, it is sometimes necessary to operate the instantiated phase-locked loops (PLLs) using different settings for the Stratix II and HardCopy II projects in the Quartus® II software. However, the different settings present a problem for the HardCopy II Companion Revision Comparison utility, which reports the differences as a failed comparison between the Stratix II and HardCopy II revisions in the Quartus design project.

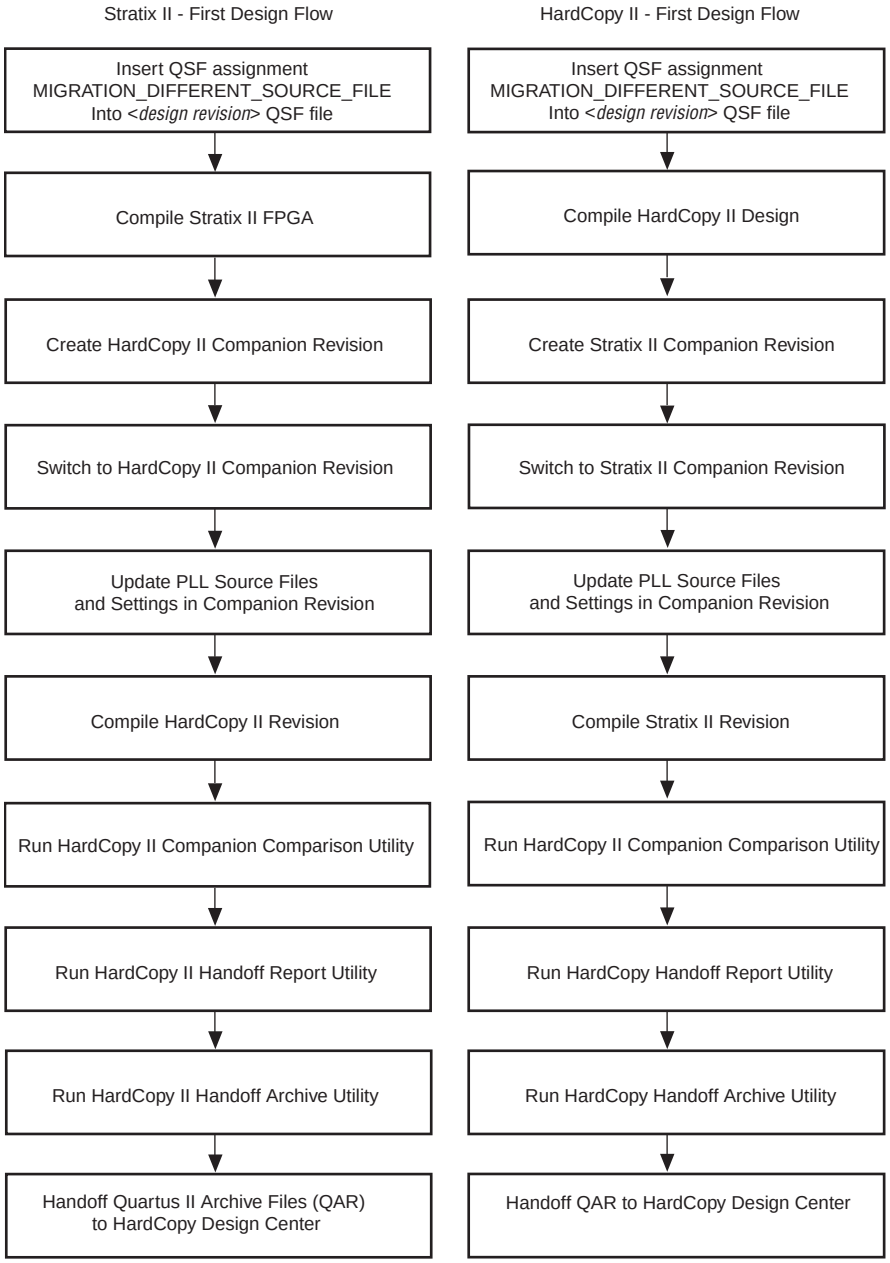
Migration Process With Different PLL Settings

The HardCopy II Companion Revision Comparison is a utility provided by the Quartus II software to ensure that Stratix II and HardCopy II designs are functionally equivalent after migration. This utility must be run in the Quartus II software as part of the HardCopy II design and handoff methodology. The utility identifies any differences in design constraints, timing assignments, and netlist structure. After this information is collected, the utility alerts you of possible design mismatches.

Sometimes the HardCopy II Companion Revision Comparison alerts you of design mismatches that are not actually mismatches, but design constraint differences. There are many circumstances that could cause design constraints for the HardCopy II device and the Stratix II FPGA to differ. For example, to improve the performance of a HardCopy II device without changing the performance of the Stratix II FPGA, you need to modify the PLL-generated clock to provide a higher-frequency clock in the HardCopy II device. Another example is found in DDR memory interfaces, where the clock-phase relationships in the HardCopy II device may need to be set differently from those in the Stratix II FPGA to achieve timing closure for both designs. These types of modifications are accepted by the HardCopy Design Center during the design handoff review. However, they must be handled correctly so that the HardCopy II Companion Revision Comparison utility does not generate any critical errors.

To have different PLL settings, you must have different PLL source files for revisions of Stratix II and HardCopy II devices. Each PLL must have the same module name. However, by default, the module name matches the title of each file name. This section describes how to override the default file naming convention so that you have two PLL files with different names that reference the same module. In addition, you must include an assignment in the Quartus II Settings File (**.qsf**) to specify the different PLL source files for Stratix II and HardCopy II revisions. The **.qsf** assignment is independent of the design flow you choose to use: Stratix II-first or HardCopy II-first design flow. Both design flows follow the same process, as shown in Figure 1. The assignment allows for both VHDL and Verilog source files to be migrated.

Figure 1. Stratix II-First versus HardCopy II-First Design Flow



The original design revision must contain the **.qsf** assignment for the PLL source files that are changed. In the case of a Stratix II-first design flow, the **.qsf** assignment must be in the Stratix II revision before creating the HardCopy II companion revision. Add the following **.qsf** assignment to the original design:

```
set_global_assignment -name MIGRATION_DIFFERENT_SOURCE_FILE <filename>
```

☞ Each MIGRATION_DIFFERENT_SOURCE_FILE assignment can be set for one source file only. You must assign another source file to a new MIGRATION_DIFFERENT_SOURCE_FILE assignment.

Add this assignment before creating the HardCopy II companion revision, which you create using the **Create/Overwrite HardCopy II Companion Revision** in the HardCopy II Utilities found in the **Project** menu of the Quartus II software. After the companion revision is created, the source files identified in the **.qsf** assignment are copied and can be changed to the necessary PLL settings for the HardCopy II design.

Modify the PLL source file manually or with the MegaWizard Plug-In Manager. In either case, the source file list in the **.qsf** of the HardCopy II companion revision must be updated to reflect the use of the new source file.

When the MegaWizard Plug-In Manager updates the new source file, it modifies the top-level name of the module or entity in the source file to match the name of the source file. Therefore, you must rename the module or entity after you have updated the file with the MegaWizard Plug-In Manager so that your top-level design instantiates the PLL with the newly modified PLL design file.

After updating the PLL source file in the HardCopy II revision, verify that the **.qsf** source file setting `set_global_assignment -name <VHDL_FILE|VERILOG_FILE>` <*filename*> contains the newly modified PLL source file. Then compile your HardCopy II device. The new settings for the PLL will be used.

After compilation is complete, run the HardCopy II Companion Revision Comparison utility to observe and track changes made to the PLLs and design settings. These changes are captured as critical warnings in the revision comparison report and must be reviewed by the HardCopy Design Center before the design is accepted for migration.

An example of how this PLL modification process is performed is described in the "Example Design Flow" section.

Example Design Flow

To use different PLL settings between Stratix II and HardCopy II devices, perform the following steps:

1. "Set Up Design"
2. "Compile and Migrate" on page 4
3. "Rename PLL Module" on page 5
4. "Compare Revisions" on page 5

Set Up Design

To illustrate how the PLL modification process should be performed, this section provides an example design migration between a EP2S90F1020C4 device and a HC230F1020C device. The design uses one PLL with a 50-MHz reference clock, and it generates a 100-MHz output clock for the Stratix II design. Name the PLL design file **pll_sii**. The design must run at 200 MHz in a HardCopy II device, but the reference clock to the PLL cannot change on the board design. This means that the PLL multiplication to generate the 200-MHz clock in the HardCopy II revision must be modified, but the 100-MHz clock in the Stratix II revision must remain the same.

The top-level design is called `pll_swap_test` and is shown in the Verilog HDL in Example 1.

Example 1. Top-Level Design for pll_swap_test in Verilog HDL

```
module pll_swap_test(data_in, data_out, ref_clk);
input data_in, ref_clk;
output data_out;
reg data_in_reg, data_out;v
always @ (posedge clk)
 begin
 data_in_reg <= data_in;
 data_out <= ~ data_in_reg;
 end
pll_sii pll_inst (
 .inclk0 ( ref_clk ),
 .c0 ( clk )
 );
endmodule
```

The PLL source file comparison must be flagged to indicate it differs between the Stratix II and HardCopy II revisions. To do so, in the original design revision—the Stratix II design revision in this case—add this assignment to the project's **.qsf** (<*project name*>`.qsf`):

```
set_global_assignment -name MIGRATION_DIFFERENT_SOURCE_FILE pll_sii.v
```

All source files must be listed in the **.qsf** under the design files assignment to prevent the Quartus II software from accidentally selecting a design file that is unlisted in the **.qsf**, but may exist in the project directory or in the user-specified library directories. In this example, the design file `pll_sii.v` must be included in the **.qsf** assignments. The following lines of code list the project's design files:

```
set_global_assignment -name VERILOG_FILE “pll_swap_test.v”
set_global_assignment -name VERILOG_FILE “pll_sii.v”
```

The listing of source files is necessary when the design is migrated to the HardCopy II revision. This is because you will have a separately named source file for the PLL used in the HardCopy II revision with different settings from the one used in the Stratix II revision.

Compile and Migrate

With the migration assignment included above and the PLL source file included in the project's design source files list, compile the Stratix II design and create the HardCopy II companion revision using the HardCopy II Utilities. Once compilation is complete, name the resulting revision `pll_swap_test_hcii` to denote that the revision is the HardCopy II revision of the original design.

Because you used the constraint set_global_assignment `-name MIGRATION_DIFFERENT_SOURCE_FILE pll_sii.v` when you created the HardCopy II companion revision, the Quartus II software creates a copy of the **pll_sii.v** file in the project directory and modifies the name of it to reflect the change. This is reported in the Quartus II message window as shown below:

```
Info: Copied “pll_sii.v” to “pll_sii_pll_swap_test_hcii.v”
```

In the code above, for the project called `pll_swap_test`, a HardCopy II companion revision named `pll_swap_test_hcii` is created using the HardCopy II Utilities. A copy of the source file, **pll_sii.v**, is created by the Quartus II software and named as **pll_sii_pll_swap_test_hcii.v**. To modify the design for the new PLL-generated clock frequency of 200 MHz required for your design, switch to the HardCopy II design revision.

☞ Note that **pll_sii.v** has been replaced by **pll_sii_pll_swap_test_hcii.v** in the **pll_swap_test_hcii.qsf** file. This is done automatically in the Quartus II software version 7.2 and later.

```
set_global_assignment -name MIGRATION_DIFFERENT_SOURCE_FILE pll_sii_pll_swap_test_hcii.v

set_global_assignment -name VERILOG_FILE “pll_swap_test.v”
set_global_assignment -name VERILOG_FILE “pll_sii_pll_swap_test_hcii.v”
```

Rename PLL Module

The top-level RTL design does not need modification, as the module name of the PLL is unchanged. However, by default, the module name matches the file name for the MegaWizard Plug-In Manager, so you must override the name to have two source files describing the same named module. When the PLL settings are modified to generate a 200-MHz clock instead of a 100-MHz clock using the MegaWizard Plug-In Manager, it saves the source file and module name with the same name as the new source file. After modification, the PLL module is named `pll_sii_pll_swap_test_hcii` and the Verilog HDL source file for the PLL generated by the MegaWizard Plug-In Manager is saved as **pll_sii_pll_swap_test_hcii.v**. After the file is saved, open the file in a text editor and change the module name back to `pll_sii` in the design file.

During the next compilation, the Quartus II software reads the design file **pll_sii_pll_swap_test_hcii.v** instead of **pll_sii.v** and compiles the design with the new design file.

Compare Revisions

After the compilation is complete, run **Compare HardCopy II Companion Revisions** to verify that changes in the PLL source file and settings are reflected in the revision comparison. The report shows these revision comparison differences as critical warnings. These differences must be reviewed by the HardCopy Design Center before the design is accepted for back-end migration.

For example, in the design example where you modified the PLL output clock generated from 100 MHz in the Stratix II FPGA to 200 MHz in the HardCopy II structured ASIC, you get critical warnings, as shown in Example 2, in the HardCopy II Companion Revision Comparison utility.

Example 2. Critical Warnings in the HardCopy II Companion Comparison

```
Critical Warning: Object “Nominal VCO frequency” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “599.9 MHz” versus “699.8 MHz”

Critical Warning: Object “Freq min lock” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “46.48 MHz” versus “48.72 MHz”

Critical Warning: Object “Freq max lock” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “86.9 MHz” versus “74.48 MHz”

Critical Warning: Object “M value” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “12” versus “14”

Critical Warning: Object “Charge pump current” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “77 uA” versus “96 uA”

Critical Warning: Atom “pll_sii:pll_inst|altpll:altpll_component|pll” has data
properties that differ between revisions

Critical Warning: Object “Nominal VCO frequency” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “699.8 MHz” versus “599.9 MHz”

Critical Warning: Object “Freq min lock” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “48.72 MHz” versus “46.48 MHz”

Critical Warning: Object “Freq max lock” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “74.48 MHz” versus “86.9 MHz”

Critical Warning: Object “M value” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “14” versus “12”

Critical Warning: Object “Charge pump current” has property field
“pll_sii:pll_inst|altpll:altpll_component|pll” as value “96 uA” versus “77 uA”

Critical Warning: Atom “pll_sii:pll_inst|altpll:altpll_component|pll” has data
properties that differ between revisions
```

These critical warnings must be reviewed by the HardCopy Design Center; if accepted, they must be waived before the design is accepted for back-end migration to a HardCopy II structured ASIC.

Conclusion

To design a HardCopy II device with different PLL settings from a Stratix II FPGA device, you must use the **.qsf** assignment:

```
set_global_assignment -name MIGRATION_DIFFERENT_SOURCE_FILE <filename>
```

With this setting, the HardCopy II Companion Revision Comparison utility tracks all changes made to your PLL settings. This setting also prevents the utility from issuing critical revision comparison failures. All critical revision comparison warnings must be reviewed by the HardCopy Design Center before the design is accepted for migration to a HardCopy II structured ASIC.

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date and Document Version	Changes Made
March 2010, v1.2	■ Updated "Migration Process With Different PLL Settings" ■ Minor text edits
December 2007, v1.1	■ Updated the "Migration Process With Different PLL Settings" section on page 1 ■ Updated Figure 1 ■ Updated and added subheadings to "Example Design Flow" section on page 5 ■ Replaced all occurrences of set_global_assignment -name with set_global_assignment -name
November 2006, v1.0	Initial release.

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