AN 554: How to Read HardCopy PrimeTime Timing Reports

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The Altera HardCopy Design Center generates timing reports in Synopsys PrimeTime format. This application note describes the different timing report files and explains how to interpret them.

Introduction

For the static timing analysis (STA) timing sign-off of a project, an Altera® HardCopy® Design Center (HCDC) engineer generates 15 corner critical path STA reports of the core and I/O path with setup and hold time analysis. Each corner contains four timing reports that include setup and hold time analysis for the core and I/O timing paths. Therefore, a total of 60 timing reports are delivered to the designer for review and approval.

The following example shows a timing report structure of a PrimeTime report for a typical industrial design. The temperature ranges from –40° to 100° C.

1. `ff_25d_v095_tn40/`
   a. `cbest/` (fast corner, 0.95 V, –40° C with parasitic extraction from thin and narrow metal lines, thick dielectric layers)
   b. `cworst/` (fast corner, 0.95 V, –40° C with parasitic extraction from thick and wider metal lines, thin dielectric layers)
   c. `rcbest/` (fast corner, 0.95 V, –40° C with parasitic extraction from thick and wider metal lines, thick dielectric layers)
   d. `rcworst/` (fast corner, 0.95 V, –40° C with parasitic extraction from thin and narrower metal lines, thin dielectric layers)
   e. `typical/` (fast corner, 0.95 V, –40° C with parasitic extraction from expected typical metal lines)
2. `ss_15d_v080_tn40/`
   a. `cbest/` (slow corner, 0.8 V, –40° C with parasitic extraction from thin and narrower metal lines, thick dielectric layers)
   b. `cworst/` (slow corner, 0.8 V, –40° C with parasitic extraction from thick and wider metal lines, thin dielectric layers)
   c. `rcbest/` (slow corner, 0.8 V, –40° C with parasitic extraction from thick and wider metal lines, thick dielectric layers)
   d. `rcworst/` (slow corner, 0.8 V, –40° C with parasitic extraction from thin and narrower metal lines, thin dielectric layers)
   e. `typical/` (slow corner, 0.8 V, –40° C with parasitic extraction from expected typical metal lines)

3. `ss_15d_v080_tp100/`
   a. `cbest/` (slow corner, 0.8 V, 100° C with parasitic extraction from thin and narrower metal lines, thick dielectric layers)
   b. `cworst/` (slow corner, 0.8 V, 100° C with parasitic extraction from thick and wider metal lines, thin dielectric layers)
   c. `rcbest/` (slow corner, 0.8 V, 100° C with parasitic extraction from thick and wider metal lines, thick dielectric layers)
   d. `rcworst/` (slow corner, 0.8 V, 100° C with parasitic extraction from thin and narrower metal lines, thin dielectric layers)
   e. `typical/` (slow corner, 0.8 V, 100° C with parasitic extraction from expected typical metal lines)

The two essential types of timing paths in all of the timing reports are the I/O-register timing and register-to-register timing paths. For I/O-register timing, the timing slack depends on the timing budget from the system board. It is constrained by either input delay or output delay specified by the designer, which may be adjustable by the designer based on actual system timing. All I/Os must be constrained. For register-to-register timing, the timing slack is constrained solely by the clock's edge-to-edge relation.

In this application note, Altera assumes you have a basic understanding of Synopsys PrimeTime timing reports. This application note describes HardCopy ASIC-specific pin and instance names and how timing is reported using various examples.

For more information about PrimeTime timing reports, refer to the *PrimeTime SI User Guide*.

Core Timing Paths

Core timing paths are those timing paths that are not directly going through a chip primary port. They are the timing paths from a sequential cell to another sequential cell. In HardCopy ASICs, the three main types of sequential cells are registers (`D` flipflops), memories, and digital signal processors (DSPs).

Register-to-Register

You can identify the setup timing path by `Path Type: max` and the hold timing path by `Path Type: min` in a PrimeTime report. Example 1 is a setup timing example.

Example 1. Setup Timing Example *(Note 1)*

```
Startpoint: modem/qr_tmp
              (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[2])
 Endpoint: modem/qr
              (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[2])
 Path Group: Sysclk|altpll|clk[2]
 Path Type: max

 Point                                                   Incr       Path
 ------------------------------------------------------------------------------
 clock Sysclk|altpll|clk[2] (rise edge)                 0.000      0.000
 clock network delay (propagated)                       0.204      0.204
 modem/qr_tmp/CLK (DFF_D1_CLK1_NCLR1_CKEN1_RSCN1_SCIN1) 0.000      0.204 r
 modem/qr_tmp/Q (DFF_D1_CLK1_NCLR1_CKEN1_RSCN1_SCIN1)   0.146 &    0.350 f
 modem/qr_tmp_ASTfhInst7779/OUT (BUF_D3)                0.073 &    0.423 f
 lcell_comb6052/OUT (BUF_D6)                            0.166 &    0.589 f
 modem/qr/D (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)             0.026 &    0.614 f
 data arrival time                                                 0.614

 clock Sysclk|altpll|clk[2] (rise edge)                 6.510      6.510
 clock network delay (propagated)                       0.321      6.831
 clock reconvergence pessimism                          0.003      6.835
 inter-clock uncertainty                               -0.160      6.675
 modem/qr/CLK (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)                      6.675 r
 library setup time                                    -0.340      6.334
 data required time                                                6.334
 ------------------------------------------------------------------------------
 data required time                                                6.334
 data arrival time                                                -0.614
 ------------------------------------------------------------------------------
 slack (MET)                                                       5.720
```

Note to Example 1:

(1) This is a typical register-to-register timing path for setup check.

Example 1 shows a timing path starting from the clock `CLK` pin of flipflop `modem/qr_tmp`, going through its `Q` pin, two buffer cells, and ending at the data input `D` pin of another flipflop, `modem/qr`.

In HardCopy ASICs, you can identify a flipflop by its cell type `DFF_*`, and pins `CLK`, `Q`, and `D`. You can identify a buffer instance by its cell type `BUF_D*`. If the name of a buffer instance contains the `AST` string—for example, `modem/qr_tmp_ASTfhInst7779`—it is typically a buffer inserted by the Synopsys Astro tool. If the name of a buffer instance has a pattern `lcell_comb*`—for example, `lcell_comb6052`—it is a buffer inserted by the Quartus® II software.

The HCDC uses a Synopsys IC Compiler during the backend implementation; therefore, the name of the instance contains the `icc_Place` string—for example, `icc_Place_6937/OUT (BUF_D6)` is a buffer inserted by the Synopsys IC Compiler.

The typical symbols shown in a PrimeTime report are defined as follows:

- "`&`" after an incremental delay number shows that the delay number is calculated with Resistor-Capacitor (RC) network back-annotation.
- "`*`" for Standard Delay Format (SDF) back-annotation
- "`+`" for lumped RC
- "`H`" for hybrid annotation

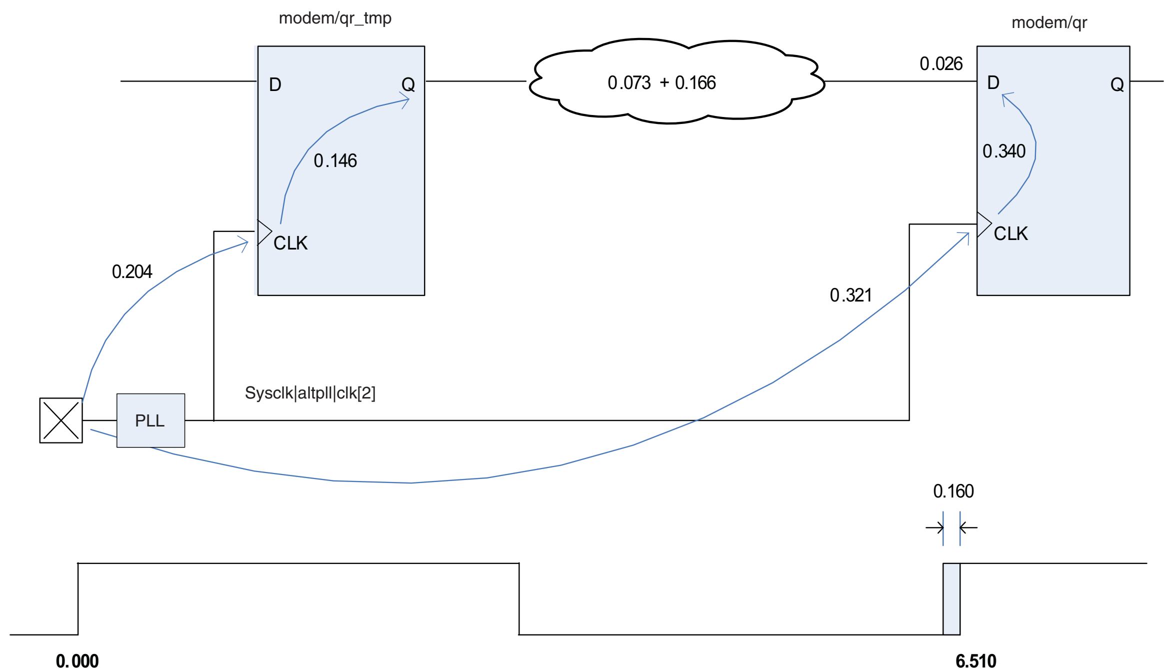
- “r” in the path column for the rising edge of the signal
- “f” in the path column for the falling edge of the signal

Most timing reports use ns for the time unit. However, you can use the PrimeTime command report_units to report all the units, such as capacitance, resistance, time, and voltage units used by the design.

Clock network delay is the delay from the clock port to the register clock pin. For phase-locked loop (PLL) clocks in normal compensation mode, the propagation delay is fully compensated and the clock network delay is expected to be 0.000 without skew. Skew is caused by the difference in the clock path delay of registers driven by the same PLL.

Figure 1 shows the register-to-register timing diagram of the timing path shown in Example 1.

Figure 1. Register-to-Register Timing Diagram for Example 1



To show how the clock network delays 0.204 and 0.321 are calculated by PrimeTime, the `report_timing -path full_clock_expanded` option is used to expand the timing path shown in Figure 1, resulting in the timing path shown in Example 2 and Example 3.

Example 2. Clock Network Delay 0.204 and 0.321 Calculations in the Timing Path for Figure 1 (part 1)

```
Startpoint: modem/qr_tmp
              (rising edge-triggered flip-flop Sysclk|altpll|clk[2])
 Endpoint: modem/qr
              (rising edge-triggered flip-flop Sysclk|altpll|clk[2])
 Path Group: Sysclk|altpll|clk[2]
 Path Type: max

 Point                                                   Incr       Path
 ---------------------------------------------------------------------------
 clock Sysclk|altpll|clk[2] (rise edge)                 0.000      0.000
 clock CLKIN (source latency)                           0.000      0.000
 clkin (in)                                             0.000 &    0.000 r
 pin_clkin/PIN (C680213_0000000000000402982000000108_V33_LVTTL)
                                                        0.077 H    0.077 r
 pin_clkin/PINin (C680213_0000000000000402982000000108_V33_LVTTL)
                                                        0.000      0.077 r
 pin_clkin/DATOVR (C680213_0000000000000402982000000108_V33_LVTTL)
                                                        0.782 H    0.859 r
 XBLIOBF_XP17B_XCLKBUF/CLKPIN0 (C65247)                 0.123 &    0.982 r
 XBCLKBUF_X3/OUT (C3802)                                0.099 &    1.080 r
 XBGPLL_XPLL_XINCBUF/OUT0 (C78620)                      0.100 &    1.180 r
 XBGPLL_XPLL_XCLKMUX_XIPBUF/CLKPIN_PLLB0 (C3735)        0.076 &    1.256 r
 pll_pll/RCLKPIN0checkpin1 (C75214_Z2)                  0.000 *    1.256 r
 pll_pll/CCLK2 (C75214_Z2) (gclock source)             -3.189 *   -1.933 r
 clkbuf_a_clk2_clkctrl/OUT (C3741_28)                   0.280 H   -1.653 r
 XM0011A_GCLK_6_CB/OUT (CLKBUFD11W)                     0.180 &   -1.473 r
 XM0011A_GCLK_6_CBB/OUT (CLKBUFD11C_TEST)               0.265 &   -1.208 r
 XM0011A_GCLK_6_CBOL_Q4/OUT (CLKBUFD9WL)                0.169 &   -1.039 r
 XM0011A_SCLK_10_LHS_Q4/OUT (CLKBUFD11WL)               0.187 &   -0.852 r
 XM0011A_RCLK_10_R34_Q4/OUT (CLKBUFD15L)                0.200 &   -0.652 r
 XM0011A_RCLK_10_S2R4_Q4/OUT (CLKBUFD13L)               0.177 &   -0.474 r
 XM0011A_LIOBB2CLK_S10/OUT (CLKBUFD9L)                  0.124 &   -0.350 r
 XLBIOCLK/LIOBB2EXT0CLK_S10 (C99314)                    0.168 &   -0.183 r
 XLIOBB2EXT0CLKA_S10/OUT (CLKBUFD9R_CTS)                0.257 &    0.074 r
 SB_LIOBB2EXT0CLKASD6_SCLK10/OUT (CLKBUFD11RB_CTS)      0.126 &    0.200 r
 modem/qr_tmp/CLK (DFF_D1_CLK1_NCLR1_CKEN1_RSCN1_SCIN1) 0.004 &    0.204 r
 modem/qr_tmp/Q (DFF_D1_CLK1_NCLR1_CKEN1_RSCN1_SCIN1)   0.146 &    0.350 f
 modem/qr_temp_ASTfhInst7779/OUT (BUF_D3)               0.073 &    0.423 f
 lcell_comb6052/OUT (BUF_D6) <-                         0.166 &    0.589 f
 modem/qr/D (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)             0.026 &    0.614 f
 data arrival time                                                 0.614
```

Example 3. Clock Network Delay 0.204 and 0.321 Calculations in the Timing Path for Figure 1 (part 2)

```
clock Sysclk|altpll|clk[2] (rise edge)                          6.510      6.510
clock CLKIN (source latency)                                    0.000      6.510
clkin (in)                                                      0.000 &    6.510 r
pin_clkin/PIN (C680213_0000000000000402982000000108_V33_LVTTL)
                                                                0.077 H    6.587 r
pin_clkin/PINin (C680213_0000000000000402982000000108_V33_LVTTL)
                                                                0.000      6.587 r
pin_clkin/DATOVR (C680213_0000000000000402982000000108_V33_LVTTL)
                                                                0.782 H    7.369 r
XBLIOBF_XP17B_XCLKBUF/CLKPIN0 (C65247)                          0.063 &    7.432 r
XBCLKBUF_X3/OUT (C3802)                                         0.096 &    7.528 r
XBGPLL_XPLL_XINCBUF/OUT0 (C78620)                               0.099 &    7.627 r
XBGPLL_XPLL_XCLKMUX_XIPBUF/CLKPIN_PLLB0 (C3735)                 0.075 &    7.703 r
pll_pll/RCLKPIN0checkpin1 (C75214_Z2)                           0.000 *    7.703 r
pll_pll/CCLK2 (C75214_Z2) (gclock source)                      -3.189 *    4.514 r
clkbuf_a_clk2_clkctrl/OUT (C3741_28)                            0.280 H    4.794 r
XM0011A_GCLK_6_CB/OUT (CLKBUFD11W)                              0.178 &    4.972 r
XM0011A_GCLK_6_CBB/OUT (CLKBUFD11C_TEST)                        0.265 &    5.237 r
XM0011A_GCLK_6_CBOL_Q4/OUT (CLKBUFD9WL)                         0.169 &    5.406 r
XM0011A_SCLK_10_LHS_Q4/OUT (CLKBUFD11WL)                        0.187 &    5.593 r
XM0011A_RCLK_10_R34_Q4/OUT (CLKBUFD15L)                         0.200 &    5.793 r
XM0011A_RCLK_10_S4R4_Q4/OUT (CLKBUFD13L)                        0.180 &    5.973 r
XM0011A_DCLK_10_D4S4R4_Q4/OUT (CLKBUFD7L)                       0.095 &    6.068 r
SB_Q4R4SR4D4SD14_SCLK10_backend_947/OUT (DEL_2)                 0.332 &    6.400 r
SB_Q4R4SR4D4SD14_SCLK10/OUT (CLKBUFD15_DLY9)                    0.423 &    6.823 r
modem/qr/CLK (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)                    0.009 &    6.831 r
clock reconvergence pessimism                                   0.003      6.835
inter-clock uncertainty                                        -0.160      6.675
library setup time                                             -0.340      6.334
data required time                                                         6.334
------------------------------------------------------------------------------
data required time                                                         6.334
data arrival time                                                         -0.614
------------------------------------------------------------------------------
slack (MET)                                                                5.720
```

As shown in Example 2 and Example 3, the source clock CLKIN comes into the chip from the `clkin` port with latency 0.000. CLKIN goes through the clock I/O instance `pin_clkin` and four clock control/mux blocks, with a propagation delay of 1.256. It then goes into the PLL through the `pll_pll/RCLKPIN0checkpin1` pin and gets out of the PLL through the `pll_pll/CCLK2` pin. A negative delay of –3.189 is annotated as PLL compensation. This number is calculated by the Quartus II software and obtained from the constraint Tcl script (**.tcl**) file. After the PLL, the clock propagates through a series of clock control muxes or clock buffers, before arriving at the flipflop's clock pin `modem/qr_tmp/CLK` with a delay of 0.204. This number is the clock network delay for the launching clock.

For the capture clock, the clock path shares the same path as the launching clock until the clock buffer `XM0011A_RCLK_10_R34_Q4`. From there, the capture clock goes to different clock branches. The clock eventually arrives at the capture register clock `modem/qr/CLK` pin with a clock network delay of 6.831 – 6.510 = 0.321.

The hold timing for the Example 1 timing path is shown in Example 4.

Example 4. Hold Timing Path for Example 1

```
Startpoint: modem/qr_tmp
               (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[2])
  Endpoint: modem/qr
               (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[2])
  Path Group: Sysclk|altpll|clk[2]
  Path Type: min

  Point                                                    Incr       Path
  ------------------------------------------------------------------------------
  clock Sysclk|altpll|clk[2] (rise edge)                   0.000      0.000
  clock network delay (propagated)                         0.103      0.103
  modem/qr_tmp/CLK (DFF_D1_CLK1_NCLR1_CKEN1_RSCN1_SCIN1)   0.000      0.103 r
  modem/qr_tmp/Q (DFF_D1_CLK1_NCLR1_CKEN1_RSCN1_SCIN1)     0.164 &    0.267 r
  modem/qr_tmp_ASTfhInst7779/OUT (BUF_D3)                  0.071 &    0.338 r
  lcell_comb6052/OUT (BUF_D6)                              0.154 &    0.493 r
  modem/qr/D (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)              -0.012 &    0.481 r
  data arrival time                                                   0.481

  clock Sysclk|altpll|clk[2] (rise edge)                   0.000      0.000
  clock network delay (propagated)                         0.387      0.387
  clock reconvergence pessimism                           -0.065      0.322
  inter-clock uncertainty                                  0.050      0.372
  modem/qr/CLK (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)                        0.372 r
  library hold time                                       -0.054      0.318
  data required time                                                  0.318
  ------------------------------------------------------------------------------
  data required time                                                  0.318
  data arrival time                                                  -0.481
  ------------------------------------------------------------------------------
  slack (MET)                                                         0.163
```

Register-to-Memory Timing Path

Example 5 shows the timing path for register-to-memory.

Example 5. Register-to-Memory Timing Path *(Note 1)*

```
Startpoint: ileavedata[4]
               (rising edge-triggered flip-flop clocked by Sysclk|altpll]|pll|clk[2])
  Endpoint: ram2 (rising edge-triggered flip-flop clocked by Sysclk|altpll]|pll|clk[3])
  Path Group: Sysclk|altpll]|pll|clk[3]
  Path Type: max

  Point                                                            Incr       Path
  ----------------------------------------------------------------------------------
  clock Sysclk|altpll]|pll|clk[2] (rise edge)                     0.000      0.000
  clock network delay (propagated)                                0.034      0.034
  ileavedata[4]/CLK (DFF_D1_CLK1_NCLR1_SLD0_ASDATA1_RSCN1_SCIN1)  0.000      0.034 r
  ileavedata[4]/Q (DFF_D1_CLK1_NCLR1_SLD0_ASDATA1_RSCN1_SCIN1)    0.130 &    0.164 f
  ileavedata_4_ASTfhInst9282/OUT (DEL_2)                          0.294 &    0.458 f
  lcell_comb98891/OUT (BUF_D6)                                    0.214 &    0.673 f
  lcell_comb77596/OUT (BUF_D6)                                    0.390 &    1.063 f
  lcell_comb46900/OUT (BUF_D6)                                    0.317 &    1.380 f
  ram2/DINA17 (C92501_Z11)                                        0.139 &    1.519 f
  data arrival time                                                          1.519

  clock Sysclk|altpll]|pll|clk[3] (rise edge)                      3.255      3.255
  clock network delay (propagated)                                -0.370      2.885
  clock reconvergence pessimism                                    0.001      2.887
  inter-clock uncertainty                                         -0.160      2.727
  ram2/E_CLKA (C92501_Z11)                                                    2.727 r
  library setup time                                               0.054       2.781
  data required time                                                          2.781
  ----------------------------------------------------------------------------------
  data required time                                                          2.781
  data arrival time                                                          -1.519
  ----------------------------------------------------------------------------------
slack (MET)                                                                   1.263
```

Note to Example 5:

(1) This is a typical register-to-memory timing path.

Example 5 shows a timing path starting from the clock pin `CLK` of flipflop `ileavedata[4]`, going through its `Q` pin, a delay cell, three buffers, and ending at data input pin `DINA17` of memory instance `ram2`. The capture clock pin of `ram2` is `E_CLKA`.

You can identify the launching flipflop by the cell type `DFF_*` and the `CLK` and `Q` pins.

Memory-to-Register Timing Path

Example 6 shows the timing path for memory-to-register.

Example 6. Memory-to-Register Timing Path *(Note 1)*

```
Startpoint: ram129 (rising edge-triggered flip-flop clocked by iqclk)
  Endpoint: datouthdly[3]
               (rising edge-triggered flip-flop clocked by iqclk)
  Path Group: iqclk
  Path Type: max

  Point                                                       Incr       Path
  ------------------------------------------------------------------------------
  clock iqclk (rise edge)                                     0.000      0.000
  clock network delay (propagated)                            1.783      1.783
  ram129/E_CLKB (C92501_Z11)                                  0.000      1.783 r
  ram129/EABOUT_05 (C92501_Z11)                               2.657 &    4.440 f
  datouthdly[3]/D (DFF_D1_CLK1_NCLR1_SLD0_ASDATA1_RSCN1_SCIN1)  0.052 &    4.492 f
  data arrival time                                                      4.492

  clock iqclk (rise edge)                                    13.020     13.020
  clock network delay (propagated)                            1.742     14.762
  clock reconvergence pessimism                               0.010     14.773
  inter-clock uncertainty                                    -0.150     14.623
  datouthdly[3]/CLK (DFF_D1_CLK1_NCLR1_SLD0_ASDATA1_RSCN1_SCIN1)        14.623 r
  library setup time                                         -0.448     14.175
  data required time                                                    14.175
  ------------------------------------------------------------------------------
  data required time                                                    14.175
  data arrival time                                                     -4.492
  ------------------------------------------------------------------------------
  slack (MET)                                                            9.683
```

Note to Example 6:

(1) This is a typical memory-to-register timing path.

Example 6 shows a timing path starting from clock pin `E_CLKB` of memory instance `ram129`, going through its output pin `EABOUT_05`, and ending at the data input pin `D` of flipflop instance `datouthdly[3]`. The capture clock pin of `datouthdly[3]` is `CLK`.

You can identify the launching memory by the name `ram*` and by its cell type `C9250*`.

Register-to-DSP Timing Path

Example 7 shows the timing path for register-to-DSP.

Example 7. Register-to-DSP Timing Path

```
Startpoint: modem/multb[12]
              (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[1])
 Endpoint: mac_mult180647
              (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[1])
 Path Group: Sysclk|altpll|clk[1]
 Path Type: max

 Point                                                    Incr       Path
 ------------------------------------------------------------------------------
 clock Sysclk|altpll|clk[1] (rise edge)                  0.000      0.000
 clock network delay (propagated)                        0.095      0.095
 modem/multb/CLK (DFF_D1_CLK1_NCLR1_SCLR1_RSCN1_SCIN1)   0.000      0.095 r
 modem/multb/Q (DFF_D1_CLK1_NCLR1_SCLR1_RSCN1_SCIN1)     0.188 &    0.283 r
 lcell_comb106022/OUT (CHLE_2_1_6_D2_0)                  0.198 &    0.481 r
 lcell_comb104239/S (ADDER_A1_B1_CI1)                    0.221 &    0.702 f
 lcell_comb103452/OUT (BUF_D6)                           0.218 &    0.920 f
 lcell_comb77776/OUT (BUF_D6)                            0.302 &    1.222 f
 mac_mult180647/INBX0 (C955081_Z1)                       0.052 &    1.274 f
 data arrival time                                                  1.274

 clock Sysclk|altpll|clk[1] (rise edge)                 13.021     13.021
 clock network delay (propagated)                       -0.409     12.612
 clock reconvergence pessimism                           0.003     12.615
 inter-clock uncertainty                                -0.160     12.455
 mac_mult180647/CLK_A (C955081_Z1)                                 12.455 r
 library setup time                                      0.243     12.699
 data required time                                                12.699
 ------------------------------------------------------------------------------
 data required time                                                12.699
 data arrival time                                                 -1.274
 ------------------------------------------------------------------------------
 slack (MET)                                                       11.425
```

Note to Example 7:

(1) This is a typical register-to-DSP timing path.

Example 7 shows a timing path starting from the clock pin CLK of flipflop modem/multb going through its Q pin, two combinational logic cells (type CHLE_* and type ADDER_*), two buffers, and ending at data input pin INBX0 of DSP instance mac_mult180647 (type C9550*). The capture clock pin of mac_mult180647 is CLK_A.

You can identify the launching flipflop by the cell type DFF_* and the CLK and Q pins.

DSP-to-Register Timing Path

Example 8 shows the timing path for DSP-to-register.

Example 8. DSP-to-Register Timing Path *(Note 1)*

```
Startpoint: mac_mult180647
              (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[1])
 Endpoint: modem/out12[6]
              (rising edge-triggered flip-flop clocked by Sysclk|altpll|clk[1])
 Path Group: Sysclk|altpll|clk[1]
 Path Type: max

 Point                                                   Incr       Path
 -----------------------------------------------------------------------------
 clock Sysclk|altpll|clk[1] (rise edge)                 0.000      0.000
 clock network delay (propagated)                      -0.342     -0.342
 mac_mult180647/CLK_A (C955081_Z1)                      0.000     -0.342 r
 mac_mult180647/MAC_OUTB34 (C955081_Z1)                 1.502 &    1.160 f
 mac_mult180647ASThfnInst2461/OUT (BUF_D4)              0.245 &    1.405 f
 lcell_comb43492/OUT (CHLE_4_2_AACA_D2_0)               0.201 &    1.606 f
 lcell_comb43633/OUT (BUF_D6)                           0.132 &    1.738 f
 lcell_comb50384/S (ADDER_A1_B0_CI1)                    0.209 &    1.947 f
 lcell_comb50385/OUT (CHLE_6_3_EAEAEAC8EAEAEAEA_D2_0)   0.171 &    2.118 f
 lcell_comb51196/OUT (BUF_D6)                           0.137 &    2.255 f
 modem/out12/D (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)          0.006 &    2.261 f
 data arrival time                                                 2.261

 clock Sysclk|altpll|clk[1] (rise edge)                13.021     13.021
 clock network delay (propagated)                       0.143     13.164
 clock reconvergence pessimism                          0.003     13.167
 inter-clock uncertainty                               -0.160     13.007
 modem/out12/CLK (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)                  13.007 r
 library setup time                                    -0.324     12.682
 data required time                                               12.682
 -----------------------------------------------------------------------------
 data required time                                               12.682
 data arrival time                                                -2.261
 -----------------------------------------------------------------------------
 slack (MET)                                                      10.421
```

Note to Example 8:

(1) This is a typical DSP-to-register timing path.

Example 8 shows a timing path starting from clock pin `CLK_A` of DSP block `mac_mult180647`, going through its out pin `MAC_OUTB34`, six combinational logic cells and buffers, and ending at the data input pin `D` of flipflop instance `modem/out12`. The capture clock pin of `modem/out12` is `CLK`.

You can identify the launching DSP by the name `mac_mult*` and by its cell type `C9550*`.

I/O Timing Path

I/O timing paths are those timing paths going through any chip primary input port or primary output port. For illustration purposes, this application note divides I/O timing paths into two categories: typical I/O and LVDS.

Typical I/O

The following sections describe input and output I/O timing.

Input I/O Timing Path

Example 9 shows the input I/O timing path to an I/O register.

Example 9. Typical I/O Timing Path to an I/O Register *(Note 1)*

```
Startpoint: exrw (input port clocked by EXCLK)
Endpoint: pin_exrw (rising edge-triggered flip-flop clocked by
PLL_33M:pll_ex|altpll:altpll_component|_clk0)
Path Group: PLL_33M:pll_ex|altpll:altpll_component|_clk0
Path Type: max

Point                                                      Trans      Incr       Path
-----------------------------------------------------------------------------------------
clock EXCLK (rise edge)                                              0.000      0.000
clock network delay (propagated)                                     0.000      0.000
input external delay                                                15.000     15.000 f
exrw (in)                                                  2.640      0.000 &   15.000 f
pin_exrw/PIN (C67002_0000000F90C1040298200000108_V33_LVTTL)   2.640  0.027 H   15.027 f
pin_exrw/PINin (C67002_0000000F90C1040298200000108_V33_LVTTL) 2.640    0.000    15.027 f
pin_exrw/DATOVR (C67002_0000000F90C1040298200000108_V33_LVTTL) 0.255    0.772 H   15.799 f
data arrival time                                                              15.799

clock PLL_33M:pll_ex|altpll:altpll_component|_clk0 (rise edge)      30.303     30.303
clock network delay (propagated)                                     0.331     30.634
clock reconvergence pessimism                                        0.000     30.634
inter-clock uncertainty                                             -0.260     30.374
pin_exrw/CLKIN (C67002_0000000F90C1040298200000108_V33_LVTTL)                   30.374 r
library setup time                                                  -3.978     26.396
data required time                                                             26.396
-----------------------------------------------------------------------------------------
data required time                                                             26.396
data arrival time                                                             -15.799
-----------------------------------------------------------------------------------------
slack (MET)                                                                    10.597
```

Note to Example 9:

(1) This is a typical I/O timing path to an I/O register.

In Example 9, the input I/O port name given by the designer is `exrw`; the capture I/O register name in the HardCopy ASIC is `pin_exrw`; the register `D` pin name is `DATOVR`; and the register `CLK` pin name is `CLKIN`.

The HardCopy ASIC cell type `C67002_0000000F90C1040298200000108_V33_LVTTL` designates that it is a 3.3-V LVTTL type of I/O. The master I/O type given by Altera is `C67002`, while `0000000F90C1040298200000108` is the specific configuration bit settings for `C67002` in this application.

PrimeTime takes 15.000 ns as input external delay in Example 9 for its timing calculation. The number comes from the constraint SDC file, in which the designer specifies a 15.000 ns input delay:

```
set_input_delay -add_delay -max -clock [get_clocks {EXCLK}]
15.000 [get_ports exrw]
```

Example 10 shows the input I/O timing path to a core register.

Example 10. Input I/O Timing Path to a Core Register

```
Startpoint: dischg (input port clocked by in_lvds_mode)
 Endpoint: top/dischg_q
              (rising edge-triggered flip-flop clocked by pll_tx_mode)
 Path Group: pll_tx_mode
 Path Type: max

 Point                                           Trans       Incr        Path
 -----------------------------------------------------------------------------
 clock in_lvds_mode (rise edge)                              0.000       0.000
 clock network delay (propagated)                            0.000       0.000
 input external delay                                        6.259       6.259 f
 dischg (in)                                     2.640       0.000 &     6.259 f
 pin_dischg/PIN (C680073_000000000000402982000001 08_V33_LVTTL)
                                                 2.640       0.060 H     6.319 f
 pin_dischg/PINin (C680073_000000000000402982000001 08_V33_LVTTL)
                                                 2.640       0.000       6.319 f
 pin_dischg/DATOVR (C680073_000000000000402982000001 08_V33_LVTTL)
                                                 0.236       0.747 H     7.066 f
 pin_dischg/CDATA0IN (C680073_000000000000402982000001 08_V33_LVTTL)
                                                 0.084       0.345 &     7.411 f
 pin_dischgASTfhInst10846/OUT (BUF_D4)           0.036       0.086 &     7.497 f
 pin_dischgASTfhInst8085/OUT (DEL_1)             0.030       0.127 &     7.624 f
 lcell_comb8533/OUT (CHLE_2_1_8_D2_0)            0.063       0.108 &     7.732 f
 U109/OUT (DEL_4)                                0.041       0.538 &     8.270 f
 U115/OUT (DEL_4)                                0.033       0.529 &     8.799 f
 top/dischg_q/D (DFF_D1_CLK1_NCLR0_RSCN1_SCIN1)
                                                 0.033       0.000 &     8.799 f
 data arrival time                                                       8.799

 clock pll_tx_mode (rise edge)                               9.259       9.259
 clock network delay (propagated)                            1.158      10.417
 clock reconvergence pessimism                               0.000      10.417
 inter-clock uncertainty                                    -0.130      10.287
 top/dischg_q/CLK (DFF_D1_CLK1_NCLR0_RSCN1_SCIN1)
                                                                        10.287 r
 library setup time                                         -0.284      10.003
 data required time                                                     10.003
 -----------------------------------------------------------------------------
 data required time                                                     10.003
 data arrival time                                                      -8.799
 -----------------------------------------------------------------------------
 slack (MET)                                                             1.204
```

In Example 10, the input I/O port name is `dischg`. It is clocked by the `in_lvds_mode` clock.

Data travels out of I/O instance `pin_dischg` through the `CDATA0IN` pin, then travels through buffer `pin_dischgASTfhInst10846` and delay cell `pin_dischgASTfhInst8085`, then travels through a combinational logic cell `lcell_comb8533`, two more delay cells `U109` and `U115`, and ends at the `D` pin of the core register `top/dischg_q`.

The following cell types are used in HardCopy ASICs:

- DEL_*—a delay cell that is mainly used for hold time fixing
- BUF_*—a data buffer that is mainly used for buffering data delay to meet setup timing
- CHLE_*—an Altera proprietary logic element that is typically used to construct combinational logic
- DFF_*—shows the instance is a D flipflop

The engineering change order (ECO)-inserted buffer or delay cells typically have a name pattern of U[0-9999]; for example, U109 and U115.

Output I/O Timing

Example 11 shows the output I/O timing path from an I/O register.

Example 11. Output Timing Path from an I/O Register

```
Startpoint: pin_pn_cnt1
             (rising edge-triggered flip-flop clocked by pll_tx_mode)
Endpoint: pn_cnt1_b (output port clocked by in_lvds_mode)
Path Group: in_lvds_mode
Path Type: max

Point                                               Trans      Incr       Path
-----------------------------------------------------------------------------
clock pll_tx_mode (rise edge)                                  0.000      0.000
clock network delay (propagated)                               0.929      0.929
pin_pn_cnt1/CLKOUT (C680043_000000000000C40298000060420_V33_LVCMOS)
                                                    0.076      0.000      0.929 r
pin_pn_cnt1/DIN (C680043_000000000000C40298000060420_V33_LVCMOS)
                                                    0.138      0.966 &    1.894 f
pin_pn_cnt1/PIN (C680043_000000000000C40298000060420_V33_LVCMOS)
                                                    0.824      1.705 &    3.599 f
pn_cnt1 (out)                                       0.824      0.000 &    3.599 f
data arrival time                                                         3.599

clock in_lvds_mode (rise edge)                                12.642     12.642
clock network delay (propagated)                               0.000     12.642
clock reconvergence pessimism                                  0.000     12.642
inter-clock uncertainty                                       -0.240     12.402
output external delay                                         -8.090      4.312
data required time                                                        4.312
-----------------------------------------------------------------------------
data required time                                                        4.312
data arrival time                                                        -3.599
-----------------------------------------------------------------------------
slack (MET)                                                               0.713
```

In Example 11, the launching I/O register name is pin_pn_cnt1; the register CLK pin name is CLKOUT; and the output I/O port name given by the designer is pn_cnt1.

The output external delay –8.090 comes from the designer constraint:

```
set_output_delay -add_delay -max -clock [get_clocks
{in_lvds_mode}] 8.090 [ get_ports pn_cnt1 ]
```

Example 12 shows the output I/O timing path from a core register.

Example 12. Output I/O Timing Path from a Core Register

```
Startpoint: rl_inv_rep_ff
              (rising edge-triggered flip-flop clocked by in_lvds_mode)
 Endpoint: pn_rl_invert
              (output port clocked by in_lvds_mode)
 Path Group: in_lvds_mode
 Path Type: max

 Point                                            Trans       Incr        Path
 -----------------------------------------------------------------------------
 clock in_lvds_mode (rise edge)                               0.000       0.000
 clock network delay (propagated)                             2.363       2.363
 rl_inv_rep_ff/CLK (DFF_D1_CLK1_NCLR0_CKEN1_RSCN1_SCIN1)
                                                  0.113       0.000       2.363 r
 rl_inv_rep_ff/Q (DFF_D1_CLK1_NCLR0_CKEN1_RSCN1_SCIN1)
                                                  0.051       0.152 &     2.515 r
 rl_inv_rep_ffASTttcInst4922/OUT (BUF_D6)
                                                  0.679       0.220 &     2.735 r
 rl_inv_rep_ffASThfnInst4547/OUT (BUF_D5)
                                                  0.491       0.247 &     2.982 r
 pin_pn_rl_invert/DIN (C680103_00000000000040298000060420_V33_LVCMOS)
                                                  0.142       0.645 H     3.627 f
 pin_pn_rl_invert/PIN (C680103_00000000000040298000060420_V33_LVCMOS)
                                                  0.876       1.731 H     5.358 f
 pn_rl_invert (out)                               0.876       0.000 &     5.358 f
 data arrival time                                                        5.358

 clock in_lvds_mode (rise edge)                              12.642      12.642
 clock network delay (propagated)                             0.000      12.642
 clock reconvergence pessimism                                0.000      12.642
 inter-clock uncertainty                                     -0.200      12.442
 output external delay                                       -5.137       7.305
 data required time                                                       7.305
 -----------------------------------------------------------------------------
 data required time                                                       7.305
 data arrival time                                                       -5.358
 -----------------------------------------------------------------------------
 slack (MET)                                                              1.947
```

In Example 12, the launching core register name is `rl_inv_rep_ff`. Data travels out of the core register at the `Q` pin, through two buffers, goes into I/O `pin_pn_rl_invert`, and finally arrives at the output I/O port `pn_rl_invert`.

The designer used the following constraint:

```
set_output_delay -add_delay -max -clock [get_clocks
{in_lvds_mode}] 5.137 [get_ports pn_rl_invert]
```

Bidir I/O Timing

For the bidir I/O port, there is both a data input timing path and a data output timing path. In addition to these two data paths, there is also an output-enable (OE) control path similar to Example 13.

Example 13. Bidir I/O Output-Enable Control Path

```
Startpoint: slave/sda_cl_z
            (rising edge-triggered flip-flop clocked by in_lvds_mode)
Endpoint: com_sda
            (output port clocked by in_lvds_mode)
Path Group: in_lvds_mode
Path Type: max

Point                                             Trans       Incr        Path
------------------------------------------------------------------------------
clock in_lvds_mode (rise edge)                                0.000       0.000
clock network delay (propagated)                              2.318       2.318
slave/sda_cl_z/CLK (DFF_D1_CLK1_NCLR0_RSCN1_SCIN1)
                                                  0.100       0.000       2.318 r
slave/sda_cl_z/Q (DFF_D1_CLK1_NCLR0_RSCN1_SCIN1)
                                                  0.044       0.117 &     2.435 f
slave/sda_cl_zASTfhInst10843/OUT (BUF_D6)
                                                  0.062       0.107 &     2.542 f
lcell_comb77126/OUT (CHLE_2_1_8_D2_0)             0.056       0.113 &     2.655 f
lcell_comb77348/OUT (BUF_D6)                      0.356       0.200 &     2.855 f
lcell_comb71550/OUT (BUF_D6)                      0.343       0.410 &     3.265 f
lcell_comb32130/OUT (BUF_D6)                      0.406       0.428 &     3.693 f
pin_com_sda/OE (C680053_000000010187C00298000000218_V33_LVTTL) <-
                                                  0.532       0.155 &     3.848 f
pin_com_sda/OEB (C680053_000000010187C00298000000218_V33_LVTTL) <-
                                                  0.127       0.501       4.349 r
pin_com_sda/PIN (C680053_000000010187C00298000000218_V33_LVTTL)
                                                  1.303       1.985 H     6.334 r
com_sda (inout)                                   1.303       0.000 &     6.334 r
data arrival time                                                         6.334

clock in_lvds_mode (rise edge)                               12.642      12.642
clock network delay (propagated)                              0.000      12.642
clock reconvergence pessimism                                 0.000      12.642
inter-clock uncertainty                                      -0.200      12.442
output external delay                                        -4.042       8.400
data required time                                                        8.400
------------------------------------------------------------------------------
data required time                                                        8.400
data arrival time                                                        -6.334
------------------------------------------------------------------------------
slack (MET)                                                               2.066
```

The Example 13 timing path is similar to Example 12 on page 15 (from a core register). The difference is that the path is through the output enable control pin (`pin_com_sda/OE`), not through the data pin (`pin_com_sda/DIN`).

LVDS

The following sections describe the LVDS input and output timing paths.

LVDS Input Timing Path

LVDS macros have built-in registers, which are typically used for serializer/deserializer (SERDES) receivers and transmitters. In this type of configuration, they are sequential cells. You can also configure LVDS macros to bypass the built-in registers and only use them as combinational logic cells.

Example 14 shows the LVDS input timing path.

Example 14. LVDS Input Timing Path

```
Startpoint: lvds_in[10]
              (input port)
 Endpoint: lvds_rx1180
              (rising edge-triggered flip-flop clocked by pll_rx_mode)
 Path Group: pll_rx_mode
 Path Type: max

 Point                                           Trans      Incr       Path
 ------------------------------------------------------------------------------
 clock (input port clock) (rise edge)                       0.000      0.000
 input external delay                                       0.000      0.000 r
 lvds_in[10] (in)                                0.280      0.000 &    0.000 r
 lvds_rx1180/LVDSIN (C69100_C03008002_V25_LVDS)  0.280      0.000 &    0.000 r
 data arrival time                                                     0.000

 clock pll_rx_mode (rise edge)                              0.903      0.903
 clock network delay (propagated)                           0.458      1.361
 clock reconvergence pessimism                              0.000      1.361
 lvds_rx1180/RXFCLK (C69100_C03008002_V25_LVDS)                        1.361 r
 library setup time                                        -0.611      0.750
 data required time                                                    0.750
 ------------------------------------------------------------------------------
 data required time                                                    0.750
 data arrival time                                                    -0.000
 ------------------------------------------------------------------------------
 slack (MET)                                                           0.750
```

In Example 14, the receiver LVDS instances have the name pattern `lvds_rx*`. The typical data input pin name of a receiver LVDS instance is `LVDSIN`. The typical clock pin name for a receiver LVDS instance is `RXFCLK`.

The input external delay `Incr 0.000` implies that the designer set the constraint so that the input data edge and clock edge are edge-aligned when arriving at the chip boundary. That is, the arriving data edge and the arriving clock edge are switching at the same time. The constraint must be consistent with the parameter settings in the HardCopy mapping report `INCLOCK_DATA_ALIGNMENT ; EDGE_ALIGNED`.

If the data edge and clock edge are center-aligned, the input external delay is typically a 90° offset; for example, 90/360*0.903 = 0.226 ns.

The actual delay from the input pin `lvds_in[10]` to the data input of the receiving register is lumped into the library setup time in the HardCopy ASIC timing model; for example, 0.611 ns.

When an input LVDS macro is configured to bypass the built-in register and only used as combinational logic, the output pin of the LVDS macro is `lvds_rx*/DATOVR`. Example 15 is a timing path starting from input port `i_data`, passing through the LVDS macro `lvds_rx183366`, and ending at an I/O register `pin_i_data`.

Example 15. LVDS Input Timing Path in Bypass Mode

```
Startpoint: i_data
               (input port clocked by i_Clk)
  Endpoint: pin_i_data
               (falling edge-triggered flip-flop clocked by i_Clk)
  Path Group: i_Clk
  Path Type: max

  Point                                                   Incr       Path
  ------------------------------------------------------------------------------
  clock i_Clk (rise edge)                                0.000      0.000
  clock network delay (propagated)                       0.000      0.000
  input external delay                                   0.268      0.268 f
  i_data (in)                                            0.000 &    0.268 f
  lvds_rx183366/LVDSIN (C69100_000000002_V25_LVDS)       0.000 &    0.268 f
  lvds_rx183366/DATOVR (C69100_000000002_V25_LVDS) <-    0.303 &    0.571 f
  pin_i_data/DATOVR (C66000_000000002040040298 20A000000_L_V25_LVDS)
                                                         0.015 &    0.586 f
  data arrival time                                                 0.586
  ------------------------------------------------------------------------------
```

LVDS Output Timing Path

Example 16 shows the LVDS output timing path.

Example 16. LVDS Output Timing Path

```
Startpoint: lvds_tx118093
             (rising edge-triggered flip-flop clocked by pll_tx_mode)
Endpoint: lvds_out[0]
             (output port)
Path Group: (none)
Path Type: max

Point                                              Trans      Incr       Path
------------------------------------------------------------------------------
clock network delay (propagated)                             0.657      0.657
lvds_tx118093/TXFCLK (C69000_000026450000)        0.026      0.000      0.657 r
lvds_tx118093/LVDSOUT (C69000_000026450000)       0.667      1.917 &    2.574 r
lvds_out[0] (inout)                               0.666      0.000 &    2.574 r
data arrival time                                                       2.574
------------------------------------------------------------------------------
```

Example 16 shows that the transmitter LVDS instances have the name pattern `lvds_tx*`. The typical output pin name of a transmitting LVDS instance is `LVDSOUT`. The typical clock pin name for a transmitting LVDS instance is `TXFCLK`.

The timing path starts at clock pin `lvds_tx118093/TXFCLK`, demonstrating that `lvds_tx118093` is configured as an output register.

Example 17 shows that an output LVDS macro is configured in bypass mode and the built-in output register is not used. The timing path starts at the clock pin `CLKOUT` of the I/O register `pin_o_data`, passes through LVDS instance `lvds_tx183417`, and ends at output port `o_data`.

Example 17. LVDS Output Timing Path in Bypass Mode

```
 Startpoint: pin_o_data
               (rising edge-triggered flip-flop clocked by i_Clk)
  Endpoint: o_data
               (output port clocked by o_Clk)
  Path Group: o_Clk
  Path Type: max

  Point                                                    Incr       Path
  ------------------------------------------------------------------------------
  clock i_Clk (rise edge)                                 0.000      0.000
  clock network delay (propagated)                        2.530      2.530
  pin_o_data/CLKOUT (C66002_000000000000C4029820A060000_L_V25_LVDS)
                                                          0.000      2.530 r
  pin_o_data/DIN (C66002_000000000000C4029820A060000_L_V25_LVDS)
                                                          0.898 &    3.428 f
  lvds_tx183417/DIN (C69000_000002450000)                 0.000 &    3.428 f
  lvds_tx183417/LVDSOUT (C69000_000002450000) <-          1.565 &    4.994 f
  o_data (out)                                            0.000 &    4.994 f
  data arrival time                                                  4.994
------------------------------------------------------------------------------
```

Other Timing

In HardCopy ASICs, except for a PLL block, the reset/clear pin of a sequential cell is typically named `ACLR`, `NCLR`, or `*CLR*` in the timing reports.

Recovery Path

Example 18 shows a recovery path.

Example 18. Recovery Path

```
Startpoint: txdpa0/reset3n
               (rising edge-triggered flip-flop clocked by iqclk)
  Endpoint: pin_ddio_ina[0]_27
               (recovery check against falling-edge clock iqclk)
  Path Group: **async_default**
  Path Type: max

  Point                                                    Incr       Path
  ------------------------------------------------------------------------------
  clock iqclk (rise edge)                                 0.000      0.000
  clock network delay (propagated)                        1.785      1.785
  txdpa0/reset3n/CLK (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)      0.000      1.785 r
  txdpa0/reset3n/Q (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)        0.143 &    1.929 f
  lcell_comb8679/OUT (DEL_1)                              0.145 &    2.074 f
  lcell_comb8680/OUT (DEL_1)                              0.357 &    2.431 f
  lcell_comb7462/OUT (BUF_D6)                             0.401 &    2.832 f
  pin_ddio_ina[0]_27/ACLR (C66000_0000000D18A0040299205000000_V33_LVTTL)
                                                          0.031 &    2.864 f
  data arrival time                                                  2.864

  clock iqclk (fall edge)                                 3.255      3.255
  clock network delay (propagated)                        1.816      5.071
  clock reconvergence pessimism                           0.010      5.082
  inter-clock uncertainty                                -0.150      4.932
  pin_ddio_ina[0]_27/CLKIN (C66000_0000000D18A0040299205000000_V33_LVTTL)
                                                                     4.932 f
  library recovery time                                  -0.504      4.428
  data required time                                                 4.428
  ------------------------------------------------------------------------------
  data required time                                                 4.428
  data arrival time                                                 -2.864
  ------------------------------------------------------------------------------
  slack (MET)                                                        1.564
```

In Example 18, `Path Type: max` implies the path is either a setup or recovery path. Data ends at the `ACLR` pin of I/O instance `pin_ddio_ina[0]_27`; therefore, it is a recovery path. In addition, `library recovery time` confirms it is a recovery path.

Removal Path

Example 19 shows a removal path.

Example 19. Removal Path

```
Startpoint: txdpa0/reset3n
              (rising edge-triggered flip-flop clocked by iqclk)
 Endpoint: pin_ddio_ina[0]_27
              (removal check against rising-edge clock iqclk)
 Path Group: **async_default**
 Path Type: min

 Point                                                   Incr       Path
 ------------------------------------------------------------------------------
 clock iqclk (rise edge)                                0.000      0.000
 clock network delay (propagated)                       1.759      1.759
 txdpa0/reset3n/CLK (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)     0.000      1.759 r
 txdpa0/reset3n/Q (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)       0.143 &    1.903 f
 lcell_comb8679/OUT (DEL_1)                             0.145 &    2.048 f
 lcell_comb8680/OUT (DEL_1)                             0.354 &    2.402 f
 lcell_comb7462/OUT (BUF_D6)                            0.328 &    2.730 f
 pin_ddio_ina[0]_27/ACLR (C66000_0000000D18A0040299205000000_V33_LVTTL)
                                                        0.001 &    2.731 f
 data arrival time                                                 2.731

 clock iqclk (rise edge)                                0.000      0.000
 clock network delay (propagated)                       1.910      1.910
 clock reconvergence pessimism                         -0.018      1.892
 inter-clock uncertainty                                0.050      1.942
 pin_ddio_ina[0]_27/CLKIN (C66000_0000000D18A0040299205000000_V33_LVTTL)
                                                                   1.942 r
 library removal time                                  -0.128      1.814
 data required time                                                1.814
 ------------------------------------------------------------------------------
 data required time                                                1.814
 data arrival time                                                -2.731
 ------------------------------------------------------------------------------
 slack (MET)                                                       0.917
```

In Example 19, `Path Type: min` implies the path is either a hold or removal path. Data ends at the `ACLR` pin of I/O instance `pin_ddio_ina[0]_27`; therefore, it is a removal path. In addition, `library removal time` confirms it is a removal path.

Timing Paths Constrained with set_max_delay and set_min_delay

The `set_max_delay` and `set_min_delay` commands are point-to-point timing exception commands. For example, the command overrides the default single-cycle timing relationship for one or more timing paths. Other point-to-point timing exception commands include `set_multicycle_path` and `set_false_path`.

☞ A `set_max_delay` or `set_min_delay` command overrides a `set_multicycle_path` command.

For example, typical constraints `set_input_delay` and `set_output_delay` are applied to a bidir I/O port `sdram_dq[7]` first. Then `set_max_delay` and `set_min_delay` are applied to the input side as well, as shown in Example 20.

Example 20. Timing Constraints

```
set_output_delay -add_delay -max -clock [get_clocks {sdram_dqs_out}] 0.310 [ get_ports { sdram_dq[7] } ]
set_output_delay -add_delay -min -clock [get_clocks {sdram_dqs_out}] -0.480 [ get_ports { sdram_dq[7] } ]
set_output_delay -add_delay -max -clock_fall -clock [get_clocks {sdram_dqs_out}] 0.310 [ get_ports
{ sdram_dq[7] } ]
set_output_delay -add_delay -min -clock_fall -clock [get_clocks {sdram_dqs_out}] -0.480 [ get_ports
{ sdram_dq[7] } ]

set_input_delay -add_delay -max -clock [get_clocks {v_sdram_dqs_in}] 0.210 [ get_ports { sdram_dq[7] } ]
set_input_delay -add_delay -min -clock [get_clocks {v_sdram_dqs_in}] -0.310 [ get_ports { sdram_dq[7] } ]
set_input_delay -add_delay -max -clock_fall -clock [get_clocks {v_sdram_dqs_in}] 0.210 [ get_ports
{ sdram_dq[7] } ]
set_input_delay -add_delay -min -clock_fall -clock [get_clocks {v_sdram_dqs_in}] -0.310 [ get_ports
{ sdram_dq[7] } ]
set_max_delay 0.000 -from [ get_ports { sdram_dq[7] } ]
set_min_delay -3.757 -from [ get_ports { sdram_dq[7] } ]
```

For the output side, with a typical constraint `set_output_delay` associated with a clock, PrimeTime reports the typical cycle edge-to-edge transfer timing. Setup timing (`Path Type: max`) is checked at clock edge 3.757 ns of associated clock `sdram_dqs_out`; hold timing (`Path Type: min`) is checked at clock edge 0.000 ns.

The maximum output delay number 0.310 can be seen as `output external delay` in the `Path : max` timing report; the minimum output delay number –0.480 can be seen as `output external delay` in the `Path : min` timing report, as shown in Example 21 and Example 22.

Example 21. Timing Path Constrained with set_output_delay (part 1)

```
Startpoint: pin_bidir_io[0]
             (falling edge-triggered flip-flop clocked by ddrpll|altpll|pll|clk[1])
Endpoint: sdram_dq[7]
             (output port clocked by sdram_dqs_out)
Path Group: sdram_dqs_out
Path Type: max

Point                                                       Incr       Path
-------------------------------------------------------------------------------
clock ddrpll|altpll|pll|clk[1] (fall edge)
                                                           1.252      1.252
clock network delay (propagated)                          -0.070      1.182
pin_bidir_io[0]/CLKOUT (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                           0.000      1.182 f
pin_bidir_io[0]/DIN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                           1.289 &    2.471 r
pin_bidir_io[0]/PIN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                           1.888 &    4.359 r
sdram_dq[7] (inout)                                        0.000 &    4.359 r
data arrival time                                                     4.359

clock sdram_dqs_out (fall edge)                            3.757      3.757
clock network delay (propagated)                           3.060      6.817
clock reconvergence pessimism                              0.001      6.818
inter-clock uncertainty                                   -0.400      6.418
output external delay                                     -0.310      6.108
data required time                                                    6.108
-------------------------------------------------------------------------------
data required time                                                    6.108
data arrival time                                                    -4.359
-------------------------------------------------------------------------------
slack (MET)                                                           1.749
```

Example 22. Timing Path Constrained with set_output_delay (part 2)

```
Startpoint: pin_bidir_io[0]
             (falling edge-triggered flip-flop clocked by ddrpll|altpll|pll|clk[1])
Endpoint: sdram_dq[7]
             (output port clocked by sdram_dqs_out)
Path Group: sdram_dqs_out
Path Type: min

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock ddrpll|altpll|pll|clk[1] (fall edge)
                                                       1.252      1.252
clock network delay (propagated)                      -0.139      1.113
pin_bidir_io[0]/CLKOUT (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                       0.000      1.113 f
pin_bidir_io[0]/DIN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                       1.282 &    2.396 f
pin_bidir_io[0]/PIN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                       1.879 &    4.275 f
sdram_dq[7] (inout)                                    0.000 &    4.275 f
data arrival time                                                 4.275

clock sdram_dqs_out (rise edge)                        0.000      0.000
clock network delay (propagated)                       3.276      3.276
clock reconvergence pessimism                         -0.001      3.275
inter-clock uncertainty                                0.180      3.455
output external delay                                  0.480      3.935
data required time                                                3.935
-----------------------------------------------------------------------------
data required time                                                3.935
data arrival time                                                -4.275
-----------------------------------------------------------------------------
slack (MET)                                                       0.340
```

For the input side, timing exception command `set_max_delay 0.000 -from [ get_ports { sdram_dq[7] } ]` and `set_min_delay -3.757 -from [ get_ports { sdram_dq[7] } ]` dominate the `set_input_delay` constraints. PrimeTime does not check timing at the rise or fall edge of a capture clock, but checks timing against the `max_delay` or `min_delay`.

The `set_input_delay max 0.210` and `min -0.310` are also applied in PrimeTime and are shown as `input external delay` in the timing reports. When calculating the `set_max_delay/set_min_delay` numbers, designers may need to subtract the `input_delay max/min numbers` from the requirement, as shown in Example 23 and Example 24.

Example 23. Timing Path Constrained with set_input_delay and set_max_delay

```
Startpoint: sdram_dq[7]
               (input port clocked by v_sdram_dqs_in)
  Endpoint: cpu0/dq_reg_in[7]
               (rising edge-triggered flip-flop clocked by sdram_dqs_in)
  Path Group: sdram_dqs_in
  Path Type: max

  Point                                                    Incr       Path
  ------------------------------------------------------------------------------
  input external delay                                    0.210      0.210 f
  sdram_dq[7] (inout)                                     0.000 &    0.210 f
  pin_bidir_io[0]/PIN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                          0.069 *    0.279 f
  pin_bidir_io[0]/PINin (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                          0.000      0.279 f
  pin_bidir_io[0]/DATOVR (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                          0.380 H    0.659 f
  pin_bidir_io[0]/CDATA0IN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                          1.413 &    2.072 f
  lcell_comb129704/OUT (BUF_D6)                           0.576 &    2.648 f
  cpu0/dq_reg_in[7]/D (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)     0.153 &    2.801 f
  data arrival time                                                  2.801

  max_delay                                               0.000      0.000
  clock network delay (propagated)                        3.892      3.892
  clock reconvergence pessimism                           0.000      3.892
  inter-clock uncertainty                                -0.130      3.762
  library setup time                                     -0.410      3.352
  data required time                                                 3.352
  ------------------------------------------------------------------------------
  data required time                                                 3.352
  data arrival time                                                 -2.801
  ------------------------------------------------------------------------------
  slack (MET)                                                        0.551
```

Example 24. Timing Path Constrained with set_input_delay and set_min_delay

```
Startpoint: sdram_dq[7]
             (input port clocked by v_sdram_dqs_in)
Endpoint: cpu0/dq_reg_in[7]
             (rising edge-triggered flip-flop clocked by sdram_dqs_in)
Path Group: sdram_dqs_in
Path Type: min

Point                                                    Incr       Path
-------------------------------------------------------------------------------
input external delay                                   -0.310     -0.310 r
sdram_dq[7] (inout)                                     0.000 &   -0.310 r
pin_bidir_io[0]/PIN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                        0.069 *   -0.241 r
pin_bidir_io[0]/PINin (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                        0.000     -0.241 r
pin_bidir_io[0]/DATOVR (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                        0.393 H    0.153 r
pin_bidir_io[0]/CDATA0IN (C670023_0000000100046C04D90002206A8_V25_SSTL_2_II)
                                                        1.366 &    1.518 r
lcell_comb129704/OUT (BUF_D6)                           0.445 &    1.963 r
cpu0/dq_reg_in[7]/D (DFF_D1_CLK1_NCLR1_RSCN1_SCIN1)     0.114 &    2.077 r
data arrival time                                                  2.077

min_delay                                              -3.757     -3.757
clock network delay (propagated)                        4.037      0.280
clock reconvergence pessimism                           0.000      0.280
inter-clock uncertainty                                 0.130      0.410
library hold time                                      -0.093      0.317
data required time                                                 0.317
-------------------------------------------------------------------------------
data required time                                                 0.317
data arrival time                                                 -2.077
-------------------------------------------------------------------------------
slack (MET)                                                        1.760
```

Conclusion

PrimeTime timing reports are the standard deliverable from the Altera HardCopy Design Center to the designer. The designer must review these timing reports and approve them before the design can proceed to STA sign-off. Basic register-to-register timing transfers in PrimeTime are described in this application note. Various examples are provided and explained to help the designer understand HardCopy ASIC-specific pin and instance names for register, memory, DSP, I/O, PLL, and other blocks.

Document Revision History

Table 1 shows the revision history for this application note.

Table 1. Document Revision History

Date	Version	Changes Made
March 2010	2.0	■ Changed “HardCopy devices” to “HardCopy ASIC”. ■ Minor text edits.
November 2008	1.0	Initial release.

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