



AN 692: Power Sequencing Considerations for Intel[®] Cyclone[®] 10 GX, Intel[®] Arria[®] 10, Intel[®] Stratix[®] 10, and Intel[®] Agilex[™] Devices



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1. Overview and Related Information

The Intel® Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix® 10 devices require specific power-up and power-down sequences. Intel Agilex™ devices require a specific power-up sequence.

The power rails in those devices are each divided into several groups. Refer to the *Device Family Pin Connection Guidelines*, "Power Management" chapters in the *Core Fabric and General Purpose I/Os Handbooks*, and the *Power Management User Guides* for additional details.

For the Power On Reset (POR) delay time specifications, refer to the *Device Data Sheets*.

Table 1. Related Information

| Title | Link |
|--|---|
| AN 891: Using the Reset Release Intel Stratix 10 FPGA IP | AN 891: Using the Reset Release Intel Stratix 10 FPGA IP |
| Errata Sheets | https://www.intel.com/content/www/us/en/programmable/documentation/lit-es.html |
| Intel Agilex Power Management User Guide | Intel Agilex Power Management User Guide |
| Intel Agilex Device Family Pin Connection Guidelines | Intel Agilex Device Family Pin Connection Guidelines |
| Intel Agilex Device Data Sheet | Intel Agilex Device Data Sheet |
| Intel Stratix 10 Power Management User Guide | Intel Stratix 10 Power Management User Guide |
| Intel Stratix 10 Device Family Pin Connection Guidelines | Intel Stratix 10 Device Family Pin Connection Guidelines |
| Intel Stratix 10 Device Data Sheet | Intel Stratix 10 Device Data Sheet |
| Power Management in Intel Arria 10 Devices | Power Management in Intel Arria 10 Devices |
| Intel Arria 10 GX, GT, and SX Pin Connection Guidelines | Intel Arria 10 GX, GT, and SX Pin Connection Guidelines |
| Intel Arria 10 Device Data Sheet | Intel Arria 10 Device Data Sheet |
| Power Management in Intel Cyclone 10 GX Devices | Power Management in Intel Cyclone 10 GX Devices |
| Intel Cyclone 10 GX Device Family Pin Connection Guidelines | Intel Cyclone 10 GX Device Family Pin Connection Guidelines |
| Intel Cyclone 10 GX Device Data Sheet | Intel Cyclone 10 GX Device Data Sheet |
| Quad-Comparator Circuit Provides Power-Down Sequencing At Low Cost | How2Power Today, Josh Mandelcorn |



1.1. Controlled Sequence Designs

1.1.1. Programmable Power Management Controller (PPMC)

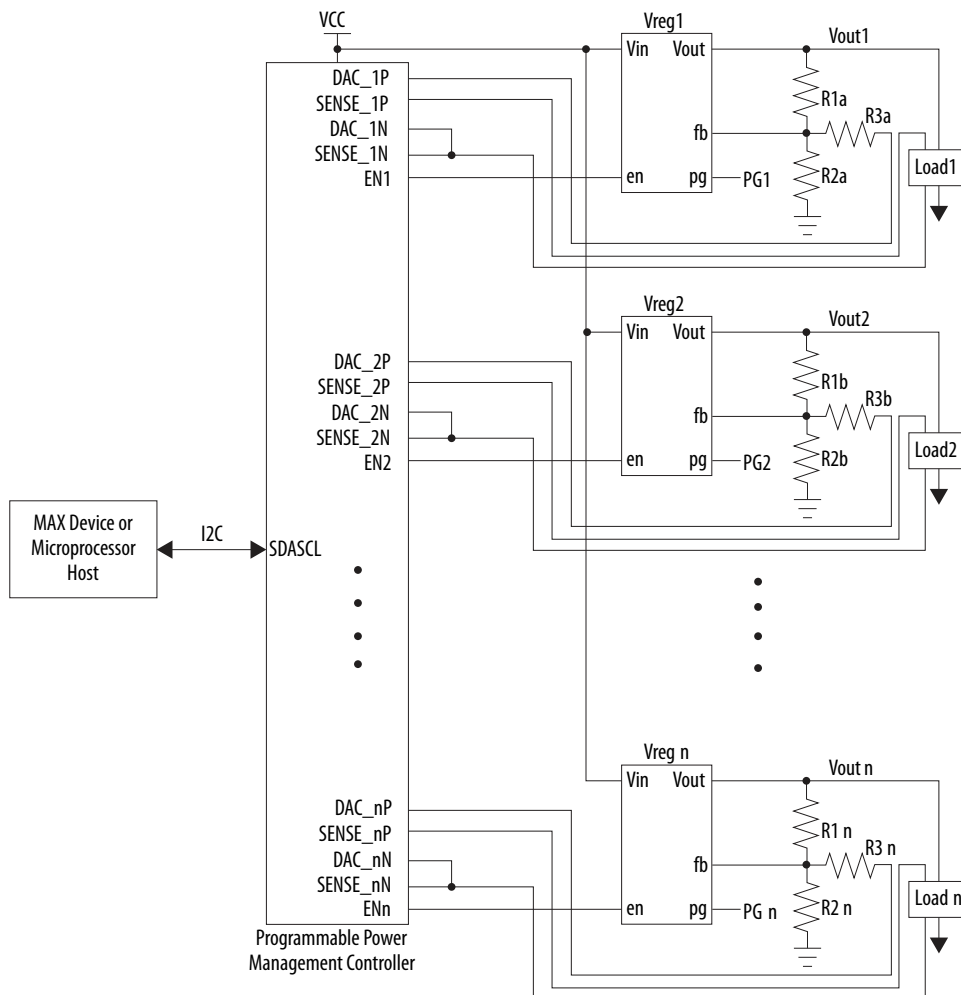
Using a programmable power management controller provides a full-featured option to implement the power sequencing requirements.

These controllers provide the necessary power-up/down sequence control functions. These controllers can dynamically monitor and scale the regulator's output voltage, and supervise fault conditions such as over voltage or under voltage. To program the power management controller, typically a PMBus or I²C interface is used to connect to an intelligent host such as the system's microprocessor.

PPMC can be an optimal solution for systems in which up-time and fault tolerance are critical features and voltage monitoring and fault reporting are essential system requirements.

1.1.1.1. PPMC Example Design

Figure 1. Simplified Programmable Power Management Controller With Multiple Channels



A single channel of the PPMC typically provides the following features:

- Differential sense line inputs to remotely monitor the load voltage.
- Digital-to-Analog Converter (DAC) outputs to trim the regulator output voltages. The DAC outputs drive the regulator's feedback input (fb) and control the regulator's output voltage.
- Enable Outputs (EN1, EN2, . . . ENn) that drive the voltage regulator's Enable Inputs (en). The regulator's enable inputs control the desired power-up/down sequence.

Typically, PPMC devices have multiple channels so that a single controller can sequence multiple regulators. If more channels are required than what is offered by a single device, then multiple devices can be cascaded. A separate host interface (PMBus or I²C) is used to connect the system processor and the PPMC to manage the controller software and programming.

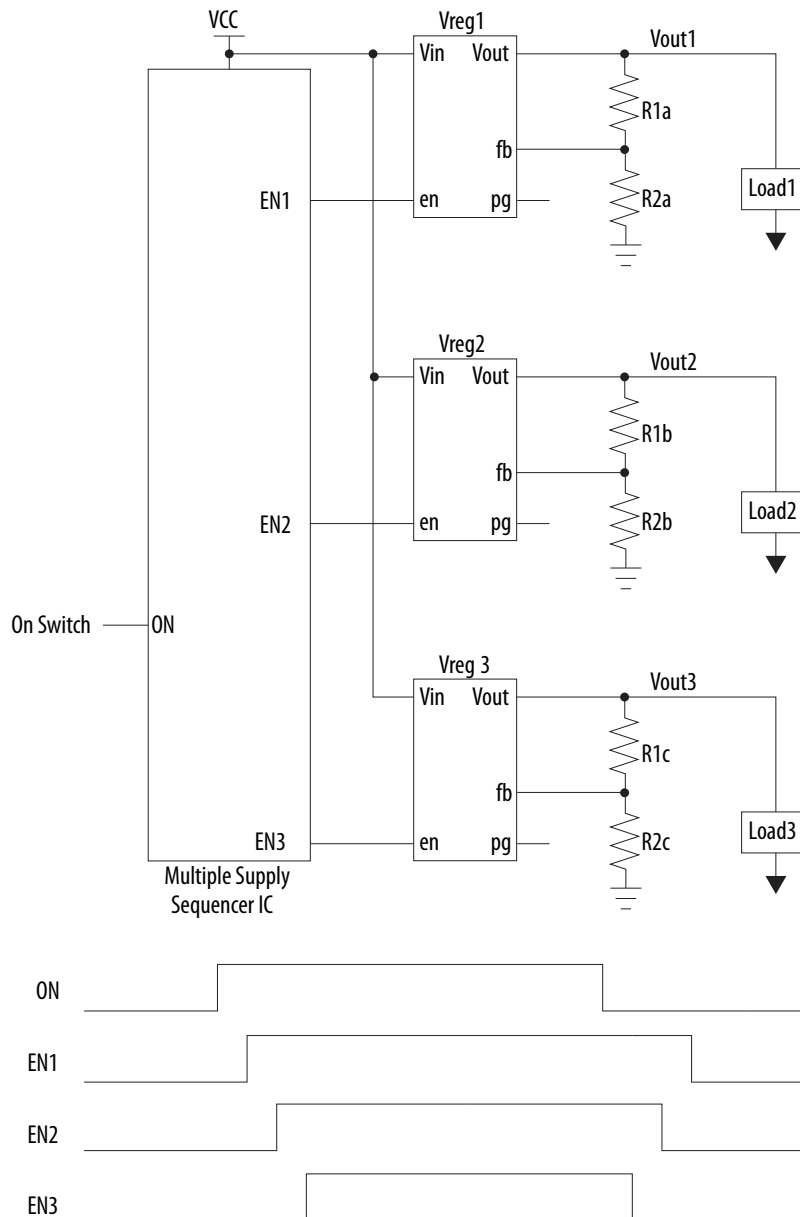
Consult your power module vendor for more information about PPMC.

1.1.1.2. Multiple Supply Sequencer

If only simple power-up/power-down sequencing is required to follow the power sequencing considerations, a low-cost multiple supply sequencer IC can be used.

These devices offer multiple sequenced output enables that are controlled by a dedicated input. When the input is switched on, the Output Enables (EN1/ EN2 /EN3) turn on in successive order after a programmed time delay. This time delay between the output enables can be adjusted.

Figure 2. Example Schematic Design of Multiple Supply IC





Consult your power module vendor for more information about multiple supply sequencer ICs.

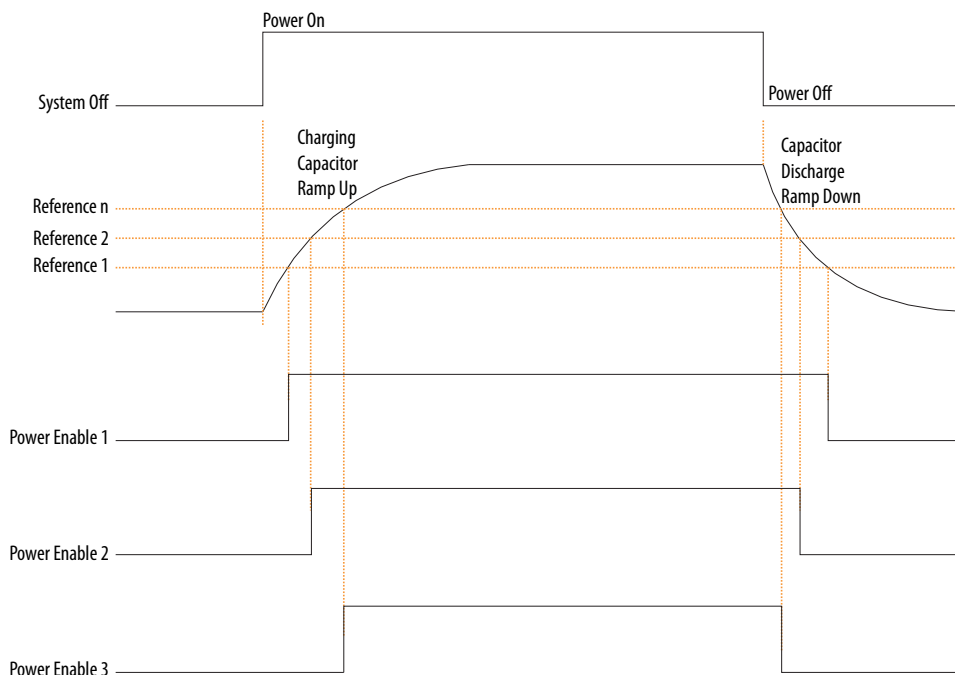
1.1.2. Low-Cost Discrete Sequencer Design

A discrete sequencer design is a low-cost option in which the charging and discharging voltage of a simple resistor-capacitor (RC) network and preset reference voltage levels are used.

The RC ramp-up/down voltage is compared with preset reference voltage levels to generate a series of sequenced power enable outputs to control the voltage regulators.

The power-on event triggers the capacitor charging. As the capacitor voltage rises above each of the preset reference voltage levels, the power enable outputs are sequentially turned on. Similarly, for the power-down event, the discharging of the capacitor causes the power enable outputs to turn off in the reverse sequential order.

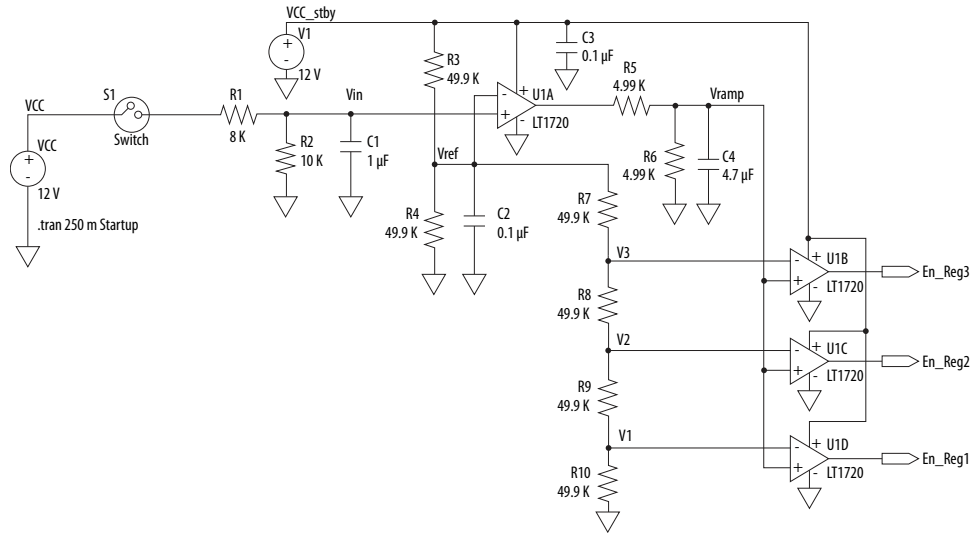
Figure 3. Power-Up / Power-Down Sequencer



1.1.2.1. Low-Cost Sequencer Circuit Description

The example design for the simple low-cost power-up/down sequencer uses a quad comparator IC (**U1**) and discrete resistors and capacitors.

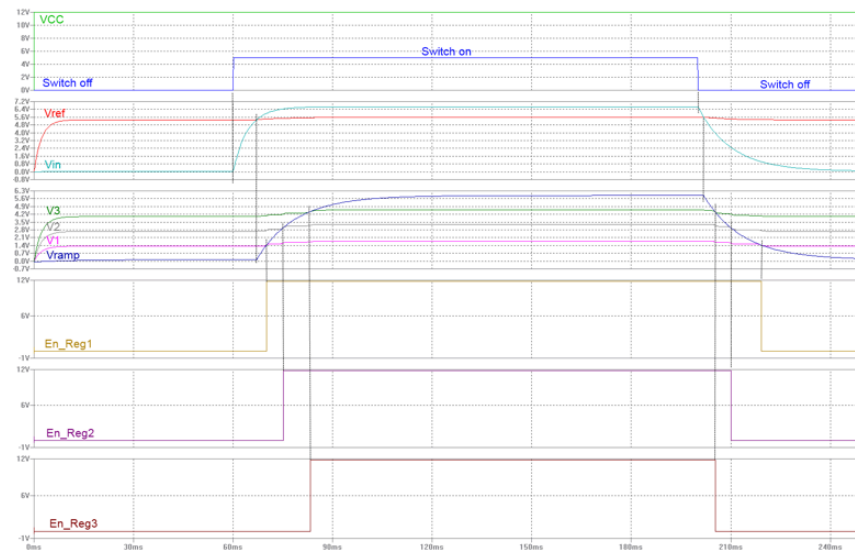
Figure 4. Low-Cost Sequencer Example Circuit



A system standby voltage VCC_stby is always present to power the comparator **U1A**. A reference voltage $Vref$ is generated from VCC_stby through resistor dividers **R3** and **R4**. $Vref$ is the reference voltage for the inverting input of comparator **U1A**. A more accurate $Vref$ can be generated using a precision trimmed zener diode in place of resistor **R4**. The resistor ladder network consists of resistors **R7**, **R8**, **R9**, and **R10**. This ladder network further divides the reference voltages $V3$, $V2$, and $V1$. Comparator (**U1B**, **U1C**, and **U1D**) outputs drive the associated regulator enables (En_reg3 , En_Reg2 , En_Reg1). These outputs turn On/Off the voltage regulators (not shown). Switch **S1** is the system power On/Off switch.

1.1.2.2. Low-Cost Discrete Sequencer Simulation Results

Figure 5. Circuit Simulation Results for Power-Up and Power-Down Events





Initially, the power sequencer circuit is not operational because the power switch **S1** is open. As a result, all regulator enables (En_Reg1 , En_Reg2 , and En_Reg3) are low. As the regulator enables drive the voltage regulators, all voltage regulators are turned off.

Power ON

- When switch **S1** is closed, the system turns on and the voltage VCC charges the capacitor **C1** to voltage level V_{in} .
- **C1** is charged through resistor **R1**. Voltage level V_{in} depends on the values of **R1** and **R2** which form voltage divider and $V_{in} = (R2 / (R1 + R2)) * VCC$. **R1** and **R2** are selected such that the value of V_{in} is slightly higher than comparator **U1A**'s reference voltage V_{ref} .
- When the value of V_{in} rises above V_{ref} , comparator **U1A**'s output goes high and capacitor **C4** starts charging through resistor **R5**.
- Resistors **R5** and **R6** set the ramp voltage V_{ramp} . Resistor **R5** and capacitor **C4** define the time constant for the ramp rate of V_{ramp} . V_{ramp} is the input voltage to the non-inverting inputs of comparators **U1B**, **U1C**, and **U1D**. As V_{ramp} rises above the voltage references (**V1**, **V2**, and **V3**), it sequentially trips comparators **U1D**, **U1C**, and **U1B**, turning on regulator enables En_Reg1 , En_Reg2 , and En_Reg3 .

Power OFF

- The order of the power-down sequence is reverse of the power-up sequence.
- When switch **S1** is opened, the system starts shutting down. Capacitor **C1** starts discharging through **R2**. **R2** and **C1** set the decay rate of V_{in} during the power-down cycle.
- When V_{in} falls below V_{ref} , comparator **U1A**'s output turns off. This discharges V_{ramp} through the parallel combination of **R5** and **R6**.
- As V_{ramp} discharges below **V3**, **V2**, and **V1**, the comparators **U1B**, **U1C** and **U1D** sequentially turn off their regulator enables.

This example circuit can be easily expanded to support more regulator enable (reg_en) outputs.

To expand the circuit, add more comparators and extend the resistor ladder network to generate additional reference voltage comparison points (for example, **V4**, **V5**, etc). Also, increase the V_{ramp} charging/discharging rate to allow more time between the additional regulator enables. This time delay is controlled by the time constant determined by **R5**, **R6**, and **C4**.

1.2. Fault Tolerance

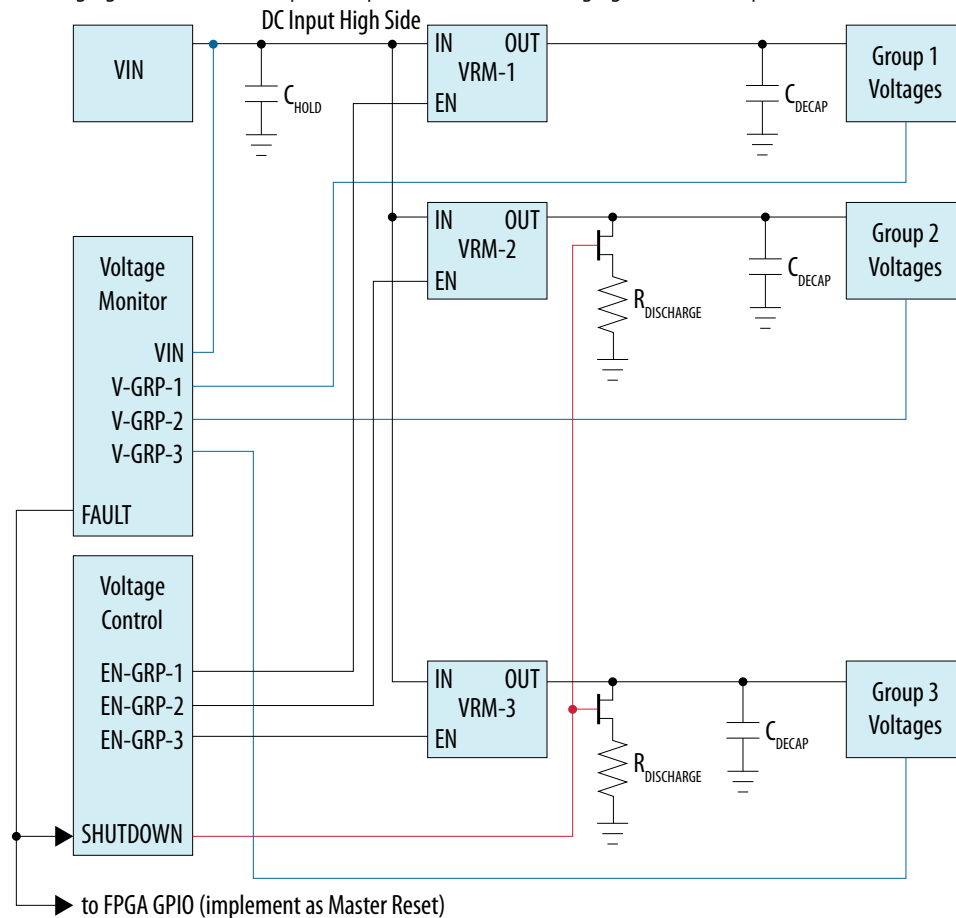
1.2.1. Managing Uncontrolled Loss of Power Events

Sudden loss of power events such as a utility grid blackout, accidental removal of the system power cable, or other uncontrolled loss of power events can create difficult power management scenarios for the system designer. To manage these types of exceptions, ensure the power management design incorporates these features:

1. Loss of power detection
2. Hold-up capacitor (if needed) to keep the Power Management Circuitry operational during shutdown
3. Reset logic to the FPGA and system to minimize power consumption during shutdown
4. Rapid discharge circuit for each power group to minimize power-down time

Figure 6. Fault Tolerant Block Diagram

The following figure shows a conceptual implementation for managing uncontrolled power loss events.





The Power Management Circuit (in the above diagram) is powered directly from the VIN high-side DC input voltage (for example, 12 V or higher) but can operate down to a lower voltage such as 5 V. You may need C_{HOLD} to maintain sufficient charge to keep the Power Management Circuitry operational during loss of power events. C_{DECAP} Group 1-3 represents the total decoupling capacitance associated with each power rail grouping. $R_{\text{DISCHARGE}}$ 2-3 and its associated power FETs enable fast discharging of each power group voltage to 0 V when you initiate a shutdown sequence. The fast discharging circuit speeds up the power-down cycle of each rail (as the natural RC discharge decay can be very slow) and can also define the order in which the rails discharge by trimming $R_{\text{DISCHARGE}}$. Without the fast discharge circuit, the shutdown time can be very long, requiring a larger capacitance for C_{HOLD} .

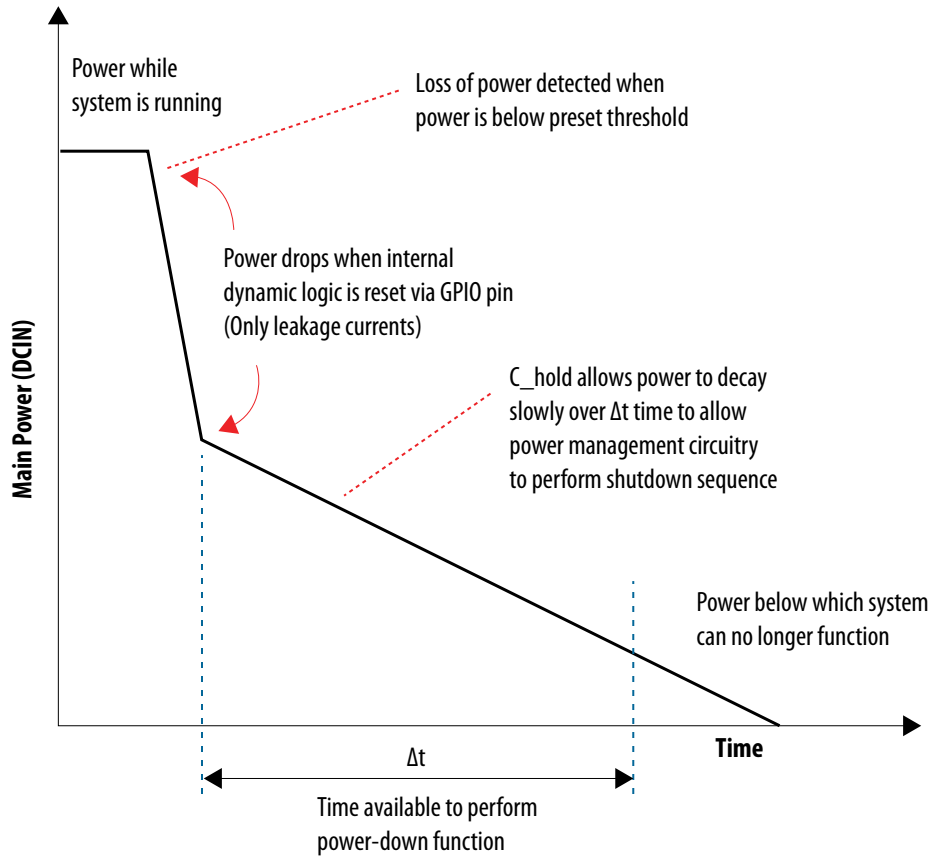
Theory of Operation

While the system is running, the high-side DC input is maintained at VIN +/-10% tolerance. The power loss detection circuit continuously monitors the DC input for a loss of power event. This detection circuit can be a simple comparator with a reference voltage set to a threshold slightly below the -10% threshold, or it can be an Analog-to-Digital Converter (ADC) employing multiple successive samplings to discriminate against false power interruptions.

When a valid loss of power event occurs, the detection circuit generates a reset to the Voltage Controller and the FPGA. It is the user's responsibility to use the reset signal to reset as much of the design as possible in order to reduce dynamic power and the operational current of the FPGA by putting it into a low Static Power (Pstatic) state. Concurrently, the Power Management Circuit is triggered to initiate a shutdown sequence. This reduces the value of C_{HOLD} needed to support the Power Management Circuitry during the shutdown process.

Note: The Voltage Monitor generated reset signal and the reset IP signal should be tied to the same reset distribution. This helps in resetting the PLLs and additional power reduction. Refer to the *AN 891: Using the Reset Release Intel Stratix 10 FPGA IP* for more details on Intel Stratix 10 Reset IP.

Figure 7. Main Power Loss Detection and Shutdown Event



The Δt time that the Power Management Circuit has to perform a graceful power-down is dependent on the total power consumption of the system and C_{HOLD} capacitor needed to maintain reliable system power. While the individual power groups are being disabled in reverse sequential order, the FET for each particular group is also successively turned on to facilitate a rapid discharge of their respective power rail to ground through the $R_{DISCHARGE}$ resistors. You must properly size the discharge FET and resistor to handle the instantaneous discharge current through it. The discharge resistor must be able to handle the single pulse power load for the duration of the discharge time. You can determine this from the data sheet of the selected resistor. The data sheet typically provides this data as a graph plotting the *Maximum pulse load power* versus the *Pulse duration* for various resistor package sizes. Determine the value of C_{HOLD} from the energy stored in the capacitor and the total power required to maintain system operation, calculated from the following equations:

$$\text{Power} = \frac{\Delta E}{\Delta t} = \frac{\frac{1}{2} C (v_1^2 - v_2^2)}{(t_1 - t_2)}$$

$$C_{\text{hold}} = \frac{2 \times (P_{\text{FPGA}_{\text{leakage}}} + P_{\text{System}_{\text{peripherals}}}) \times (t_1 - t_2)}{\text{Eff} \times (v_1^2 - v_2^2)}$$

E = Energy stored in the capacitor in *Joules*



P = Power in *Watts*

V = Voltage in *Volts*

C = Capacitance in *Farads*

t = Time in *Seconds*

Eff = Efficiency percentage of the regulator

Example Design

Consider an FPGA system that has total quiescent current of 25 A when the system is under reset (FPGA leakage and total system standby current), and the hold time of the capacitor needs to be 1 ms as the voltage drops from 10 V to 5 V. Also, assume that the voltage rail is 0.9 V.

Determine the C_{HOLD} capacitance required for the Power Management Controller to maintain operation so that you can complete a proper power-down sequence.

From the above equation:

$$\begin{aligned} C_{\text{HOLD}} &= (2 * 25 \text{ A} * 0.9 \text{ V} * .001 \text{ s}) / (0.85 * (10^2 - 5^2)) \\ &= 0.045 / 63.75 \text{ }\mu\text{F} \\ &= 706 \text{ }\mu\text{F} \end{aligned}$$

Related Information

[Intel Stratix 10 AN 891: Using the Reset Release Intel Stratix 10 FPGA IP](#)

1.2.2. Sequential vs. Simultaneous Power-Down

Some sequencers on the market may simultaneously bring all voltage rails down instead of powering the voltage rails down sequentially.

Take care when selecting a design for controlling the sequence during a fault condition. Non-sequential power-down controllers can violate power-down specifications. External active discharge and trimming R_{DISCHARGE} can alleviate this problem (refer to the "Fault Tolerant Block Diagram").

1.2.3. Voltage Regulators with Clamping Capability

There are voltage regulators on the market that clamp the output to GND in the event of a fault condition. When choosing the voltage regulator, ensure that this clamping feature can be disabled. Group 2 can be clamped only if it is clamped with the same control signal as Group 3. Otherwise, make sure that regulators in Group 1 and Group 2 do not have this option enabled.

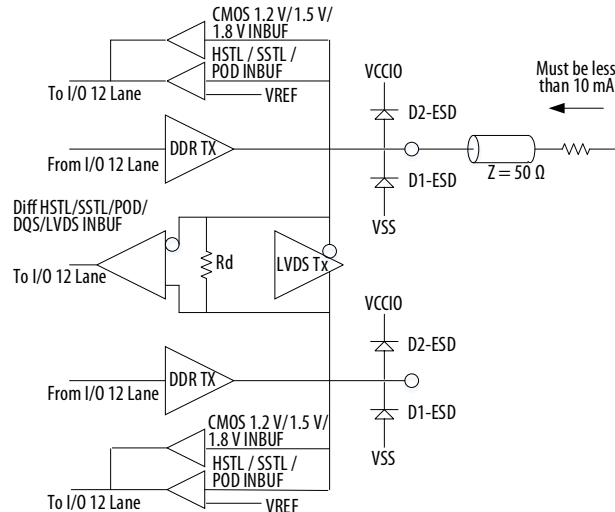
1.3. Driving Unpowered FPGA Pins

1.3.1. LVDS I/O Pin Guidance for Unpowered FPGA

The LVDS I/O pins do not support 'Hot-Socketing;' these LVDS I/O pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per I/O bank. The voltage level of the LVDS I/O pin must not exceed 1.89 V.

A series resistor can be used to help limit current if necessary. The worst case assumption is that VCCIO is unpowered (0 V) while its LVDS I/O pin is driven with a voltage less than the allowable maximum (1.89 V). Refer to the figure below.

Figure 8. LVDS I/O Banks Buffer Structure



1.3.2. Transceiver Pin Guidance for Unpowered FPGA

Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 L-tile and H-tile device transceiver pins do not support 'Hot-Socketing.'

Fully configure the transceiver block before driving or having any activity on the Intel Cyclone 10 GX and Intel Arria 10 device transceiver pins.

Intel Stratix 10 L-tile and H-tile device transceiver pins do not support 'Hot-Socketing' although these transceiver pins can tolerate 1.0 Vp-p during power-up or power-down.

1.4. Document Revision History for AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, Intel Stratix 10, and Intel Agilex Devices

| Document Version | Changes |
|------------------|--|
| 2019.10.11 | Made the following changes: <ul style="list-style-type: none"> Added references to the correct resources for up-to-date voltage rails and POR specifications. Added Intel Agilex device references. |
| 2019.06.12 | Made the following changes: <ul style="list-style-type: none"> Updated the <i>Managing Uncontrolled Loss of Power Events</i> section. <ul style="list-style-type: none"> Updated FPGA pin in the "Fault Tolerance Block Diagram". Updated the <i>Theory of Operation</i> section. Updated the "Main Power Loss Detection and Shutdown Event" figure to reflect the removal of nCONFIG and changes to the drop in the power event. |
| 2019.05.20 | Made the following changes: <ul style="list-style-type: none"> Updated V_{CCIO_UIB} power grouping in the "Voltage Rail" table. |

continued...



| Document Version | Changes |
|------------------|---|
| 2019.03.05 | <p>Made the following changes:</p> <ul style="list-style-type: none"> Added E-tile voltage rails and power-up exception to <i>Power-Up Sequence Requirements</i>. Changed Original Text: For Intel Cyclone 10 GX and Intel Arria 10 devices, you can combine and ramp up Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as Group 2 power rails VCCIO, VCCPGM, and VCCIO_HPS. to Updated Text: For Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices, you can combine and ramp up Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as Group 2 power rail VCCPT. Changed 1.1 Vp-p references to 1.0 Vp-p. |
| 2018.04.13 | <p>Made the following changes:</p> <ul style="list-style-type: none"> Deleted the note: To satisfy the power-up requirements, program the FPGA device immediately after the power-up sequence completes. Added links to <i>References</i> and moved it to the beginning. |
| 2018.02.28 | <p>Made the following changes:</p> <ul style="list-style-type: none"> Added Intel Cyclone 10 GX device support. Added "Sequential vs Simultaneous Power-Down." Added "Voltage Regulators with Clamping Capability." Added "Driving Unpowered FPGA Pins" - "LVDS I/O Pin Guidance for Unpowered FPGA" and "Transceiver Pin Guidance for Unpowered FPGA." Removed Hot-Plug support. Added POR Delay specifications for Intel Cyclone 10 GX and Intel Arria 10. |
| 2017.05.08 | <p>Made the following changes:</p> <ul style="list-style-type: none"> Added the following description for power-down sequence for Intel Arria 10 and Intel Stratix 10 devices "For Arria 10 and Stratix 10 devices, when the Group 3 power rails are 1.8V and share the same voltage regulator, then the Group 3 power rails can be combined with Group 2 power rails. In this case, Group 2 and Group 3 power rails can ramp down together." Updated the diagrams accordingly. Added the following note in "Hot-Plug Challenges" topic: "There are hot socket circuits in every 6-pack to monitor VCC, VCCT and VCCR power level. If any of those power supplies are not at operational level, all PMA outputs and inputs are gated low." |
| 2016.10.31 | <p>Made the following changes:</p> <ul style="list-style-type: none"> In the section "Hot Swap Controller and Regulator" updated the description to "When the line card is fully engaged, the card present indicator informs the host that a new card has been successfully inserted. The CONF_DONE signal should then be routed back to the master and sampled as an enable to the signals that are driven. This ensures that configuration is done, the device is stable, and that the master can drive the I/O to the newly powered up slave device without fear of damaging the part. The host system drives the line card's I/O pins and configures it for normal operation." In the "Hot-Plug Example" section added 2 new diagrams for "Hot-Plug Example using Staggered Pin Length Connectors." |
| 2016.09.20 | <p>Made the following change:</p> <ul style="list-style-type: none"> In topic "Power Sequence for Arria 10 and Stratix 10 Devices" for figure "Power-Down Sequence for Arria 10 Devices for combined Group2 and Group3 powers" edited the description to "During the power-up/down sequence, the device output pins are tri-stated. Intel recommends that the input pins should not be driven during this time to ensure long term reliability of the device." |
| 2016.06.16 | <p>Made the following changes:</p> <ul style="list-style-type: none"> Added new figures for "Power-Down Sequence for Arria 10 Devices", "Power-Down Sequence for Stratix 10 Devices" and "Power-Down Sequence for Arria 10 Devices for combined Group2 and Group3 powers". Added the "Power-Up Sequence Considerations for Stratix 10 Devices". Added a new section for "Managing Uncontrolled Loss of Power Events". Added a new figure for "Power-Up Sequence for Stratix 10 Devices". |
| 2015.1.02 | <p>Made the following change:</p> <ul style="list-style-type: none"> Clarified information in the "Power-Up Sequence for Arria 10 Devices" section. |
| 2013.09.06 | Initial release to MOLSON. |