HardCopy II Structured ASIC Family

November 2008, Version 1.1 Errata Sheet

Introduction

This errata sheet provides updated information on HardCopy® II devices. This document addresses known issues and includes methods to work around the issues.

Table 1 shows the specific issues affecting HardCopy II devices.

Table 1. Issues Affecting HardCopy II Devices

Issue	Affected Devices	Solution
Boundary-scan test (BST) exceptions prior to user mode.	HC230F1020	Refer to "Boundary-Scan Test Exceptions Prior to User Mode" on page 1
Configuration of the M4K memory block as a RAM requires a minimum of one clock pulse for initialization and proper operation.	All HardCopy II devices	Refer to "Configuration of the M4K Block as RAM" on page 2
Certain instances of PLL reconfiguration causes the scandone signal to remain in the low position. $T_{RECONFIGWAIT}$ specification added to this section ensures proper reconfiguration.	All Stratix II and HardCopy II devices	*(1)*
Removal of PLL Self-Reset support for Stratix II devices.	All Stratix II and HardCopy II devices	*(1)*

Note to Table 1:

(1) The migration of a Stratix II device to a HardCopy II device requires the equivalent functionality in its Stratix II prototype. For further information, refer to the *Stratix II FPGA Family Errata Sheet*.

HardCopy II Device Family Issues

The following are issues and solutions for HardCopy II devices.

Boundary-Scan Test Exceptions Prior to User Mode

For HardCopy II devices, the boundary-scan test (BST) can be performed prior to user mode (with `nConfig` pulled low) or during user mode. Under normal circumstances, prior to user mode, the I/O standard for all user I/Os is set to a default LVTTL of 3.3 V. You can drive data into the boundary-scan cells and pins by using the Joint Test Action Group (JTAG) instructions on all user I/O pins.

Due to restrictions in the silicon, the following exceptions apply when you perform the BST prior to user mode in a HC230F1020 device:

- The logic level on user I/Os that are programmed as output pins cannot be captured into the boundary-scan cells through JTAG instructions. Only the logic level on input and bidirectional single-ended I/Os can be captured into the boundary-scan cells by JTAG instructions.

- User I/Os that are programmed as differential input and output pin pairs can drive data independently, but cannot capture data from the pins into the boundary-scan cells.
- All I/O standards are determined by mask-programmed device settings instead of the 3.3-V LVTTL.

Solution

To work around these exceptions, use the Preconfig BSDLCustomizer tool to generate a customized BSDL file for the BST prior to user mode. The Preconfig BSDLCustomizer tool modifies the behavior of I/O pins in the generic BSDL file based on user-assigned values in the **.pin** file.

To download the Preconfig BSDLCustomizer tool, visit the Altera® website at www.altera.com.

For a successful chip-to-chip communication and BST on HC230 devices, ensure that all devices in the boundary-scan chain use the same I/O standards as in user mode.

Configuration of the M4K Block as RAM

The configuration of the M4K memory block as a RAM block in HardCopy II devices requires a minimum of one clock pulse for initialization and proper operation of the M4K. Not providing an initial clock pulse may result in incorrect write operations to the M4K.

An M4K design that utilizes two separate clock sources (such as the simple-dual port and true-dual port modes) requires a minimum of one clock pulse in each clock domain.

Designs that have a steady clock source to the M4K blocks do not experience this problem. M4K blocks that are configured as ROM blocks also do not experience this problem.

Revision History

Table 2 shows the revision history for this Errata Sheet.

Table 2. HardCopy II Structured ASIC Family Errata Sheet v1.1 Revision History

Version	Date	Change Summary
1.1	November 2008	■ Corrected third issue in first column in Table 1. ■ Minor text edits.
1.0	September 2007	Initial Release

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support
www.altera.com/support