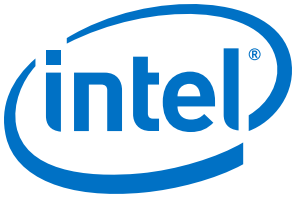

Intel Agilex Device Data Sheet

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Intel® Agilex™ Device Data Sheet

This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel® Agilex™ devices.

Until the data sheet status for a device reaches Final, the specifications are subject to change at any time and at Intel's discretion.

Table 1. Data Sheet Status for Intel Agilex Devices

Variant	Data Status
Intel Agilex F-series	Advance
Intel Agilex I-series	Advance

Table 2. Intel Agilex Device Grades and Speed Grades Supported

For specification status, see the *Data Sheet Status* table

Device Grade	Speed Grade Supported
Extended	–E1V (fastest)
	–E2V
	–E3V
	–E3E
	–E4F
Industrial	–I1V

continued...

Device Grade	Speed Grade Supported
	–I2V
	–I3V
	–I3E

The suffix after the speed grade denotes the power options offered in Intel Agilex devices.

- V—standard power (VID)
- E—lower power (VID)
- F—fixed voltage

Related Information

Package and Thermal Resistance website

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Agilex devices.

Operating Conditions

Intel Agilex devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Agilex devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Agilex devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Absolute Maximum Rating for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.5	1.14	V
V_{CCP}	Periphery circuitry power supply	—	–0.5	1.14	V
V_{CCPT}	Power supply for I/O PLL and I/O pre-driver	—	–0.5	2.08	V
V_{CCR_CORE}	CRAM power supply	—	–0.5	2.08	V
V_{CCH}	Transceiver digital power supply	E-tile and P-tile devices	–0.5	1.21	V
V_{CCH_SDM}	SDM block transceiver digital power sense	E-tile and P-tile devices	–0.5	1.21	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O bank power sense of Bank 3A	—	–0.5	2.01	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
V_{CCL_SDM}	SDM block core voltage power supply	—	–0.5	1.07	V
$V_{CCFUSEWR\_SDM}$	SDM block fuse writing power supply	—	–0.5	2.4	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	–0.5	1.07	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V
V_{CCBAT}	Battery back-up power supply (For design security volatile key register)	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCIO_PIO}	I/O bank power supply	—	–0.5	2.01	V
V_{CCA_PLL}	I/O clock network power supply	—	–0.5	2.08	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCRT_GXE}	Transceiver power supply	E-tile devices	–0.5	1.21	V
$V_{CC\_HSSI\_GXE}$	E-tile digital signal power supply	E-tile devices	–0.5	1.21	V
$V_{CCRTPLL\_GXE}$	Transceiver PLL power supply	E-tile devices	–0.5	1.21	V
V_{CCH_GXE}	Analog power supply	E-tile devices	–0.5	1.47	V
V_{CCCLK_GXE}	LVPECL REFCLK power supply	E-tile devices	–0.5	3.41	V
V_{CCRT_GXP}	Transceiver power supply	P-tile devices	–0.5	1.21	V
$V_{CC\_HSSI\_GXP}$	P-tile digital signal power supply	P-tile devices	–0.5	1.21	V
V_{CCFUSE_GXP}	P-tile efuse power supply	P-tile devices	–0.5	1.21	V
V_{CCCLK_GXP}	P-tile I/O buffer power supply	P-tile devices	–0.5	2.46	V
V_{CCH_GXP}	High voltage power for transceiver	P-tile devices	–0.5	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.5	1.21	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply	—	–0.5	1.21	V
V_{CCPLL_HPS}	HPS PLL analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V
V_I	DC Input Voltage	V_{CCIO_PIO} = 1.2 V	–0.3	1.56	V
		V_{CCIO_PIO} = 1.5 V	0	1.7	V
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V	–0.3	2.19	V
I_{OUT} (1) (2)	DC output current per pin	V_{CCIO_PIO} = 1.2 V, 1.5 V (3)	–15	15	mA

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (4)	–20	20	mA
T_J	Absolute junction temperature	—	–55	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following tables and undershoot to –1.1 V when using V_{CCIO_HPS}/ V_{CCIO_SDM} of 1.8 V and –0.3 V when using V_{CCIO_PIO} of 1.2 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, when using 1.2 V I/O standard, a signal that overshoots to 1.71 V can only be at 1.71 V for ~3% over the lifetime of the device.

No overshooting beyond 1.7 V and undershooting below 0 V is allowed when using V_{CCIO_PIO} = 1.5 V.

(1) Total current per I/O bank must not exceed 100 mA.

(2) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

(3) The maximum current allowed through any I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA. The voltage level must not exceed 1.2 V.

(4) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 40 mA. The voltage level must not exceed 1.89 V.

Table 4. Maximum Allowed Overshoot During Transitions for Intel Agilex Devices (for 1.2 V I/O)

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.30	100	%
		V_{CCIO_PIO} + 0.35	37	%
		V_{CCIO_PIO} + 0.40	9	%
		V_{CCIO_PIO} + 0.45	3	%
		V_{CCIO_PIO} + 0.50	1	%
		> V_{CCIO_PIO} + 0.50	No Overshoot Allowed	%

Table 5. Maximum Allowed Overshoot During Transitions for Intel Agilex Devices (for 1.8 V I/O)

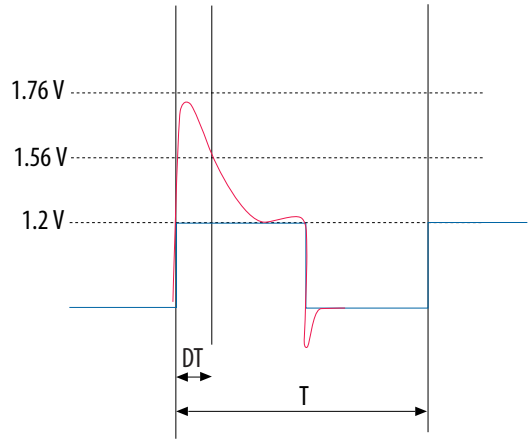
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_SDM} + 0.30, V_{CCIO_HPS} + 0.30	100	%
		V_{CCIO_SDM} + 0.35, V_{CCIO_HPS} + 0.35	60	%
		V_{CCIO_SDM} + 0.40, V_{CCIO_HPS} + 0.40	30	%
		V_{CCIO_SDM} + 0.45, V_{CCIO_HPS} + 0.45	20	%
		V_{CCIO_SDM} + 0.50, V_{CCIO_HPS} + 0.50	10	%
		V_{CCIO_SDM} + 0.55, V_{CCIO_HPS} + 0.55	6	%
		>V_{CCIO_SDM} + 0.55, >V_{CCIO_HPS} + 0.55	No Overshoot Allowed	%

When using 1.2 V V_{CCIO_PIO}, for an overshoot of 1.56 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

Figure 1. Intel Agilex Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Agilex devices.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions for Intel Agilex Devices

This table lists the steady-state voltage values expected for Intel Agilex devices. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum(5)	Typical	Maximum(5)	Unit
V_{CC}	Core voltage power supply	–1V, –2V, –3V, –3E(6)	(Typical) – 3%	0.685 – 0.90(7)	(Typical) + 3%	V
		–4F	0.776	0.8	0.824	V
V_{CCP}	Periphery circuitry power supply	–1V, –2V, –3V, –3E(6)	(Typical) – 3%	0.685 – 0.90(7)	(Typical) + 3%	V
		–4F	0.776	0.8	0.824	V
V_{CCPT}	Power supply for I/O PLL and I/O pre-driver	—	1.71	1.8	1.89	V
V_{CCR_CORE}	CRAM power supply	—	1.14	1.2	1.26	V
V_{CCH}	Transceiver digital power supply	E-tile and P-tile devices	0.87	0.9	0.93	V
V_{CCH_SDM}	SDM block transceiver digital power sense	E-tile and P-tile devices	0.87	0.9	0.93	V
$V_{CCIO\_PIO\_SDM}$ (8)	SDM block I/O bank power sense of Bank 3A	1.5 V	1.455	1.5	1.545	V
		1.2 V	1.14	1.2	1.26	V

continued...

(5) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(6) The use of Power Management Bus (PMBus*™) voltage regulator dedicated to Intel Agilex SmartVID devices is mandatory. The PMBus voltage regulator and Intel Agilex SmartVID devices are connected via PMBus.

(7) The typical value is based on the SmartVID programmed value.

(8) Must be powered up with the same voltage level as $V_{CCIO\_PIO\_3A}$. Must be supplied at 1.2 V when using Avalon®-ST ×16/×32 configuration schemes.

Symbol	Description	Condition	Minimum[5]	Typical	Maximum[5]	Unit
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
V_{CCL_SDM}	SDM block core voltage power supply	—	0.776	0.8	0.824	V
$V_{CCFUSEWR\_SDM}$	SDM block fuse writing power supply	—	1.75	1.8	1.85	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	0.776	0.8	0.824	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
V_{CCBAT} [9]	Battery back-up power supply (For design security volatile key register)	—	1	—	1.8	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	I/O bank power supply	1.5 V	1.455	1.5	1.545	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA_PLL}	I/O clock network power supply	—	1.14	1.2	1.26	V
V_I [10]	DC input voltage	V_{CCIO_PIO} = 1.2 V	–0.3	—	V_{CCIO_PIO} + 0.3	V
		V_{CCIO_PIO} = 1.5 V	0	—	1.7	V

continued...

(5) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(9) You need to always power up V_{CCBAT}. If you do not use the design security feature in Intel Agilex devices, connect V_{CCBAT} to a 1.8 V power supply. Intel Agilex power-on reset (POR) circuitry monitors V_{CCBAT}.

(10) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

Symbol	Description	Condition	Minimum(5)	Typical	Maximum(5)	Unit
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V	–0.3	—	V_{CCIO_SDM} + 0.3, V_{CCIO_HPS} + 0.3	V
V_O	Output voltage	—	0	—	V_{CCIO_PIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40(11)	—	100	°C
t_{RAMP} (12) (13)	Power supply ramp time	Standard POR	250 µs	—	100 ms	—

(5) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(11) E-tile supports an operating temperature range of –40°C to 100°C. However, the E-tile transceivers may experience a higher error rate from –40°C to –20°C because of the calibration procedure when starting at a low temperature. Therefore, the recommended operating temperature range for E-tile protocol-compliant transceiver links is –20°C to 100°C. The maximum temperature ramp rate is 2°C per minute.

(12) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(13) To support AS fast mode, all power supplies to the Intel Agilex device must be fully ramped-up within 10 ms to the recommended operating conditions.

Transceiver Power Supply Operating Conditions

Table 7. E-Tile Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
V_{CCRT_GXE} (14)	Transceiver power supply	0.9	± 0.5%	± 2.5%		± 3%	V
$V_{CC\_HSSI\_GXE}$	E-tile digital signal power supply	0.9	± 0.5%	± 2.5%		± 3%	V
$V_{CCRTPLL\_GXE}$ (14)	Transceiver PLL power supply	0.9	± 0.5%	± 2.5%		± 3%	V
V_{CCH_GXE}	Analog power supply	1.1	± 0.5%	± 0.5%	± 2%	± 3%	V
V_{CCCLK_GXE}	LVPECL REFCLK power supply	2.5	± 0.5%	± 0.5%	± 3.5%	± 5%	V

Table 8. P-Tile Transceiver Power Supply Operating Conditions

The specifications below should be met at the board vias directly connected to the package power balls. Place the VR sense point in the FPGA pinfield (in the package shadow), as close as possible to the corresponding package power balls. For these rails, measure the output voltage at this remote sense location.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
V_{CCRT_GXP}	Transceiver power supply	0.9	± 0.5%	± 2.5%		± 3%	V
$V_{CC\_HSSI\_GXP}$	P-tile digital signal power supply	0.9	± 0.5%	± 2.5%		± 3%	V

continued...

(14) The difference between V_{CCRT}/$V_{CCRTPLL}$ and V_{CCH} should be no less than 200 mV.

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
V_{CCFUSE_GXP}	P-tile efuse power supply	0.9	± 0.5%	± 2.5%		± 3%	V
V_{CCCLK_GXP}	P-tile I/O buffer power supply	1.8	± 0.5%	± 0.5%	± 2%	± 3%	V
V_{CCH_GXP}	High voltage power for Transceiver	1.8	± 0.5%	± 0.5%	± 2%	± 3%	V

HPS Power Supply Operating Conditions

Table 9. HPS Power Supply Operating Conditions for Intel Agilex Devices

This table lists the steady-state voltage and current values expected for Intel Agilex system-on-a-chip (SoC) devices with ARM-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions for Intel Agilex Devices* table for the steady-state voltage values expected from the FPGA portion of the Intel Agilex SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	Performance boost, fixed voltage: –1V	0.87	0.9	0.93	V
		SmartVID: –1V, –2V, –3V, –3E	(Typical) – 3%	0.685 – 0.85	(Typical) + 3%	V
		Fixed voltage: –4F	0.776	0.8	0.824	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply (can be connected to V_{CCL_HPS})	Performance boost, fixed voltage: –1V	0.87	0.9	0.93	V
		SmartVID: –1V, –2V, –3V, –3E	(Typical) – 3%	0.685 – 0.85	(Typical) + 3%	V
		Fixed voltage: –4F	0.776	0.8	0.824	V
V_{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 10
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 47

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Intel FPGA Power and Thermal Calculator and the Intel Quartus® Prime Power Analyzer feature.

Use the Intel FPGA Power and Thermal Calculator before you start your design to estimate the supply current for your design. The Intel FPGA Power and Thermal Calculator provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

I/O Pin Leakage Current

Table 10. I/O Pin Leakage Current for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–250	250	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–250	250	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC* standard.

Table 11. Bus Hold Parameters for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	V_{CCIO_PIO} (V)		Unit
			1.2		
			Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	30	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–30	—	µA
Bus-hold, low, overdrive current	I_{ODL}	$0 V < V_{IN} < V_{CCIO\_PIO}$	—	1,200	µA
Bus-hold, high, overdrive current	I_{ODH}	$0 V < V_{IN} < V_{CCIO\_PIO}$	—	–1,200	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 12. OCT Calibration Accuracy Specifications for Intel Agilex Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

These specifications require RZQ reference accuracy of 240 Ω ±1%.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO_PIO} = 1.2	±15	%
50-Ω and 60-Ω R_T	Internal parallel termination with calibration (50-Ω and 60-Ω setting)	SSTL-12 and HSTL-12 I/O standards	–10 to +60	%
		POD12 I/O standard	±15	

OCT Without Calibration Resistance Tolerance Specifications

Table 13. OCT Without Calibration Resistance Tolerance Specifications for Intel Agilex Devices

This table lists the Intel Agilex OCT without calibration resistance tolerance to PVT changes.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO_PIO} = 1.2	–30 to +60	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO_PIO} = 1.5	±40	%

Pin Capacitance

Table 14. Pin Capacitance for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	2.5(15)	pF

Internal Weak Pull-Up Resistor

All I/O pins, except configuration and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 15. Internal Weak Pull-Up Resistor Values for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you	V_{CCIO_PIO} = 1.2 ±5%	3	10	30	kΩ

(15) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	have enabled the programmable pull-up resistor option.					

Related Information

Intel Agilex Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Agilex devices.

For minimum voltage values, use the minimum V_{CCIO_PIO} values. For maximum voltage values, use the maximum V_{CCIO_PIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 10

Single-Ended I/O Standards Specifications

Table 16. Single-Ended I/O Standards Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)	
	Min	Typ	Max	Min	Max	Min	Max
1.2 V LVCMOS (16)	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.3

Related Information

1.2 V I/O Interface Voltage Level Compatibility section, Intel Agilex General Purpose I/O and LVDS SERDES User Guide
Provides output voltage swing calculation examples.

(16) Refer to *Intel Agilex General Purpose I/O and LVDS SERDES User Guide* for output voltage swing calculation example.

Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications

Table 17. Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.475 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.525 × V_{CCIO_PIO}
HSTL-12	1.14	1.2	1.26	0.47 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.53 × V_{CCIO_PIO}	0.475 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.525 × V_{CCIO_PIO}
HSUL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	—	—	—
POD12	1.14	1.2	1.26	—	Internally calibrated	—	—	V_{CCIO_PIO}	—

Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

Table 18. Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

I/O Standard	$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Max	Min	Max	Min
SSTL-12	V_{REF} – 0.075	V_{REF} + 0.075	V_{REF} – 0.100	V_{REF} + 0.100
HSTL-12	V_{REF} – 0.080	V_{REF} + 0.080	V_{REF} – 0.150	V_{REF} + 0.150
HSUL-12	V_{REF} – 0.100	V_{REF} + 0.100	V_{REF} – 0.135	V_{REF} + 0.135
POD12[17]	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For output voltage swing calculation example, refer to the *Intel Agilex General Purpose I/O and LVDS SERDES User Guide*.

(17) This specification is defined over internal V_{ref} range from 0.6 × V_{CCIO_PIO} to 0.92 × V_{CCIO_PIO}.

Related Information

1.2 V I/O Interface Voltage Level Compatibility section, Intel Agilex General Purpose I/O and LVDS SERDES User Guide
Provides output voltage swing calculation examples.

Differential SSTL, HSTL, and HSUL I/O Standards Specifications

Table 19. Differential SSTL, HSTL, and HSUL I/O Standards Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (V)			$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Max	Min	Max	Min	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	–0.15	0.15	–0.2	0.2	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSTL-12	1.14	1.2	1.26	–0.16	0.16	–0.3	0.3	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSUL-12	1.14	1.2	1.26	–0.2	0.2	–0.27	0.27	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12

Differential POD I/O Standards Specifications

Table 20. Differential POD I/O Standards Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)[18]
	Min	Typ	Max	Max	Min	Max	Min	Max
POD12	1.14	1.2	1.26	–0.11	0.11	–0.14	0.14	25

(18) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

Differential I/O Standards Specifications

Table 21. Differential I/O Standards Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)[19]		$V_{ICM(DC)}$ (V)			V_{OD} (V)[20] [21]			V_{OCM} (V)[20]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling (Transmitter & Receiver)[22]	1.455	1.5	1.545	100	600	0.3	Data rate ≤700 Mbps	1.4	0.247	—	0.454	0.99	1.1	1.21
						0.9	Data rate >700 Mbps	1.4						
True Differential Signaling (Receiver only)[22]	1.14	1.2	1.26	100	600	0.3	Data rate ≤700 Mbps	1.1	—	—	—	—	—	—
						0.9	Data rate >700 Mbps	1.1						

Switching Characteristics

This section provides the performance characteristics of Intel Agilex core and periphery blocks.

(19) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(20) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(21) The specification is only applicable to default V_{OD} setting.

(22) The True Differential Signaling input buffer is supported on 1.2V and 1.5V V_{CCIO_PIO} bank. The maximum input voltage driven into the True Differential Signaling input buffer must not exceed $V_{ICM(max)} + V_{ID(max)}/2$.

Core Performance Specifications

Clock Tree Specifications

Table 22. Clock Tree Performance for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Parameter	Performance			Unit
	–1V	–2V	–3V, –3E, –4F	
Programmable clock routing	1,100	1,000	780	MHz

I/O PLL Specifications

Table 23. I/O PLL Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1V	10	—	1,100(23)	MHz
		–2V	10	—	900(23)	MHz
		–3V, –3E, –4F	10	—	750(23)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	I/O PLL VCO operating range	–1V	600	—	1,600	MHz
		–2V	600	—	1,434	MHz
		–3V, –3E, –4F	600	—	1,250	MHz
f_{CLBW}	I/O PLL closed-loop bandwidth	I/O bank I/O PLL	0.5	—	10	MHz
		Fabric-feeding I/O PLL	1	—	10	MHz

continued...

(23) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock (C counter)	–1V	—	—	1,100	MHz
		–2V	—	—	900	MHz
		–3V, –3E, –4F	—	—	750	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1V	—	—	800	MHz
		–2V	—	—	720	MHz
		–3V, –3E, –4F	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP} (24)	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for mgmt_clk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps

continued...

(24) Not applicable for fabric-feeding I/O PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{REFPJ}	Reference phase jitter (rms)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise(25)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 KHz	—	—	–110	dBc/Hz
		10 KHz	—	—	–120	dBc/Hz
		100 KHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz
		10 MHz	—	—	–142	dBc/Hz
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (24)	Period jitter for dedicated clock output	f_{REF} < 100 MHz (26)	—	—	17.5	mUI (p-p)
		f_{REF} ≥ 100 MHz (26)	—	—	175	ps (p-p)
t_{OUTCCJ_DC} (24)	Cycle-to-cycle jitter for dedicated clock output	f_{REF} < 100 MHz (26)	—	—	17.5	mUI (p-p)
		f_{REF} ≥ 100 MHz (26)	—	—	175	ps (p-p)
t_{OUTPJ_IO} (27)	Period jitter for clock output on the regular I/O	f_{REF} < 100 MHz (26)	—	—	60	mUI (p-p)
		f_{REF} ≥ 100 MHz (26)	—	—	600	ps (p-p)

continued...

(25) The phase noise numbers in the table above are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 100 MHz + (20 × log10 (f/100))

(26) f_{REF} is f_{IN}/N, specification applies when N = 1.

(27) External memory interface clock output jitter specifications use a different measurement method, which are available in *Memory Output Clock Jitter Specifications for Intel Agilex Devices* table.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTCCJ_IO} (27)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{REF} < 100 MHz (26)	—	—	60	mUI (p-p)
		f_{REF} ≥ 100 MHz (26)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (24)	Period jitter for dedicated clock output in cascaded PLLs	f_{REF} < 100 MHz (26)	—	—	17.5	mUI (p-p)
		f_{REF} ≥ 100 MHz (26)	—	—	175	ps (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 39
Provides more information about the external memory interface clock output jitter specifications.

DSP Block Specifications

Table 24. DSP Block Performance Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Mode	Performance				Unit
	–1V	–2V	–3V, –3E	–4F	
Fixed-point 18 × 19 multiplication mode	900	771	676	600	MHz
Fixed-point 27 × 27 multiplication mode(28)	900	771	676	600	MHz
Fixed-point 18 × 19 multiplier adder mode(28)	900	771	676	600	MHz

continued...

(28) When Chainout is enabled but systolic registers are not used, the performance specifications for the following speed grades are as follows:

- –1V: 675 MHz
- –2V: 578 MHz
- –3V and –3E: 507 MHz
- –4F: 450 MHz

Mode	Performance				Unit
	–1V	–2V	–3V, –3E	–4F	
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	900	771	676	600	MHz
Fixed-point 18 × 19 systolic mode	900	771	676	600	MHz
Fixed-point 18 × 19 complex multiplication mode	900	771	676	600	MHz
Fixed-point four 9 × 9 multiplier adder mode(28)	900	771	676	600	MHz
FP32 floating-point multiplication mode	750	579	507	475	MHz
FP32 floating-point adder or subtract mode	750	579	507	475	MHz
FP32 floating-point multiplier adder or subtract mode	750	579	507	475	MHz
FP32 floating-point multiplier accumulate mode	750	579	507	475	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	750	579	507	475	MHz
FP32 floating-point complex multiplication	750	579	507	475	MHz
FP32 floating-point direct vector dot product	750	579	507	475	MHz
FP16 floating-point complex multiplication	750	579	507	475	MHz
FP16 floating-point direct vector dot product	750	579	507	475	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 25. Memory Block Performance Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance				Unit
		–1V	–2V	–3V, –3E	–4F	
MLAB	Single-port RAM/ROM Simple dual-port RAM	1,000	782	667	600	MHz
	Simple dual-port RAM with read-during-write option	630	510	460	330	MHz
M20K Block[29]	Single-port RAM/ROM Simple dual-port RAM	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	600 (HS) 510 (LP)	MHz
	Simple dual-port RAM, coherent read enabled	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	600 (HS) 510 (LP)	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	800 (HS) 680 (LP)	640 (HS) 540 (LP)	560 (HS) 476 (LP)	480 (HS) 410 (LP)	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	600 (HS) 500 (LP)	480 (HS) 400 (LP)	420 (HS) 357 (LP)	360 (HS) 300 (LP)	MHz

continued...

(29) For M20K block, timing/power optimization feature is available. The available options are High Speed (HS) and Low Power (LP). For details on this timing/power optimization feature, refer to the *Agilex Embedded Memory User Guide*.

Memory	Mode	Performance				Unit
		–1V	–2V	–3V, –3E	–4F	
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	600 (HS) 510 (LP)	MHz
	Dual-port ROM True dual-port RAM	600 (HS)	500 (HS)	420 (HS)	360 (HS)	MHz
	Simple quad-port RAM	600 (HS)	480 (HS)	420 (HS)	360 (HS)	MHz
eSRAM	Simple dual-port	750	640	500	500	MHz

Local Temperature Sensor Specifications

Table 26. Local Temperature Sensor Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Description	Temperature Range	Accuracy	Sampling Rate	Conversion Time
Local Temperature Sensor	–40 to 125 °C(30)	±5 °C	1 KSPS	< 1 ms

Remote Temperature Diode Specifications

Note the following for the remote temperature diode specifications:

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

(30) Temperature range refers to junction temperature.

Table 27. Remote Temperature Diode Specifications for Intel Agilex Devices (Core Fabric TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	170	µA
V_{bias}, voltage across diode	0.43	—	0.75	V
Series resistance	—	—	<3	Ω
Diode ideality factor	—	1.006(31)	—	—

Table 28. Remote Temperature Diode Specifications for Intel Agilex Devices (E-Tile TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	100	—	170	µA
V_{bias}, voltage across diode	0.56	—	0.8	V
Series resistance	—	—	< 2	Ω
Diode ideality factor	—	1.008	—	—

Table 29. Remote Temperature Diode Specifications for Intel Agilex Devices (P-Tile TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	170	µA
V_{bias}, voltage across diode	0.56	—	0.87	V
Series resistance	—	—	<10	Ω
Diode ideality factor	—	1.0108(32)	—	—

(31) When using lower injection current (two-currents) implementation, the ideality factor is 1.009.

(32) When using lower injection current (two-currents) implementation, the ideality factor is 1.03.

Voltage Sensor Specifications

Table 30. Voltage Sensor Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	7	—	Bit
Sampling rate		—	—	1	KSPS
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Input capacitance		—	—	40	pF
Voltage sensor accuracy, V_{in} range: 0 V to 1.249 V		—	—	3.5	%
Unipolar Input Mode	Input signal range for Vsigp	—	—	1.49	V
	Common mode voltage on Vsign	—	—	0.25	V
	Input signal range for Vsigp – Vsign	—	—	1.24	V

Periphery Performance Specifications

This section describes the periphery performance, LVDS SERDES, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

LVDS SERDES Specifications

Table 31. LVDS SERDES Specifications for Intel Agilex Devices

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 3 to 10.

DDR registers support SERDES factor J = 1 to 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40(33)	10	—	800	10	—	700	10	—	625	10	—	625	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40(33)	10	—	625	10	—	625	10	—	525	10	—	525	MHz

continued...

(33) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	f_{HSCLK_OUT} (output clock frequency)	—	—	—	800[34]	—	—	700[34]	—	—	625[34]	—	—	625[34]	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)[35]	SERDES factor J = 4 to 10[36] [37] [38]	150	—	1,600	150	—	1,434	150	—	1,250	150	—	1,000	Mbps
		SERDES factor J = 3[36] [37] [38]	150	—	1,200	150	—	1,076	150	—	938	150	—	600	Mbps
		SERDES factor J = 2, uses DDR registers	150	—	840[39]	150	—	[39]	150	—	[39]	150	—	[39]	Mbps

continued...

[34] This is achieved by using the PHY clock network.

[35] Requires package skew compensation with PCB trace length.

[36] The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

[37] The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

[38] The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

[39] The maximum ideal data rate is the SERDES factor (J) × the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 1, uses DDR registers	150	—	420(39)	150	—	(39)	150	—	(39)	150	—	(39)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	160	—	—	200	—	—	250	—	—	350	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	—	—	0.21	UI
	t_{DUTY} (40)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	t_{RISE} & t_{FALL} (37) (41)	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	—	—	220	ps

continued...

(40) Not applicable for DIVCLK = 1.

(41) This applies to default pre-emphasis and V_{OD} settings only.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	T_{CCS} (35) (40)	True Differential I/O Standards	—	—	330	—	—	330	—	—	330	—	—	330	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10(36) (37) (38)	150	—	1,600	150	—	1,434	150	—	1,250	150	—	1,000	Mbps
		SERDES factor J = 3(36) (37) (38)	150	—	1,200	150	—	1,076	150	—	938	150	—	600	Mbps
	f_{HSDR} (data rate) (without DPA)(35)	SERDES factor J = 3 to 10	(38)	—	(42)	(38)	—	(42)	(38)	—	(42)	(38)	—	(42)	Mbps
		SERDES factor J = 2, uses DDR registers	(38)	—	(39)	(38)	—	(39)	(38)	—	(39)	(38)	—	(39)	Mbps
		SERDES factor J = 1, uses DDR registers	(38)	—	(39)	(38)	—	(39)	(38)	—	(39)	(38)	—	(39)	Mbps

continued...

(42) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DPA (FIFO mode)	DPA run length	—	—	—	10,000	—	—	10,000	—	—	10,000	—	—	10,000	UI
DPA (soft CDR mode)	DPA run length	SGMII/ GbE protocol	—	—	5	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling Window	—	—	—	330	—	—	330	—	—	330	—	—	330	ps

DPA Lock Time Specifications

Table 32. DPA Lock Time Specifications for Intel Agilex Devices

The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1- to-0 transition.

For specification status, see the *Data Sheet Status* table

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(43)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	768
Parallel Rapid I/O	00001111	2	128	768

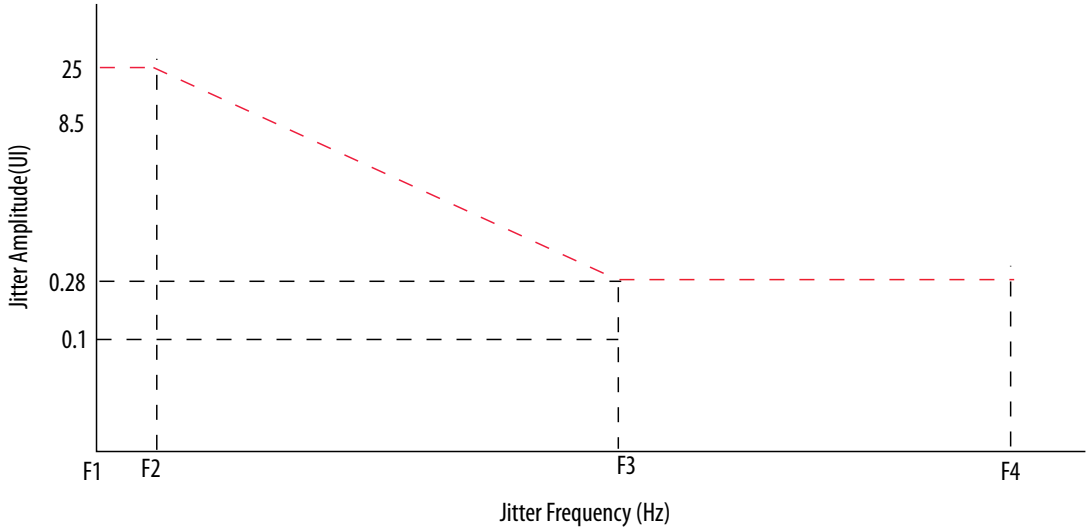
continued...

(43) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(43)	Maximum Data Transition
	10010000	4	64	768
Miscellaneous	10101010	8	32	768
	01010101	8	32	768

LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications

Figure 2. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps



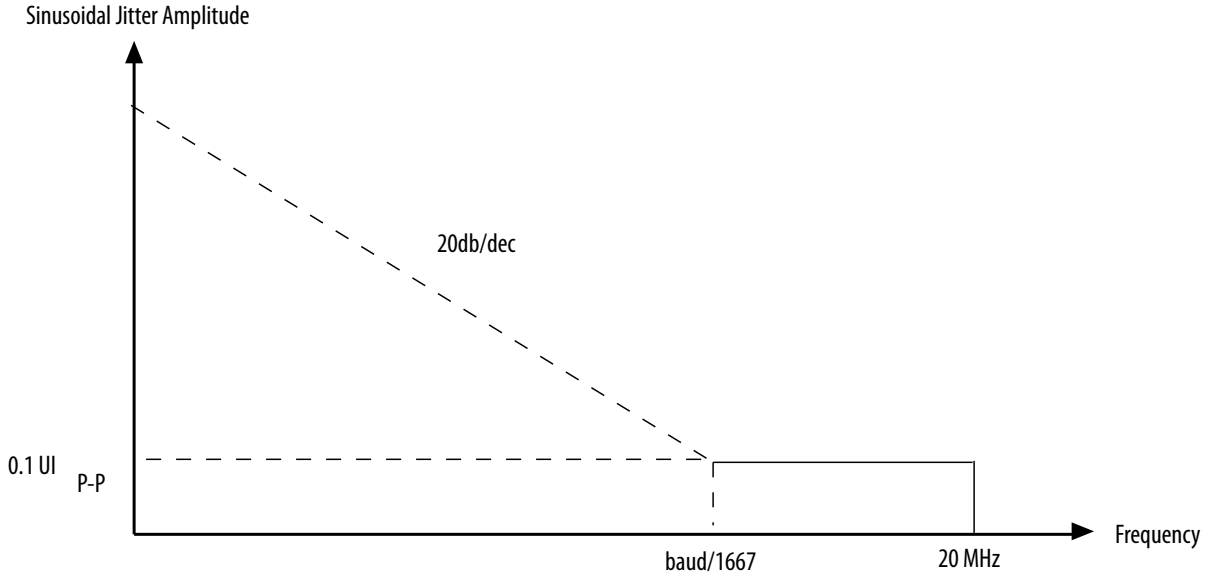
(43) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Table 33. LVDS SERDES Soft-CDR Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps

For specification status, see the *Data Sheet Status* table

Parameter	Jitter Frequency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25
F2	17,565	25
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 3. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 34. Memory Standards Supported by the Hard Memory Controller for Intel Agilex Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	1,600

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

Memory Standards Supported by the Soft Memory Controller

Table 35. Memory Standards Supported by the Soft Memory Controller for Intel Agilex Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3(44)	Quarter rate	1,200
QDR IV SRAM	Quarter rate	1,066

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(44) For Intel Agilex RLDRAM 3, Intel only provides the PHY-only option.

Memory Standards Supported by the HPS Hard Memory Controller

Table 36. Memory Standards Supported by the HPS Hard Memory Controller for Intel Agilex Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	1,600
	Half rate	1,333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 37. DLL Frequency Range Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,600	MHz
DLL reference clock input	Minimum 600	MHz

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC specifications when the phase jitter (integration bandwidth 10 kHz to 50 MHz) of the input clock is not more than 20 ps peak-to-peak, or 1.42 ps RMS at $1e^{-12}$ BER and 1.22 ps at $1e^{-16}$ BER.

E-Tile Transceiver Performance Specifications

This section provides E-tile transceiver specifications and timing for Intel Agilex devices.

E-Tile Transceiver Performance

Table 38. E-Tile Transmitter and Receiver Data Rate Performance Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		-1	-2	-3	
Supported data rate(45)	NRZ	28.9	28.3	17.4	Gbps
	PAM4	57.8(46)	56	32	Gbps

E-Tile Transceiver Reference Clock Specifications

Table 39. E-Tile Reference Clock LVPECL DC Electrical Characteristics

For specification status, see the *Data Sheet Status* table

Symbol	Refclk Parameter	Min	Typ	Max	Unit
V_{TT}	Termination Voltage (2.5 V compliant)	0.4	0.5	0.6	V
V_{TT}	Termination Voltage (3.3 V compliant)	1.04	1.3	1.56	V
R_{TT}	Termination Resistor	40	50	60	Ω
V_{DIFF}	Differential Voltage	0.4	0.8	1.2	V
V_{CM}	Input Common Mode Voltage (2.5 V compliant, no internal termination resistor)	$V_{DIFF}/2$	—	V_{CCCLK_GXE} - $V_{DIFF}/2$	V

continued...

(45) The supported data rate is for chip-to-chip and backplane links.

(46) Two channels are combined to support up to 57.8 Gbps.

Symbol	Refclk Parameter	Min	Typ	Max	Unit
	Input Common Mode Voltage (2.5 V compliant, internal termination resistor)	V_{CCCLK_GXE} - 1.6	V_{CCCLK_GXE} - 1.3	V_{CCCLK_GXE} - 1.0	V
	Input Common Mode Voltage (3.3 V compliant, no internal termination resistor)	$V_{DIFF}/2$	—	V_{CCCLK_GXE} - $V_{DIFF}/2$	V
	Input Common Mode Voltage (3.3 V compliant, internal termination resistor)	1.4	2	2.6	V

Table 40. E-Tile Reference Clock Electrical and Jitter Requirements

For specification status, see the *Data Sheet Status* table

Parameter	Condition	Min	Typ	Max	Unit
Frequency	—	125	156.25	700	MHz
Frequency Tolerance	—	-100	—	100	ppm
Clock Duty Cycle	—	45	50	55	%
Rise/Fall Times	20% to 80%	40	—	300	ps
Phase Jitter	12 kHz to 20 MHz	—	0.375	0.5	ps rms
Phase Noise(47)	10 kHz	—	—	-130	dBc/Hz
	100 kHz	—	—	-138	dBc/Hz
	500 kHz	—	—	-138	dBc/Hz
	3 MHz	—	—	-140	dBc/Hz
	10 MHz	—	—	-144	dBc/Hz
	20 MHz	—	—	-146	dBc/Hz

(47) The phase noise numbers in the table above are the maximum acceptable phase noise values measured at a carrier frequency of 156.25 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + $20*\log_{10}(f/156.25)$.

E-Tile Transmitter Specifications

Table 41. E-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis	—	0.965	—	V
Transmitter common mode voltage	—		$V_{CCRT\_GXE}/2$		V

E-Tile Receiver Specifications

Table 42. E-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Absolute V_{MAX} for a receiver pin	—		1.2		V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before/after device configuration	—		1.2		V
V_{ICM} (AC coupled)(48)	—		V_{CCRT_GXE}		V
Receiver run length(49)	—	—	—	100(50)	symbols
DC input impedance	—	40	—	60	Ω
DC differential input impedance	—	80	100	120	Ω

continued...

(48) This value uses internal AC coupling. External coupling capacitors are required beyond the V_{CCRT_GXE}.

(49) No additional transition density requirements apply.

(50) The incoming data must be statistically DC-balanced.

Symbol/Description	Condition	Min	Typ	Max	Unit
Powered down DC input impedance	Receiver pin impedance when the receiver termination is powered down	100k	—	—	Ω
Differential termination	From DC to 100 MHz	80	100	120	Ω
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data	—	—	750	ppm

P-Tile Transceiver Performance Specifications

This section provides P-tile transceiver specifications and timing for Intel Agilex devices.

P-Tile Transceiver Performance

Table 43. P-Tile Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Gen 1	Gen 2	Gen 3	Gen 4	Unit
Supported data rate	PCIe*	2.5	5	8	16	Gbps

Table 44. P-Tile PLLA Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		Min	Typ	Max	
VCO frequency	—	—	5	—	GHz
PLL bandwidth (BWTX-PKG_PLL1)	PCIe 2.5 GT/s	1.5	—	22	MHz
PLL peaking (PKGTX-PLL1)	PCIe 2.5 GT/s	—	—	3	dB
PLL bandwidth (BWTX-PKG_PLL2)	PCIe 5.0 GT/s	5	—	16	MHz
PLL peaking (PKGTX-PLL2)	PCIe 5.0 GT/s	—	—	1	dB

Table 45. P-Tile PLLB Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		Min	Typ	Max	
VCO frequency	—	—	8	—	GHz
PLL bandwidth (BWTX-PKG_PLL1)	PCIe 8.0 GT/s	2	—	4	MHz
	PCIe 16.0 GT/s	2	—	4	MHz
PLL peaking (PKGTX-PLL1)	PCIe 8.0 GT/s	—	—	2	dB
	PCIe 16.0 GT/s	—	—	2	dB

P-Tile Transceiver Reference Clock Specifications

Table 46. P-Tile Reference Clock Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	—	HCSL			—
Input Reference Clock Frequency(51)	—	99.97	100	100.03	MHz
Rising Edge Rate(52)	—	0.6	—	4	V/ns
Falling Edge Rate(52)	—	0.6	—	4	V/ns
Duty cycle	—	40	—	60	%
Spread-spectrum modulating clock frequency	—	30	—	33	kHz

continued...

(51) This number is with spread spectrum clocking (SSC) turned off.

(52) Measured from -150 mV to +150 mV on the differential waveform. The 300 mV measurement window is centered on the differential zero crossing.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Spread-spectrum downspread	—	—	0 to -0.5	—	%
Absolute V_{MAX}	—	—	1.15	—	V
Absolute V_{MIN}	—	—	-0.3	—	V
Peak-to-peak differential input voltage	—	300	—	1,500	mV
V_{ICM} (DC coupled)	—	250	—	550	mV
Cycle to cycle jitter (TCCJITTER)(53)	—	—	—	150	ps
TSSC-MAX-PERIOD-SLEW	—	—	—	1,250	ppm/us

P-Tile Transmitter Specifications

Table 47. P-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	PCIe	High Speed Differential I/O			—
Differential on-chip termination resistors	—	80	—	120	Ω
Differential peak-to-peak voltage for full swing	PCIe 2.5 GT/s	800	—	1,100	mV
	PCIe 5.0 GT/s	800	—	1,100	mV
	PCIe 8.0 GT/s	800	—	1,100	mV

continued...

(53) When using PCI Express*, you must meet the reference clock phase jitter requirements as specified in the PCIE Express Card Electromechanical Specification for 2.5 GT/s, Section 4.3.7 Refclk Specifications for 5.0 GT/s and Section 4.3.8 Refclk Specifications for 8.0 GT/s in the PCI Express Base Specification Revision 3.0, and Section 8.6 Refclk Specifications for 16.0 GT/s in the PCI Express Base Specification Revision 4.0.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
	PCIe 16.0 GT/s	800	—	1,100	mV
Differential peak-to-peak voltage during EIEOS	PCIe 8.0 GT/s and 16.0 GT/s	250	—	—	mV
Lane-to-lane output skew	PCIe 2.5 GT/s	—	—	2.5	ns
	PCIe 5.0 GT/s	—	—	2	ns
	PCIe 8.0 GT/s	—	—	1.5	ns
	PCIe 16.0 GT/s	—	—	1.25	ns

P-Tile Receiver Specifications

Table 48. P-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	PCIe	High Speed Differential I/O			—
Peak-to-peak differential input voltage V_{ID} (diff p-p)	PCIe 2.5 GT/s(54)	175(55)	—	1,200	mV
	PCIe 5.0 GT/s(54)	100(55)	—	1,200	mV
	PCIe 8.0 GT/s	25(55)	—	—(56)	mV
	PCIe 16.0 GT/s	25(55)	—	—(56)	mV

continued...

(54) Voltage shown for PCIe 2.5 GT/s and 5.0 GT/s are at the package pins (TP2).

(55) For PCIe at 2.5 and 5 GT/s, the V_{ID} is measured at TP2, which is the accessible test point at the device under test. For PCIe 8.0 GT/s and 16.0 GT/s, the V_{ID} is measured at TP2P. TP2P defines a reference point that comprehends the effects of the behavioral Rx package plus Rx equalization and represents the only location where a meaningful eye height and eye width limits can be defined.

(56) The maximum eye height value depends on the transmitter launch voltage maximum value. Refer to the PCIe Express Base Specification Rev. 4.0 for the generator (TX) launch voltage value.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
V_{ICM} (AC coupled)	—	—	0	—	V
Differential on-chip termination resistors	—	80	—	120	Ω
RESREF[57]	—	167.3	169	170.7	Ω

HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing for Intel Agilex devices.

HPS Clock Performance

Table 49. Maximum HPS Clock Frequencies for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Performance	VCCL_HPS (V)	MPU Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	MPFE Frequency (MHz)	Rate	DDR Clock (MHz)	DDR (Mb/s per pin)
–1 speed grade	Fixed: 0.9	1,350	400	400	Quarter	1,600	3,200
				667	Half	1,333	2,666
	SmartVID	1,200	400	400	Quarter	1,600	3,200
				667	Half	1,333	2,666
–2 speed grade	SmartVID	1,000	400	334	Quarter	1,333	2,666
				600	Half	1,200	2,400
–3 speed grade	SmartVID	800	400	300	Quarter	1,200	2,400

continued...

(57) Connecting RESREF at 169 Ω calibrates PCIe channel on-chip termination to 85 Ω.

Performance	VCCL_HPS (V)	MPU Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	MPFE Frequency (MHz)	Rate	DDR Clock (MHz)	DDR (Mb/s per pin)
				534	Half	1,067	2,133
–4 speed grade	Fixed: 0.8	800	400	267	Quarter	1,067	2,133
				467	Half	933	1,866

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the maximum allowed SDRAM operating frequency.

HPS Internal Oscillator Frequency

Table 50. HPS Internal Oscillator Frequency for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Internal Oscillator Frequency	160	370	400	MHz

HPS PLL Specifications

Table 51. HPS PLL Input Requirements for Intel Agilex Devices

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the *Intel Agilex Device Family Pin Connection Guidelines* for information about assigning this pin.

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	PPM
Clock input duty cycle	45	50	55	%

Table 52. HPS PLL Performance for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Description	Min	Max	Unit
Main PLL VCO output	—	3,000	MHz
Peripheral PLL VCO output	—	3,000	MHz
h2f_user0_clk[58]	—	500	MHz
h2f_user1_clk[58]	—	500	MHz

Related Information

Intel Agilex Device Family Pin Connection Guidelines
Provides more information about the HPS_OSC_CLK pin assignment.

HPS SPI Timing Characteristics

Table 53. SPI Master Timing Requirements for Intel Agilex Devices

You can adjust the input delay timing by programming the `rx_sample_dly` register.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns

continued...

(58) The HPS PLL provides this clock to the FPGA fabric.

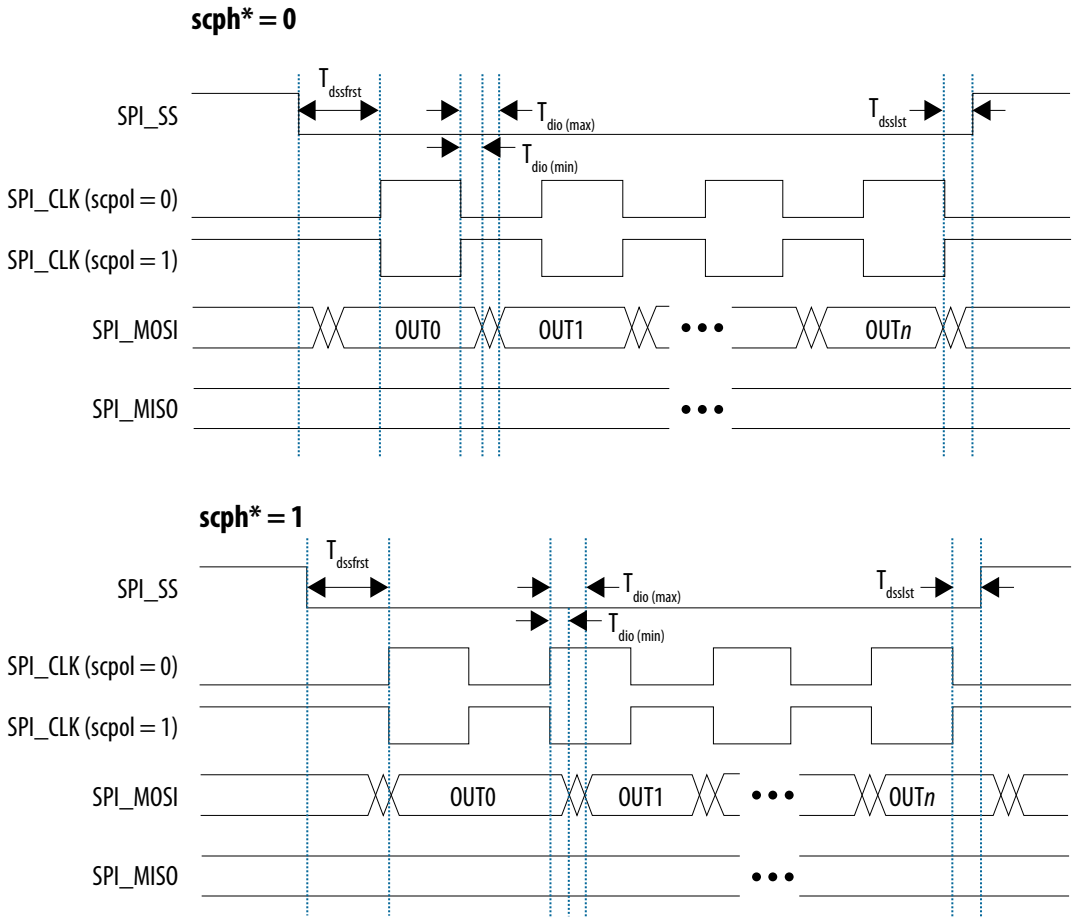
Symbol	Description	Min	Typ	Max	Unit
$T_{dssfrst}$ (59)	SPI_SS_N asserted to first SPIM_CLK edge	(1.5 × T_{clk}) – 2	—	—	ns
T_{dsslst} (59)	Last SPIM_CLK edge to SPI_SS_N deasserted	Tclk – 2	—	—	ns
T_{su} (60)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	4.5 – (`rx_sample_dly` × $T_{spi\_ref\_clk}$)(61)	—	—	ns
T_h (60)	Input hold in respect to SPIM_CLK capture edge	1.3 + (`rx_sample_dly` × $T_{spi\_ref\_clk}$)	—	—	ns

(59) SPI_SS_N behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

(60) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the scpol register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

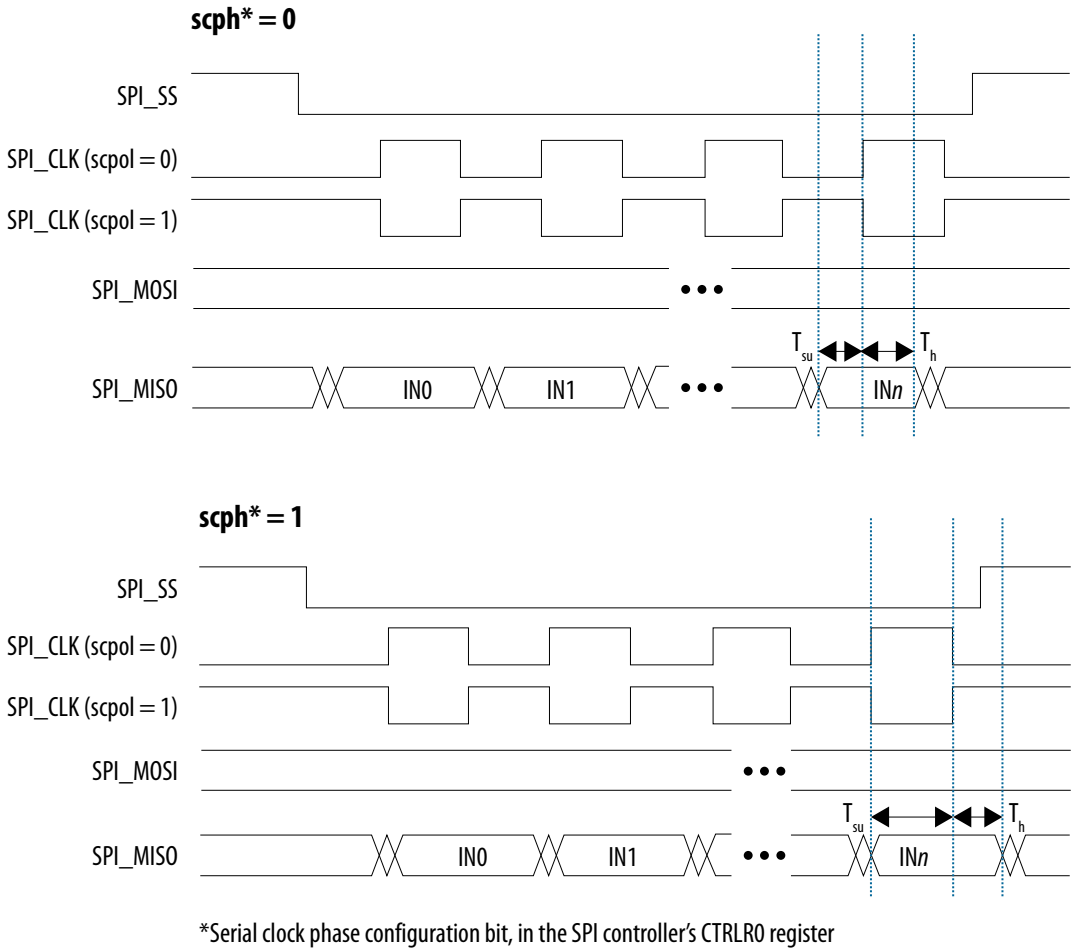
(61) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps)

Figure 4. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 5. SPI Master Input Timing Diagram



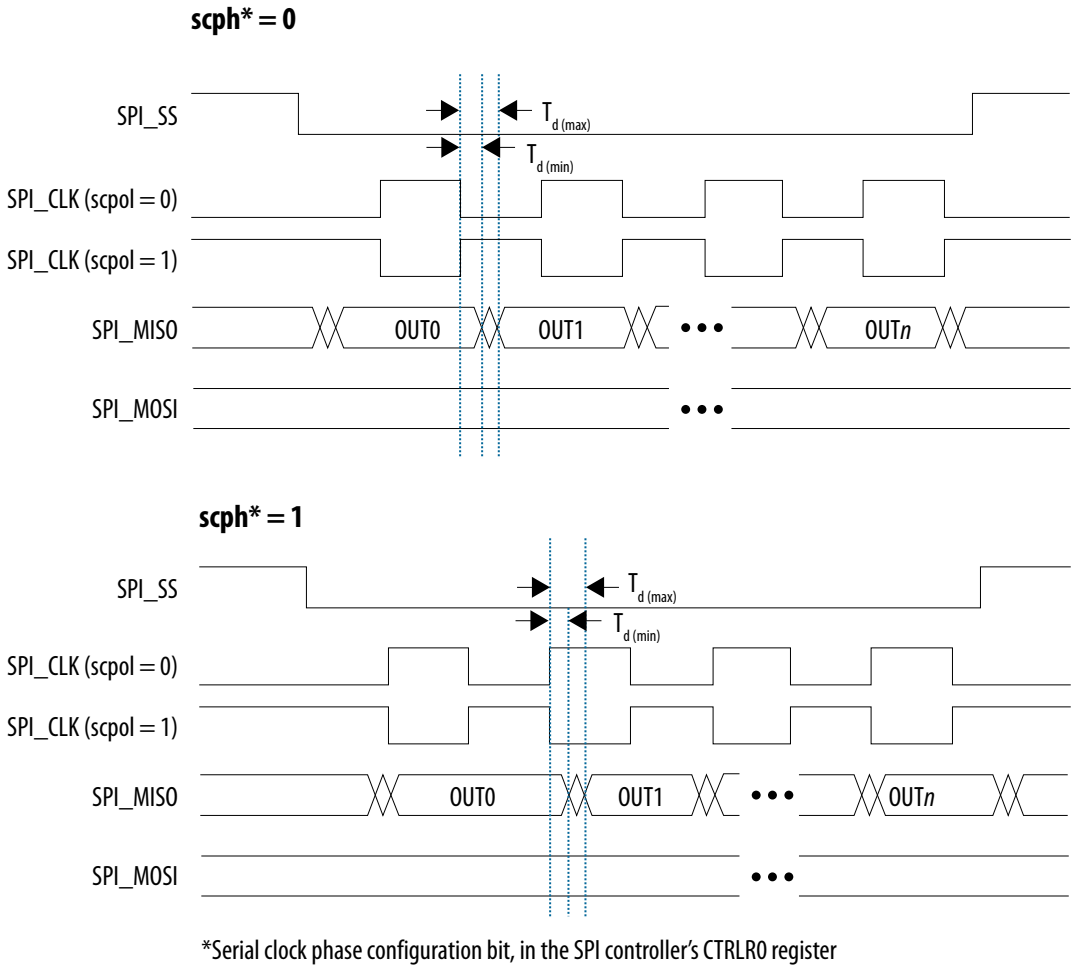
*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 54. SPI Slave Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

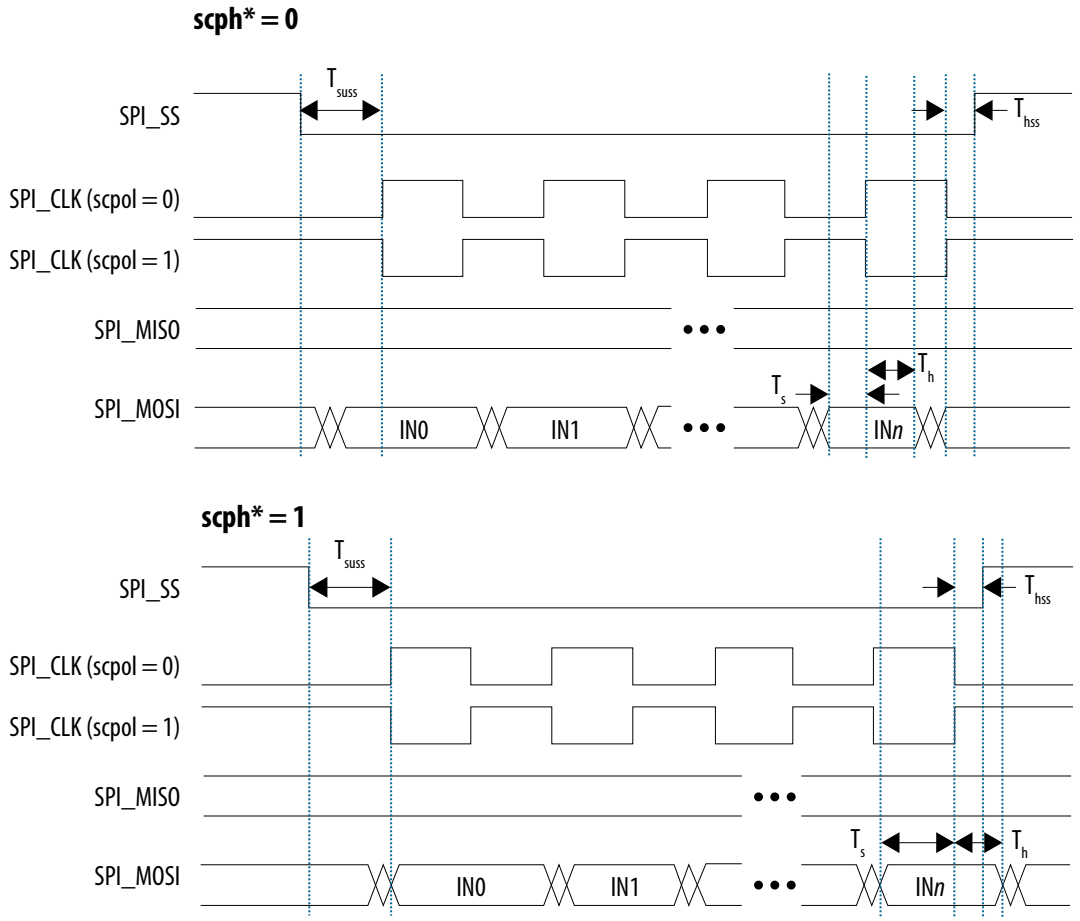
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4$	—	—	ns

Figure 6. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 7. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

HPS SD/MMC Timing Characteristics

Table 55. HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Agilex Devices

These timings apply to SD, MMC, and embedded MMC (eMMC) cards operating at 1.8 V.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{sdmmc_cclk}	SDMMC_CCLK clock period (Identification mode)	2,500	—	—	ns
	SDMMC_CCLK clock period (SDR12)	40	—	—	ns
	SDMMC_CCLK clock period (SDR25)	20	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle	45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter	—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4	5	—	—	ns
T_d	SDMMC_CMD/ SDMMC_DATA[7:0] output delay(62)	T_{sdmmc_clk} × drvsel/2	—	3 + (T_{sdmmc_clk} × drvsel/2)	ns
T_{su}	SDMMC_CMD/ SDMMC_DATA[7:0] input setup(63)	6 – (T_{sdmmc_clk} × smplsel/2)	—	—	ns
T_h	SDMMC_CMD/ SDMMC_DATA[7:0] input hold(63)	0.5 + (T_{sdmmc_clk} × smplsel/2)	—	—	ns

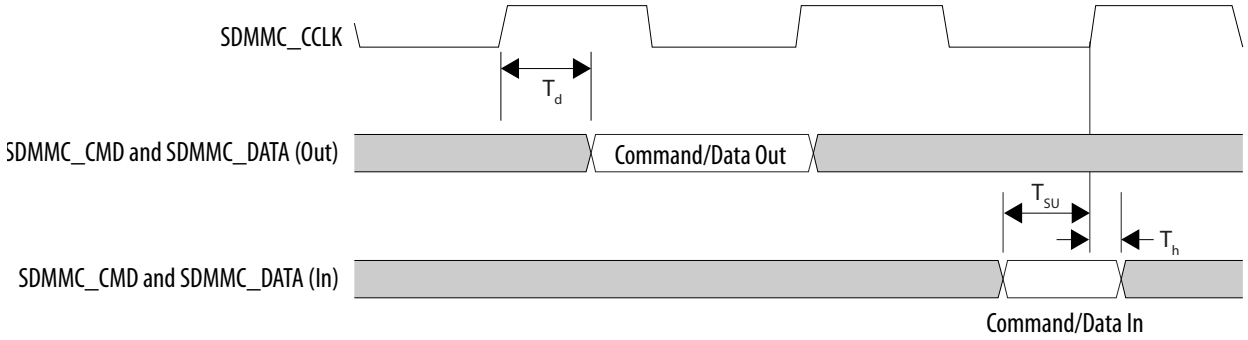
None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

(62) When the drvsel bitfield in the sdmmc register is set to 3 (in the system manager) and the reference clock (sdmmc_clk) is 200 MHz for example, the output delay time is 7.5 to 10.5 ns.

(63) When the smplsel bitfield in the sdmmc register is set to 2 (in the system manager) and the reference clock (sdmmc_clk) is 200 MHz for example, the setup time is 1 ns and the hold time is 5.5 ns.

Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

Figure 8. SD/MMC Timing Diagram



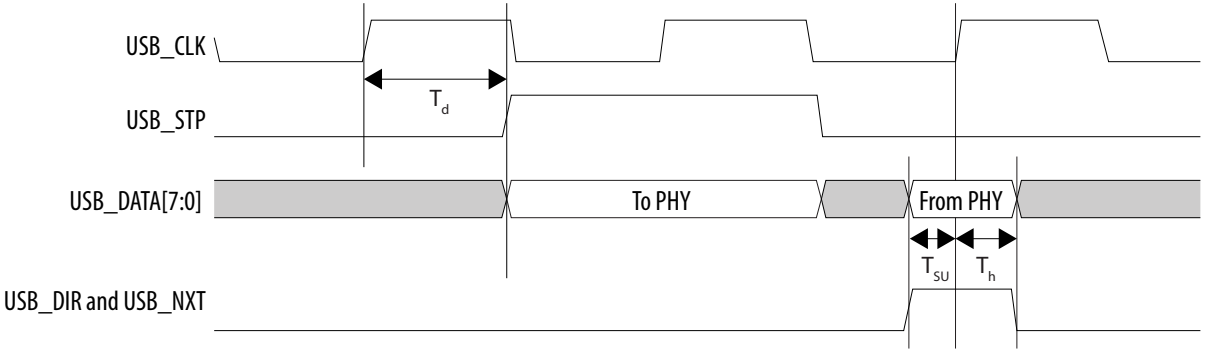
HPS USB UPLI Timing Characteristics

Table 56. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 9. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 57. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (64) (65)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

(64) Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

(65) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5—2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1-ns data-to-clock skew requirement.

Figure 10. RGMII TX Timing Diagram

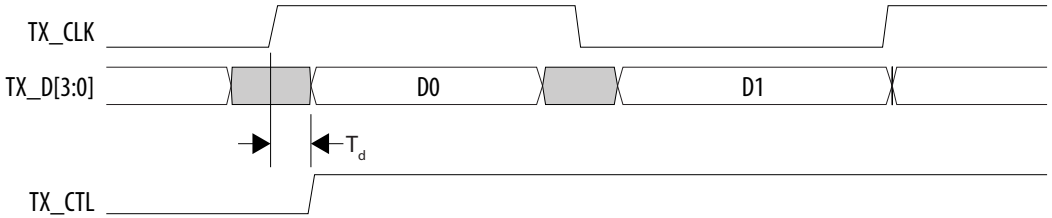


Table 58. RGMII RX Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h (66)	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

(66) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5-2 ns, using the HPS I/O programmable delay.

Figure 11. RGMII RX Timing Diagram

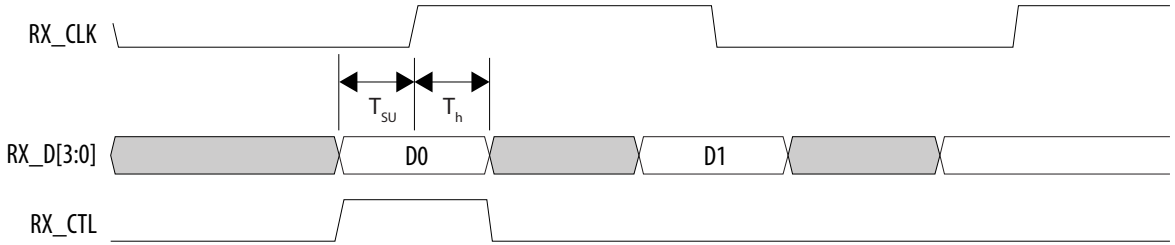


Table 59. Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

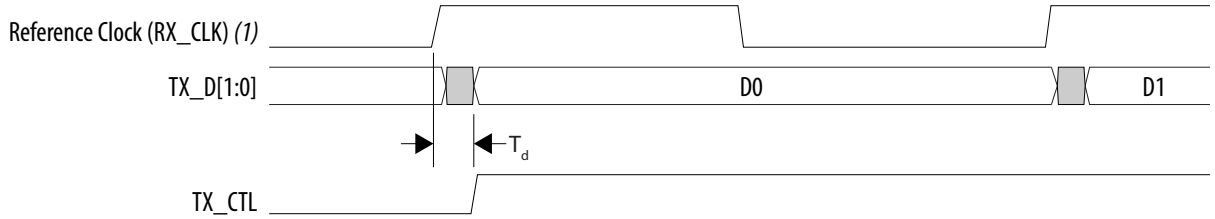
Symbol	Description	Min	Typ	Max	Unit
T_{clk}	REF_CLK clock period, sourced by HPS TX_CLK	—	20	—	ns
	REF_CLK clock period, sourced by external clock source	—	20	—	ns
$T_{dutycycle\_int}$	Clock duty cycle, REF_CLK sourced by TX_CLK	35	50	65	%
$T_{dutycycle\_ext}$	Clock duty cycle, REF_CLK sourced by external clock source	35	50	65	%

Table 60. RMII TX Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_d	TX_CLK to TXD/TX_CTL output data delay	2	—	10	ns

Figure 12. RMII TX Timing Diagram



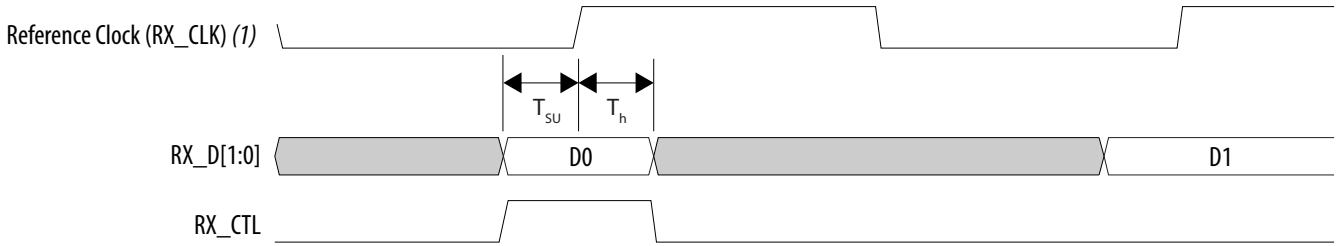
Note:
1. For RMII mode, RX_CLK is always used as the reference clock. Refer to the *HPS-to-PHY Interface Diagram* in the *Intel Agilex Hard Processor System Technical Reference Manual* for example system-level topologies.

Table 61. RMII RX Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{su}	RX_D/RX_CTL setup time	2	—	—	ns
T_h	RX_D/RX_CTL hold time	1	—	—	ns

Figure 13. RMII RX Timing Diagram



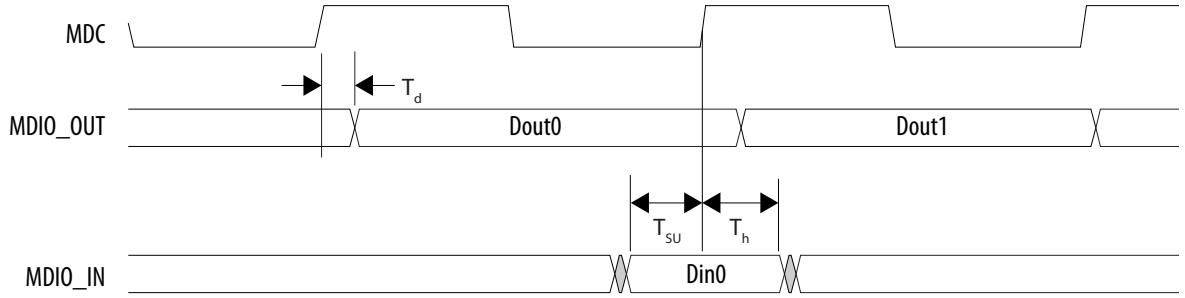
Note:
1. For RMII mode, RX_CLK is always used as the reference clock. Refer to the *HPS-to-PHY Interface Diagram* in the *Intel Agilex Hard Processor System Technical Reference Manual* for example system-level topologies.

Table 62. Management Data Input/Output (MDIO) Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 14. MDIO Timing Diagram



Related Information

HPS-to-PHY Interface Diagrams section, Intel Agilex Hard Processor System Technical Reference Manual
Provides the example system-level topologies.

HPS I²C Timing Characteristics

Table 63. HPS I²C Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I2C clock output jitter	—	2	—	2	%
T_{HIGH} (67)	SCL high period	4(68)	—	0.6(69)	—	µs
T_{LOW} (70)	SCL low period	4.7(71)	—	1.3(72)	—	µs
$T_{SU;DAT}$	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
$T_{HD;DAT}$ (73)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
$T_{VD;DAT}$ and $T_{VD;ACK}$ (74)	SCL to SDA output data delay	—	3.45(75)	—	0.9(76)	µs

continued...

(67) You can adjust T_{high} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(68) The recommended minimum setting for `ic_ss_scl_hcnt` is 440.

(69) The recommended minimum setting for `ic_fs_scl_hcnt` is 71.

(70) You can adjust T_{low} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(71) The recommended minimum setting for `ic_ss_scl_lcnt` is 500.

(72) The recommended minimum setting for `ic_fs_scl_lcnt` is 141.

(73) $T_{HD;DAT}$ is affected by the rise and fall time.

(74) $T_{VD;DAT}$ and $T_{VD;ACK}$ are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

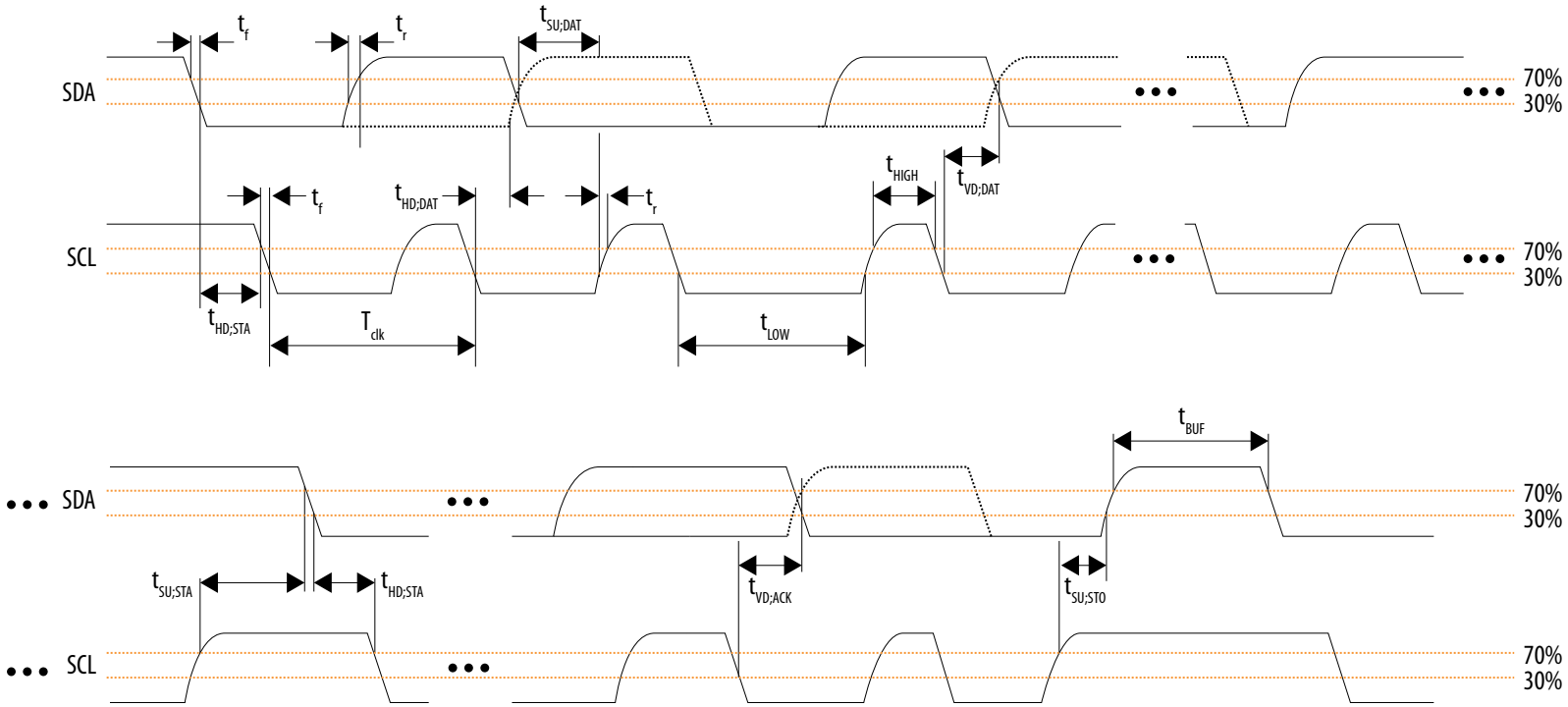
Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
$T_{SU;STA}$	Setup time for a repeated start condition	4.7	—	0.6	—	µs
$T_{HD;STA}$	Hold time for a repeated start condition	4	—	0.6	—	µs
$T_{SU;STO}$	Setup time for a stop condition	4	—	0.6	—	µs
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
$T_{scl:r}$ (77)	SCL rise time	—	1,000	20	300	ns
$T_{scl:f}$ (77)	SCL fall time	—	300	6.54	300	ns
$T_{sda:r}$ (77)	SDA rise time	—	1,000	20	300	ns
$T_{sda:f}$ (77)	SDA fall time	—	300	6.54	300	ns

(75) Use maximum SDA_HOLD = 240 to be within the specification.

(76) Use maximum SDA_HOLD = 60 to be within the specification.

(77) Rise and fall time parameters vary depending on external factors such as the characteristics of the I/O driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 15. I²C Timing Diagram



HPS NAND Timing Characteristics

Table 64. HPS NAND ONFI 1.0 Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{WP} (78)	Write enable pulse width	10	—	ns
T_{WH} (78)	Write enable hold time	7	—	ns
T_{RP} (78)	Read enable pulse width	10	—	ns
T_{REH} (78)	Read enable hold time	7	—	ns
T_{CLS} (78)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (78)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (78)	Chip enable to write enable setup time	15	—	ns
T_{CH} (78)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (78)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (78)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (78)	Data to write enable setup time	7	—	ns
T_{DH} (78)	Data to write enable hold time	5	—	ns
T_{WB} (78)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns

continued...

(78) This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Intel Agilex Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Symbol	Description	Min	Max	Unit
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

Figure 16. NAND Command Latch Timing Diagram

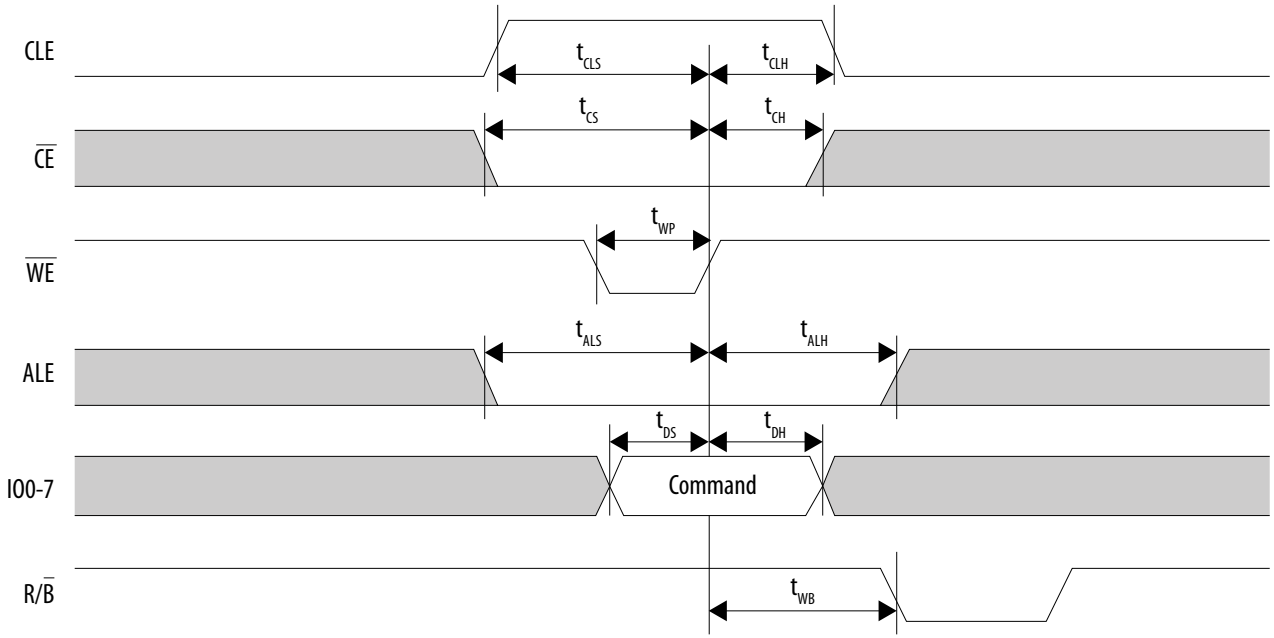


Figure 17. NAND Address Latch Timing Diagram

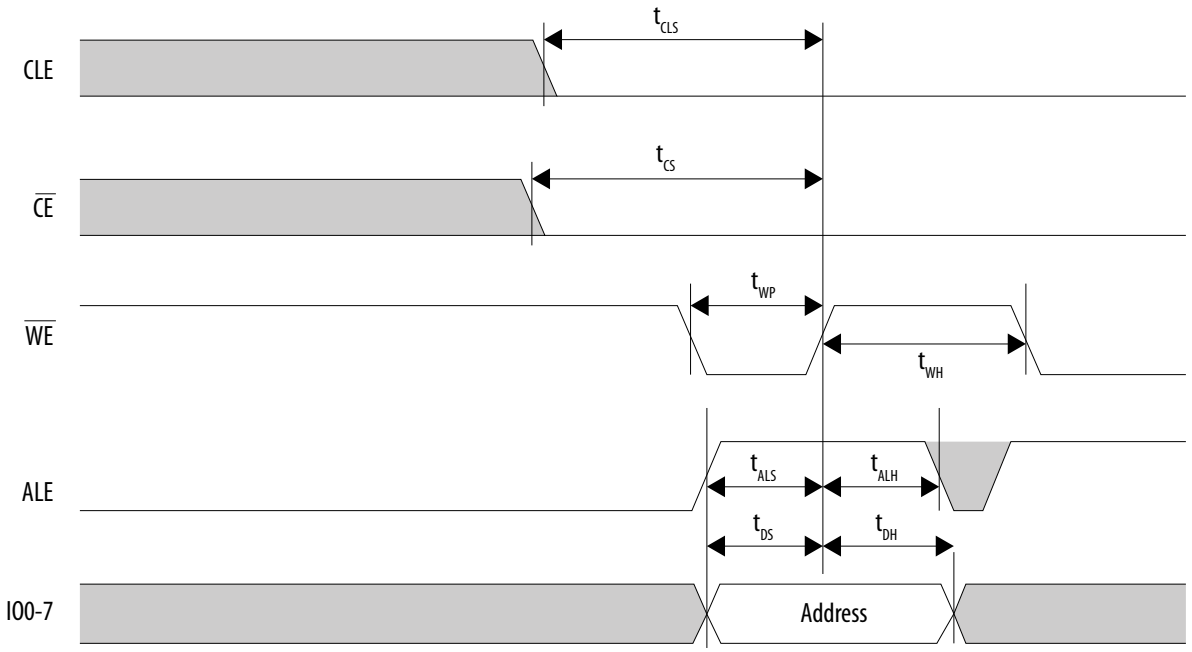


Figure 18. NAND Data Output Cycle Timing Diagram

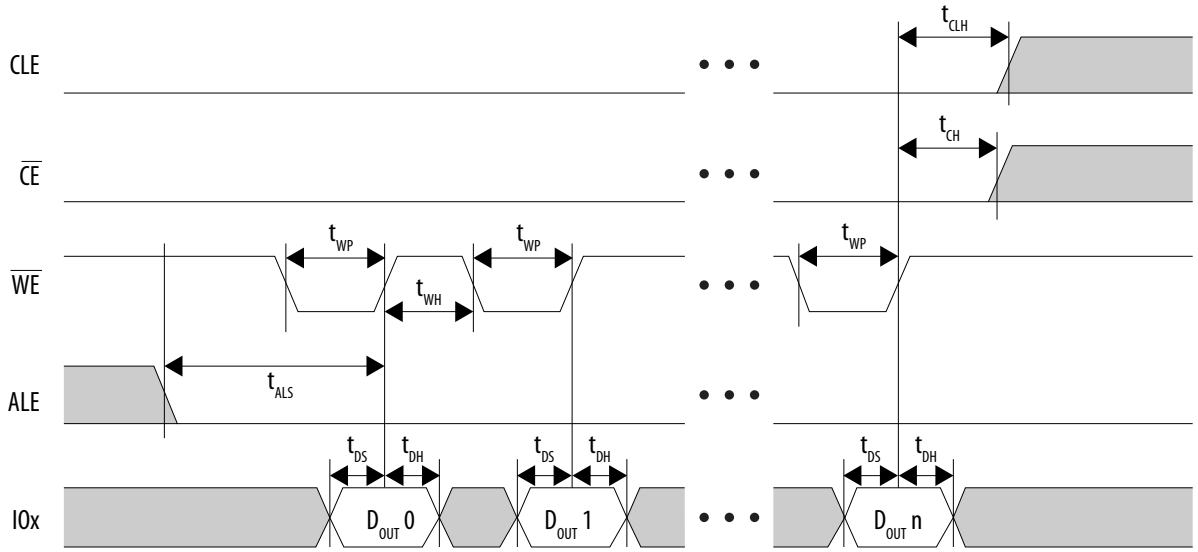


Figure 19. NAND Data Input Cycle Timing Diagram

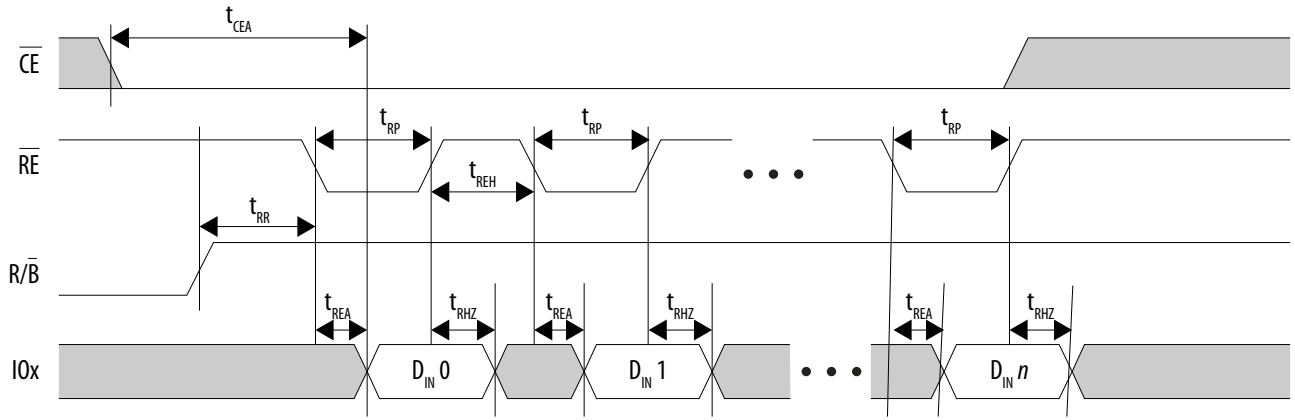


Figure 20. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

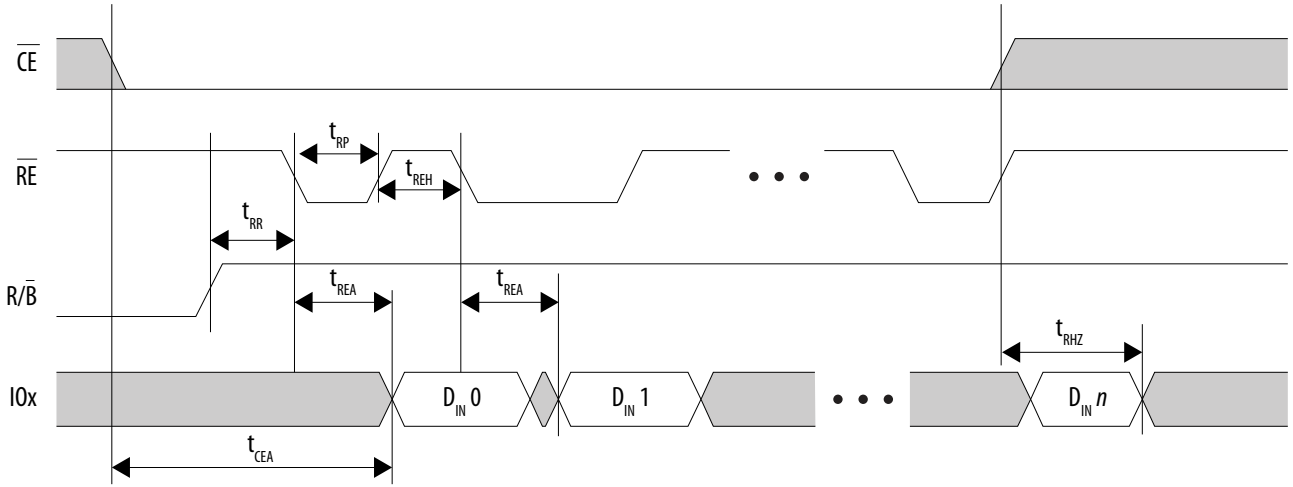


Figure 21. NAND Read Status Timing Diagram

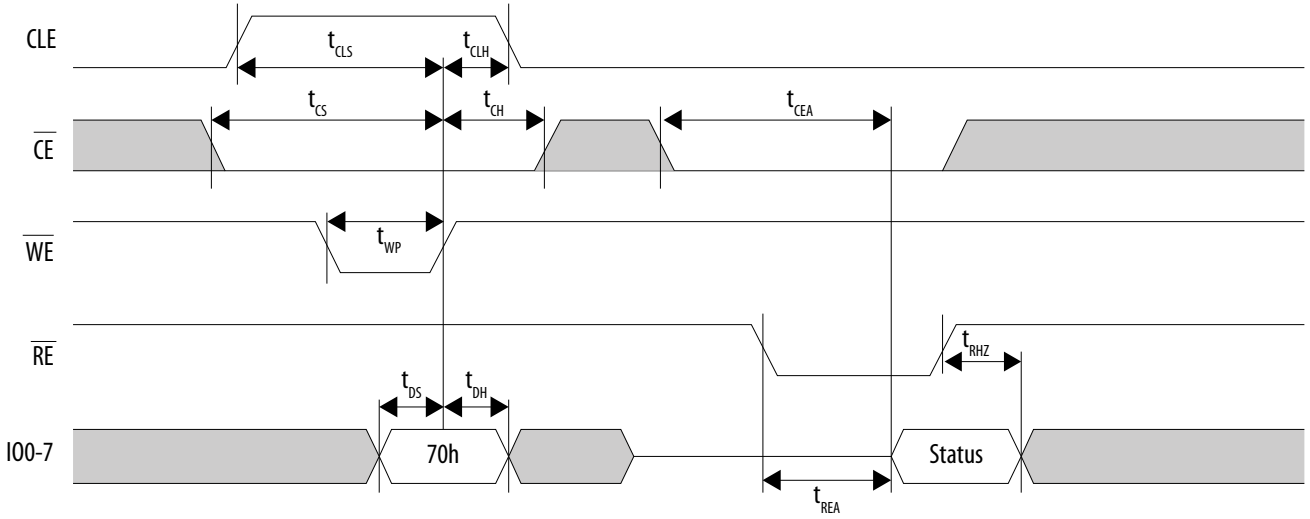
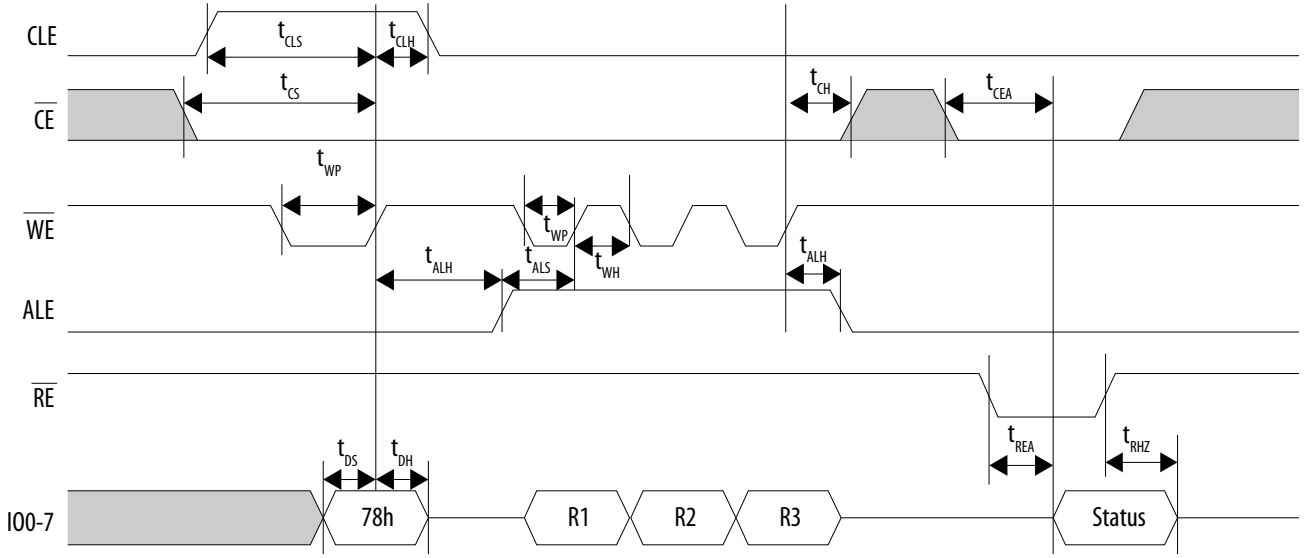


Figure 22. NAND Read Status Enhanced Timing Diagram



HPS Trace Timing Characteristics

Table 65. Trace Timing Requirements for Intel Agilex Devices

To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

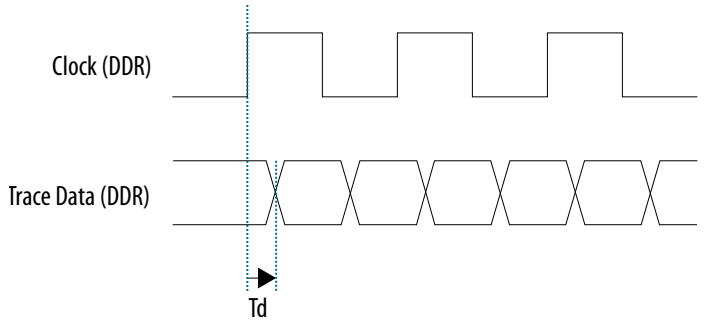
Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module data sheet for termination recommendations.

Most trace modules implement programmable clock and data skew, to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	Trace clock period	6.667	—	—	ns
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	0	—	1.8	ns

Figure 23. Trace Timing Diagram



HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz).

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

HPS JTAG Timing Characteristics

Table 66. HPS JTAG Timing Requirements for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
t_{JCP}	TCK clock period	41.66	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	5	—	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

HPS Programmable I/O Timing Characteristics

Table 67. HPS Programmable I/O Delay (Output Path) for Intel Agilex Device

For specification status, see the *Data Sheet Status* table

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	TBD	0	TBD	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	TBD	TBD	TBD	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	TBD	TBD	TBD	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	TBD	TBD	TBD	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	TBD	TBD	TBD	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	TBD	TBD	TBD	ps
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	TBD	TBD	TBD	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	TBD	TBD	TBD	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	TBD	TBD	TBD	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	TBD	TBD	TBD	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	TBD	TBD	TBD	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	TBD	TBD	TBD	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	TBD	TBD	TBD	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	TBD	TBD	TBD	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	TBD	TBD	TBD	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	TBD	TBD	TBD	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	TBD	TBD	TBD	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	TBD	TBD	TBD	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	TBD	TBD	TBD	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	TBD	TBD	TBD	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	TBD	TBD	TBD	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	TBD	TBD	TBD	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	TBD	TBD	TBD	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	TBD	TBD	TBD	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	TBD	TBD	TBD	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	TBD	TBD	TBD	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	TBD	TBD	TBD	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	TBD	TBD	TBD	ps
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	TBD	TBD	TBD	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	TBD	TBD	TBD	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	TBD	TBD	TBD	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	TBD	TBD	TBD	ps

Table 68. HPS Programmable I/O Delay (Input Path) for Intel Agilex Device

For specification status, see the *Data Sheet Status* table

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	TBD	0	TBD	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	TBD	TBD	TBD	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	TBD	TBD	TBD	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	TBD	TBD	TBD	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	TBD	TBD	TBD	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	TBD	TBD	TBD	ps
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	TBD	TBD	TBD	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	TBD	TBD	TBD	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	TBD	TBD	TBD	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	TBD	TBD	TBD	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	TBD	TBD	TBD	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	TBD	TBD	TBD	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	TBD	TBD	TBD	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	TBD	TBD	TBD	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	TBD	TBD	TBD	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	TBD	TBD	TBD	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	TBD	TBD	TBD	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	TBD	TBD	TBD	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	TBD	TBD	TBD	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	TBD	TBD	TBD	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	TBD	TBD	TBD	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	TBD	TBD	TBD	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	TBD	TBD	TBD	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	TBD	TBD	TBD	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	TBD	TBD	TBD	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	TBD	TBD	TBD	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	TBD	TBD	TBD	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	TBD	TBD	TBD	ps
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	TBD	TBD	TBD	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	TBD	TBD	TBD	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	TBD	TBD	TBD	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	TBD	TBD	TBD	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

Configuration Specifications

General Configuration Timing Specifications

Table 69. General Configuration Timing Specifications for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Requirement		Unit
		Min	Max	
$t_{CF12ST1}$ (79)	nCONFIG high to nSTATUS high	—	20	ms
$t_{CF02ST0}$	nCONFIG low to nSTATUS low	—	400	ms
t_{ST0}	nSTATUS low pulse during configuration error	0.5	10	ms
t_{CD2UM} (80)	CONF_DONE high to user mode	—	5	ms

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 70. POR Delay Specification for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16, AVST ×32	11	17	ms
AS (Fast mode)	1.1	6.9	ms

(79) The maximum time does not exceed 2× of the typical value.

(80) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

External Configuration Clock Source Requirements

Table 71. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

For specification status, see the *Data Sheet Status* table

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency(81)	Powered by V_{CCIO_SDM}	25/100/125			MHz
Clock input jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

JTAG Configuration Timing

Table 72. JTAG Timing Parameters and Values for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

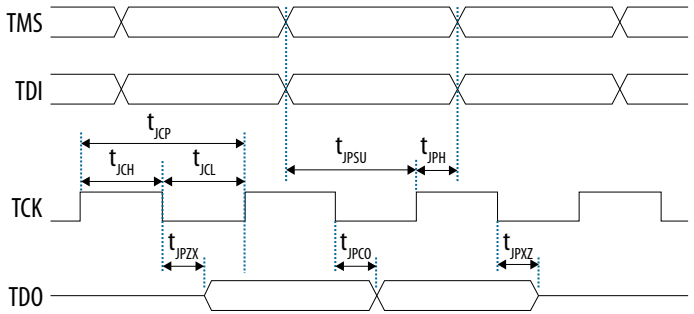
Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns

continued...

(81) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Intel Quartus Prime software. Other frequencies in the range are not supported.

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JPCO}	JTAG port clock to output	—	7	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 24. JTAG Timing Diagram



AS Configuration Timing

Table 73. AS Timing Parameters for Intel Agilex Devices

Intel recommends performing trace length matching for nCS0 and AS_DATA pins to AS_CLK to minimize the skew. The maximum tolerance for skew between nCS0 and AS_CLK is recommended to be less than 200 ps. The tolerance for skew between AS_CLK to AS_DATA must be within 0 ps – 400 ps.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (82)	AS_CLK clock period	—	7.52	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	4.21(83)	—	7.50(83)	ns

continued...

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	5.18(83)	—	8(83)	ns
T_{do} (84)	AS_DATA0 output delay	0	—	1.5	ns
T_{ext_delay} (85) (86)	Total external propagation delay on AS signals	0	—	15	ns
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	1	—	—	AS_CLK

(82) AS_CLK f_{MAX} has dependency on the maximum board loading. For AS single device configuration or AS using multiple serial flash devices configuration, use the equations in T_{do} and T_{ext_delay} notes to ensure your board has sufficient timing margin to meet flash setup/hold time specifications and Intel Agilex AS timing specifications in the *Intel Agilex Device Datasheet*. For AS using multiple serial flash devices, refer to the *Intel Agilex Configuration User Guide* for the recommended AS_CLK frequency and maximum board loading.

(83) AS operating at maximum clock frequency = 133 MHz. The delay is larger when operating at AS clock frequency lower than 133 MHz.

(84) Load capacitance for DCLK = 12 pF and AS_DATA = 27 pF. Intel recommends obtaining the T_{do} for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPIC simulation. To analyze flash setup time,

- T_{su} = AS_CLK/2 - $T_{do(max)}$ + T_{bd_clk} – $T_{bd\_data(max)}$
- T_{ho} = AS_CLK/2 + $T_{do(min)}$ – T_{bd_clk} + $T_{bd\_data(min)}$

(85) T_{ext_delay} = T_{bd_clk} + T_{co} + T_{bd_data} + T_{add}

- T_{bd_clk}: Propagation delay for AS_CLK between FPGA and flash device.
- T_{co}: Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.
- T_{bd_data}: Propagation delay for AS_DATA bus between FPGA and flash device.
- T_{add}: Propagation delay for active/passive components on AS_DATA interfaces.

(86) T_{ext_delay} specification is based on AS_CLK = 133 MHz. The value can be larger at lower AS_CLK frequency. For more details, refer to the *Intel Agilex Configuration User Guide*.

Figure 25. AS Configuration Serial Output Timing Diagram

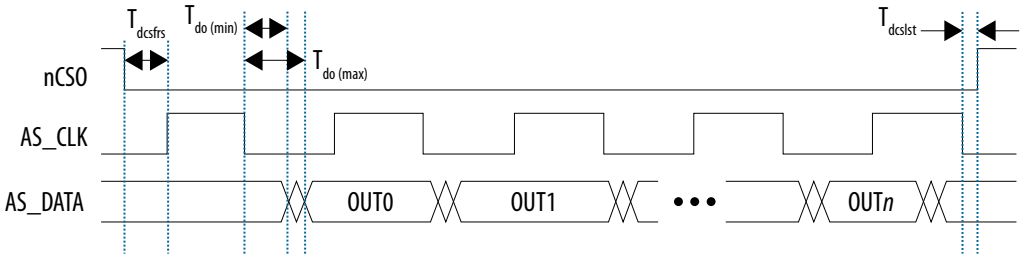
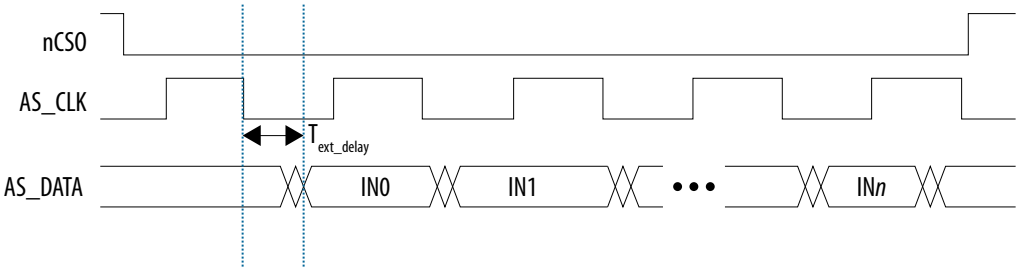


Figure 26. AS Configuration Serial Input Timing Diagram



Related Information

Intel Agilex Configuration User Guide
Provides more information about AS_CLK.

Avalon Streaming (Avalon-ST) Configuration Timing

Table 74. Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Agilex Devices

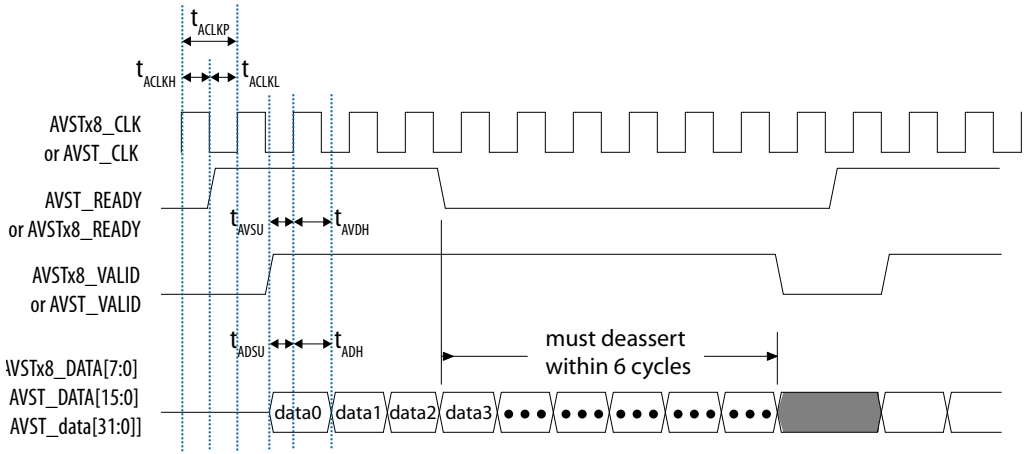
For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Unit
t_{ACLKH}	AVST_CLK high time	3.6	ns
t_{ACLKL}	AVST_CLK low time	3.6	ns

continued...

Symbol	Description	Minimum	Unit
t_{ACLKP}	AVST_CLK period	8	ns
t_{ADSU} (87)	AVST_DATA setup time before rising edge of AVST_CLK	2.1	ns
t_{ADH} (87)	AVST_DATA hold time after rising edge of AVST_CLK	0	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	2.1	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	ns

Figure 27. Avalon-ST Configuration Timing Diagram



(87) Data sampled by the FPGA (sink) at the next rising clock edge.

Configuration Bit Stream Sizes

Table 75. Configuration Bit Stream Sizes for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Variant	Compressed Configuration Bit Stream Size (Mbits)
AGF004, AGF006	178.4
AGF008	238
AGF012, AGF014	446.3
AGF022, AGF027, AGI022, AGI027	833.4

Maximum Configuration Time Estimation

Table 76. Maximum Configuration Time Estimation for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

Variant	Maximum Configuration Time (ms)			
	AS ×4	AVST ×8	AVST ×16	AVST ×32
AGF004, AGF006	554.3	315.6	221.9	122.4
AGF008	773.1	414.9	288.1	155.6
AGF012, AGF014	1,400	762.3	519.7	271.3
AGF022, AGF027, AGI022, AGI027	2,500	1,400	949.6	486.3

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

AN 775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

Programmable IOE Delay

Table 77. Programmable IOE Delay for Intel Agilex Devices

For specification status, see the *Data Sheet Status* table

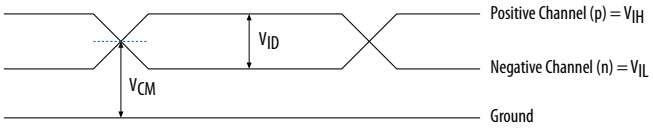
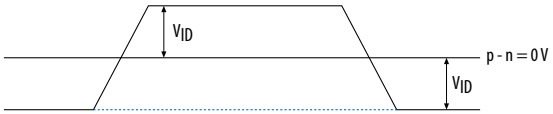
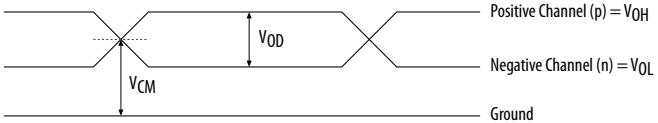
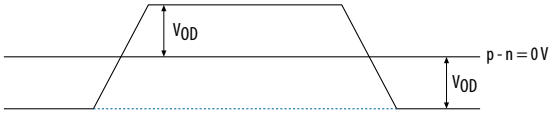
Parameter	Maximum Offset	Minimum offset	Fast Model	Slow model		Unit
			Extended	–E2	–E3	
Input Delay Chain (INPUT_DELAY_CHAIN)	63	0	1.748	2.659	3.030	ns
Output Delay Chain (OUTPUT_DELAY_CHAIN)	15	0	0.410	0.626	0.712	ns

Glossary

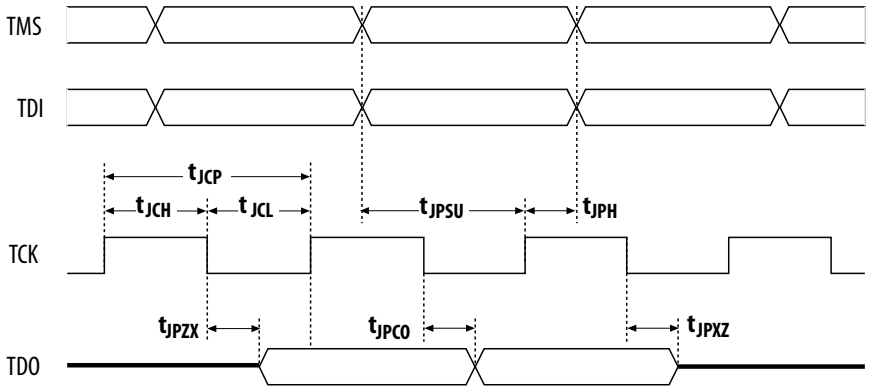
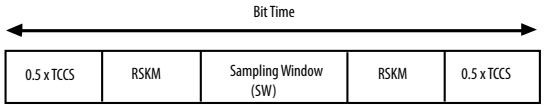
Table 78. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	LVDS SERDES block—maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J (SERDES factor)	LVDS SERDES block—deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Intel Agilex device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

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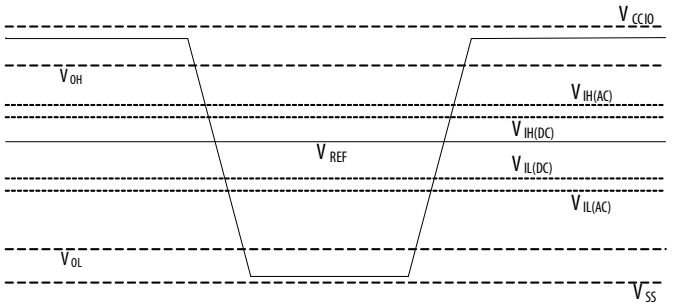
Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	LVDS SERDES block—duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—the common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage—minimum DC input differential voltage required for switching.

continued...

Term	Definition
V_{IH}	Voltage input high—the minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—the maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—the common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	LVDS SERDES block—Clock Boost Factor.

Document Revision History for the Intel Agilex Device Data Sheet

Document Version	Changes
2020.06.30	• Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Added note to $V_{CCIO\_PIO\_SDM}$. — Removed the note on HPS_PORSEL from t_{RAMP}. HPS_PORSEL pin is not available for Intel Agilex devices. • Added note to T_{ext_delay} in the *AS Timing Parameters for Intel Agilex Devices* table. • Removed SD/MMC configuration mode specifications in the following tables: — *POR Delay Specification for Intel Agilex Devices* — *Maximum Configuration Time Estimation for Intel Agilex Devices*
2020.05.14	Updated $V_{CCFUSEWR\_SDM}$ specifications in the *Recommended Operating Conditions for Intel Agilex Devices* table.

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Document Version	Changes
2020.03.18	• Added the *Absolute Maximum Rating for Intel Agilex Devices* table. • Added *Maximum Allowed Overshoot and Undershoot Voltage* section. • Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Updated the typical values for V_{CC} and V_{CCP}. — Added V_{CCR_CORE} specifications. — Updated description for V_{CCPT} and $V_{CCIO\_PIO\_SDM}$. — Updated $V_{CCFUSEWR\_SDM}$ and V_I specifications. — Updated V_{CCA_PLL} specifications and description. — Added a note for T_J minimum specifications for Industrial. — Updated t_{RAMP} minimum specification. • Updated the *E-Tile Transceiver Power Supply Operating Conditions* table. — Updated V_{CCCLK_GXE} for maximum DC level. — Updated V_{CCCLK_GXE} for recommended AC transient level. — Updated wording for all recommended DC values from % of DC level to % of $V_{nominal}$. • Updated wording for all recommended DC values from % of DC level to % of $V_{nominal}$ in the *P-Tile Transceiver Power Supply Operating Conditions*. • Updated the *E-Tile Transmitter and Receiver Data Rate Performance Specifications* table with the transceiver speed grades for the NRZ and PAM4 supported data rates. • Updated the transmitter differential output voltage peak-to-peak typical value in the *E-Tile Transmitter Specifications* table. • Updated the *E-tile Receiver Specifications* table: — Added the absolute V_{max} for a receiver pin specification — Added the maxium peak-to-peak differential input voltage V_{ID} (diff p-p) before/after device configuration specification — Added V_{ICM} (AC coupled) specification — Removed the electrical idle detection voltage specification • Updated *P-Tile Transceiver Performance*: — Added supported data rate for Gen1, Gen 2, Gen 3, and Gen 4 in the *P-Tile Transmitter and Receiver Data Rate Performance* table. — Removed the maximum VCO frequency value and replaced it with a typical value in the *P-Tile PLLA Performance* table. — Removed the maximum VCO frequency value and replaced it with a typical value in the *P-Tile PLLB Performance* table. • Updated *P-Tile Transmitter Specifications*: — Added PCIe condition for Supported I/O Standards. — Removed V_{OCM} (AC Coupled). • Updated *P-Tile Receiver Specifications*: — Added PCIe condition for Supported I/O Standards. — Added PCIe 8.0 GT/s and 16.0 GT/s specifications for the peak-to-peak differential input voltage V_{ID} (diff p-p) and added corresponding notes. — Updated RESREF specification. Added a note to the RESREF specification. • Updated V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ specifications for SmartVID in the *HPS Power Supply Operating Conditions for Intel Agilex Devices* table. • Changed *Early Power Estimator (EPE)* to *Intel FPGA Power and Thermal Calculator*.

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Document Version	Changes
	• Added a note to 1.2 V LVCMOS in the *Single-Ended I/O Standards Specifications for Intel Agilex Devices* table. • Added a note in the *Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications for Intel Agilex Devices* table. • Updated the *Differential I/O Standards Specifications for Intel Agilex Devices* table. — Updated I/O standard name from "1.5 V True Differential Signaling" to "True Differential Signaling (Transmitter & Receiver)". — Added specifications for True Differential Signaling (Receiver only). — Updated note to True Differential Signaling. • Updated the *I/O PLL Specifications for Intel Agilex Devices* table. — Added notes for t_{FCOMP}, t_{OUTPJ_DC}, and t_{OUTCCJ_DC}. — Removed t_{INCCJ} specifications. — Added t_{REFPJ} and t_{REFPN} specifications. — Updated t_{OUTPJ_DC}, t_{OUTCCJ_DC}, t_{OUTPJ_IO}, t_{OUTCCJ_IO}, and $t_{CASC\_OUTPJ\_DC}$ specifications. • Added a note for fixed-point 27 × 27 multiplication mode in the *DSP Block Performance Specifications for Intel Agilex Devices* table. • Updated the *Memory Block Performance Specifications for Intel Agilex Devices* table. — Updated the specifications for MLAB memory. — Updated the specifications for M20K block and added low power (LP) specifications. • Updated the specifications in the *Remote Temperature Diode Specifications for Intel Agilex Devices (Core Fabric TSD)* table. • Added the *Remote Temperature Diode Specifications for Intel Agilex Devices (P-Tile TSD)* table. • Updated the *LVDS SERDES Specifications for Intel Agilex Devices* table. — Updated the tx Jitter - True Differential I/O Standards specifications for –4 speed grade. — Removed global, regional, or local in clock routing resource. • Updated the DPA Lock Time Specifications for Intel Agilex Devices table. — Updated the description of the table. — Updated the maximum data transition from 960 to 768. • Updated the jitter requirements in the *Memory Output Clock Jitter Specifications* section. • Updated the specifications in the *Maximum HPS Clock Frequencies for Intel Agilex Devices* table. • Updated the *HPS Programmable I/O Delay (Output Path) for Intel Agilex Device* and *HPS Programmable I/O Delay (Input Path) for Intel Agilex Device* tables. • Updated the following diagrams: — *USB ULPI Timing Diagram* — *RGMII TX Timing Diagram* — *RMII TX Timing Diagram* — *RMII RX Timing Diagram* • Updated t_{ST0} and t_{CD2UM} specifications in the *General Configuration Timing Specifications for Intel Agilex Devices* table.

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Document Version	Changes
	• Added notes to T_{clk} and T_{do} specifications in the *AS Timing Parameters for Intel Agilex Devices* table. • Updated t_{ADSU} and t_{AVSU} specifications in the *Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Agilex Devices* table. • Added the following tables: — *Configuration Bit Stream Sizes for Intel Agilex Devices* — *Maximum Configuration Time Estimation for Intel Agilex Devices* — *Programmable IOE Delay for Intel Agilex Devices*
2019.12.18	Updated the *I/O PLL Specifications for Intel Agilex Devices* table. • Removed `scanclk` from $f_{DYCONFIGCLK}$ parameter. • Corrected the maximum specification for $f_{DYCONFIGCLK}$ from 200 MHz to 100 MHz.
2019.04.02	Initial release.