2. Description, Architecture, and Features

H51016-2.5

Introduction

Altera® HardCopy® II devices feature an architecture that provides high-density, high-performance, and low-power consumption suitable for a variety of applications. HardCopy II devices are low-cost structured ASICs with pin-outs, densities, and architecture that complement Stratix® II FPGAs. HardCopy II devices make optimal use of die area and core resources while offering features that are functionally equivalent to the Stratix II FPGA. The combination of Stratix II FPGAs for in-system prototype and design verification, HardCopy II devices for high-volume production, and the Quartus® II design software, provide a complete, seamless path from prototype to volume production. Table 2–1 provides an overview of the HardCopy II device features.

Table 2–1. HardCopy II Family Overview (Part 1 of 2)

Feature	HC210W *(1)*	HC210	HC220	HC230	HC240
ASIC gates *(2)*	1,000,000	1,000,000	1,900,000	2,900,000	3,600,000
M4K RAM blocks (4k bits plus parity)	190	190	408	614	768 *(3)*
M-RAM blocks (512k bits plus parity)	0	0	2	6	9
Total RAM bits (including parity bits)	875,520	875,520	3,059,712	6,368,256	8,847,360
Enhanced PLLs	2	2	2	4	4
Fast PLLs	2	2	2	4	8
Package (maximum user I/O pins) *(4)*, *(5)*	484-pin FineLine BGA (308)	484-pin FineLine BGA (334)	672-pin FineLine BGA (492) 780-pin FineLine BGA (494)	1,020-pin FineLine BGA (698)	1,020-pin FineLine BGA (742) 1,508-pin FineLine BGA (951)

Table 2–1. HardCopy II Family Overview (Part 2 of 2)

Feature	HC210W *(1)*	HC210	HC220	HC230	HC240
FPGA prototype options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180

Notes to Table 2–1:

(1) HC210W devices use a wire bond package. All other HardCopy II devices and Stratix II FPGAs use a flip-chip package. Devices in a wire bond package offer different performance and signal integrity characteristics compared to devices in a flip-chip package.

(2) This is the number of ASIC gates available in the HardCopy II base array for both logic and DSP functions that can be implemented in a Stratix II FPGA prototype.

(3) Total number of usable M4K blocks is 768, which allows migration compatibility when prototyping with an EP2S180 device. This may be different from the Quartus II software total physical M4K count of the HC240.

(4) The I/O pin counts include the dedicated clock input pins, which can be used for clock signals or data inputs.

(5) The Quartus II I/O pin counts include an additional pin (`PLLENA`), which is not available as a general-purpose I/O pin. The `PLLENA` pin can only be used to enable the PLLs.

Functional Description

The HardCopy II device family provides greater flexibility to design with FPGA prototypes before moving to structured ASICs for production. Before seamlessly migrating to the HardCopy II structured ASIC, designers can prototype and test their design functionality using a Stratix II FPGA. There are multiple options for the prototype FPGA, allowing designers to choose the right HardCopy II device for volume production and maximum cost savings. The Quartus II design software includes features such as the Device Resource Guide, to help select the optimal HardCopy II device based on the design requirements.

For more information on the Device Resource Guide, refer to the *Quartus II Support for HardCopy II Devices* chapter in the *HardCopy Series Handbook*.

HardCopy II devices require minimal involvement from the designer in the device migration process. Additionally, unlike ASICs, the designer is not required to generate test benches, test vectors, or timing and functional simulations since prototyping is performed using an FPGA.

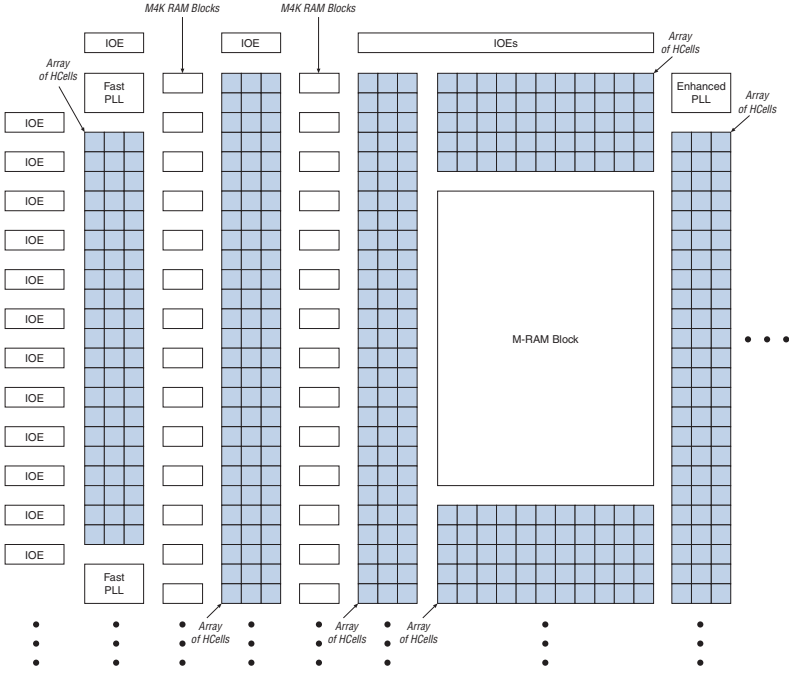
HardCopy II devices consist of base arrays that are common to all designs for a particular device density, with design-specific customization done using two metal layers. The reprogrammable FPGA logic, routing, memory, and FPGA configuration-related logic are stripped from HardCopy II devices. Removing all programmable and configuration resources and replacing them with direct metal connections results in considerable die size reduction and cost savings. A fine-grain architecture consisting of an array of HCells extends the die reduction and cost

savings, which results in low-cost structured ASICs with high-performance and low-power suitable for a wide variety of applications.

The SRAM configuration cells of the Stratix II FPGAs are replaced in HardCopy II devices with metal connections, which define the function of logic, memory, phase-locked loop (PLL), and I/O elements (IOEs) in the device. These resources are interconnected using metallization layers. Once a HardCopy II device is manufactured, the functionality of the device is fixed.

HardCopy II devices are manufactured using the same 90-nm process technology and operate using the same core voltage (1.2 V) as Stratix II FPGAs. Additionally, almost all architectural features in HardCopy II devices are functionally equivalent to features found in the Stratix II FPGA architecture. HardCopy II devices feature HCells, memory blocks, PLLs, and IOEs (Figure 2–1).

Figure 2–1. Example Block Diagram of HC230 Device *Note (1)*



Note to Figure 2–1:

(1) Figure 2–1 shows a graphical representation of the device floor plan. A detailed floor plan is available in the Quartus II software.

HardCopy II and Stratix II Similarities and Differences

HardCopy II devices preserve the functionality of Stratix II FPGAs. Implementation of these architectural features in HardCopy II structured ASICs matches Stratix II FPGA implementation, with a few exceptions. Table 2–2 shows a qualitative comparison of HardCopy II device feature implementation versus Stratix II FPGA feature implementation. Other sections within this chapter provide details on similarities and differences of a particular HardCopy II feature.

Table 2–2. HardCopy II Device vs. Stratix II FPGA Feature Implementation

Feature	Equivalent	Different
Logic blocks		✓
DSP blocks		✓
Memory	✓	
Clock networks	✓	
PLLs	✓	
I/O features	✓	
Configuration *(1)*		✓

Note to Table 2–2:
(1) HardCopy II structured ASICs do not need to be configured upon power-up.

The major similarities and differences between Stratix II FPGAs and HardCopy II devices are highlighted below:

- HardCopy II may result in a power reduction of up to 50% than an equivalent Stratix II FPGAs operating at the same frequency. Power consumption is design dependent and is a direct result of design performance and resource utilization.
- HardCopy II devices offer up to 100% performance improvement when compared to Stratix II FPGA prototypes. The performance improvement is achieved by efficient use of logic blocks, metal interconnect optimization, die size reduction, and customized signal buffering.
- Logic blocks, known as HCells, are the basic building block of the core logic in HardCopy II devices and replace Stratix II adaptive logic modules (ALMs). HCells implement logic and DSP functions.
- DSP block functions are implemented using HCells, instead of dedicated DSP blocks.
- M4K and M-RAM memory blocks can implement various types of memory (the same as Stratix II FPGAs), with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and first-in first-out (FIFO) buffers.

- Unlike Stratix II FPGAs, the HardCopy II M4K block contents cannot be pre-loaded with a Memory Initialization File (**.mif**) when used as RAM. When used as ROM, HardCopy II M4K blocks are initialized to the ROM contents.
- When used as RAM, and you select the non-registered output mode, HardCopy II M4K and M-RAM blocks power up with outputs unknown. In Stratix II FPGAs, M4K blocks power up with outputs cleared, while M-RAM blocks power up with outputs unknown. If registered outputs mode is selected, the outputs are cleared on both the M4K and M-RAM blocks in HardCopy II.
- The memory contents are unknown under both instances.
- All HardCopy II clock network features are the same as in Stratix II FPGAs.
- Enhanced PLL and fast PLL implementations in HardCopy II devices are the same as in Stratix II FPGAs.
- All Stratix II I/O features and supported I/O standards are offered in HardCopy II devices.
- The Joint Test Action Group (JTAG) boundary scan order and length in HardCopy II devices is different than that of the Stratix II FPGA. Use a HardCopy II boundary-scan description language (BSDL) file that describes the re-ordered and shortened boundary scan chain.
- Unlike Stratix II devices, HardCopy II devices are customized using two metal layers. Therefore, configuration circuitry is not required. FPGA configuration emulation and other configuration modes, including remote system upgrades and design security using configuration bitstream encryption, are not supported in HardCopy II devices.
- Even though configuration is not required, the `CRC_ERROR` pin function is supported by the HardCopy II using Quartus II software version 6.0 and above. There is no need to recompile the Stratix II design to eliminate this feature.

Only supplementary information to highlight HardCopy II similarities and differences compared to the Stratix II FPGA architecture and functionality is provided in this chapter. For more information on similarities and differences of available resources of the HardCopy II, refer to the *Migrating Stratix II Device Resources to HardCopy II Devices* chapter of this Handbook. In addition, the *Stratix II Device Handbook* has detailed explanations of architectural features and functions that are similar to the HardCopy II devices.

HCells

HardCopy II devices are built using an array of fine-grained architecture blocks called HCells. HCells are a collection of logic transistors based on 1.2 V, 90 nm process technology, similar to Stratix II devices. The construction of logic using HCells allows flexible functionality such that when HCells are combined, all viable logic combinations of Stratix II functionality are replicated. These HCells constitute the array of HCells area in Figure 2–1. Only HCells needed to implement the customer design are assembled together, which optimizes HCell utilization. The unused area of the HCell logic fabric is powered down, resulting in significant power savings compared with the Stratix II FPGA prototype.

The Quartus II software uses the library of pre-characterized HCell macros to place Stratix II ALM and DSP configurations into the HardCopy II HCell-based logic fabric. An HCell macro defines how a group of HCells are connected together within the array. HCell macros can construct all combinations of combinational logic, adder, and register functions that can be implemented by a Stratix II ALM. HCells not used for ALM configurations can be used to implement DSP block functions.

Based on design requirements, the Quartus II software will chose the appropriate HCell macros to implement the design functionality. For example, Stratix II ALMs offer flexible look-up table (LUT) blocks, registers, arithmetic blocks, and LAB-wide control signals. In HardCopy II devices, if your design requires these architectural elements, the Quartus II synthesis tool will map the design to the appropriate HCells, resulting in improved design performance compared to the Stratix II FPGA prototype.

Stratix II FPGAs have dedicated DSP blocks to implement various DSP functions. Stratix II DSP blocks consist of a multiplier block, an adder/subtractor/accumulator block, a summation block, input and output interfaces, and input and output registers. In HardCopy II devices, HCell macros implement Stratix II DSP block functionality with area efficiency and performance on par with the dedicated DSP blocks in Stratix II FPGAs.

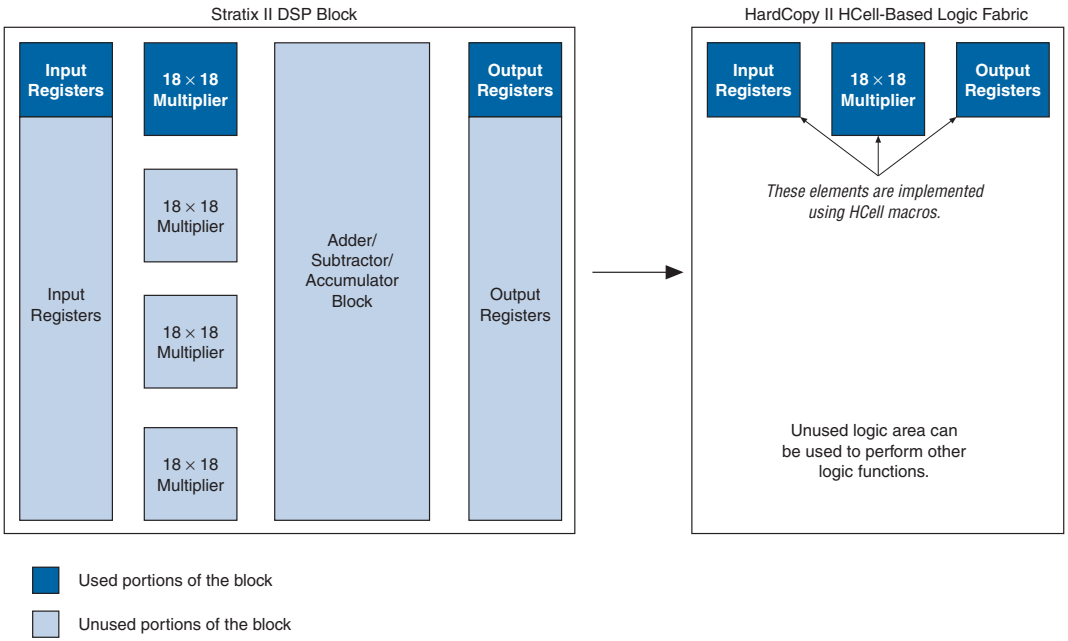
There are eight HCell macros which implement the eight supported modes of operation for the Stratix II DSP block:

- 9 × 9 multiplier
- 9 × 9 two-multiplier adder (9 × 9 complex multiply)
- 9 × 9 four-multiplier adder
- 18 × 18 multiplier
- 18 × 18 two-multiplier adder (18 × 18 complex multiply)
- 18 × 18 four-multiplier adder
- 52-bit (18 × 18) multiplier-accumulator
- 36 × 36 multiplier

Only HCells that are required to implement the design's DSP functions are enabled. HCells not needed for DSP functions can be used for ALM configurations, which results in efficient logic usage. In addition to area management, the placement of these HCell macros allows for optimized routing and performance.

An example of efficient logic area usage can be seen when comparing the 18 × 18 multiplier implementation in Stratix II FPGAs using the dedicated DSP block versus the implementation in HardCopy II devices using HCells. If the Stratix II DSP function only calls for one 18 × 18 multiplier, the other three 18 × 18 multipliers and the DSP block's adder output block are not used (Figure 2–2). In HardCopy II devices, the HCell-based logic fabric that is not used for DSP functions can be used to implement other combinational logic, adder, and register functions.

Figure 2–2. Stratix II DSP Block versus HardCopy II HCell 18 × 18-Bit Multiplier Implementation



HardCopy II devices support all Stratix II DSP configurations (9 × 9, 18 × 18, and 36 × 36 multipliers) and all Stratix II DSP block features, such as dynamic sign controls, dynamic addition/subtraction, saturation, rounding, and dynamic input shift registers, except for dynamic mode switching.

Dynamic mode switching allows the designer to set up each Stratix II DSP block to dynamically switch between the following three modes:

- Up to four 18-bit independent multipliers
- Up to two 8-bit multiplier-accumulators
- One 36-bit multiplier

Each half of a Stratix II DSP block has separate mode control signals. Since DSP block functions are implemented in HardCopy II devices using HCells, HardCopy II devices do not support dynamic mode switching. If this feature is used, the Quartus II software flags the DSP implementation and does not allow you to migrate the design. The fitter reports that all HardCopy II devices are not compatible with the design. To migrate your Stratix II design to a HardCopy II companion device, disable dynamic switching in the DSP blocks.

For more information on the Stratix II DSP operational modes, refer to the *Stratix II Device Handbook*.

Embedded Memory

HardCopy II memory blocks can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. HardCopy II devices support the same memory functions and features as Stratix II FPGAs.

Functionally, the memory in both devices are identical. However, the number of available memory blocks differs based on density (Table 2–3).

Table 2–3. HardCopy II Embedded Memory Resources

Feature	HC210W	HC210	HC220	HC230	HC240
M4K RAM blocks (4 Kbits)	190	190	408	614	768
M-RAM blocks (512 Kbits)	0	0	2	6	9
Total RAM bits (bits)	875,520	875,520	3,059,712	6,368,256	8,847,360

Since device functionality is fixed in HardCopy II devices, M4K block contents cannot be preloaded or initialized with a MIF when they are configured as RAM. When the M4K blocks are used as ROM, they will initialize to the design's ROM contents.

When using the non-registered outputs mode for the HardCopy II M4K memory block, the outputs power up uninitialized. When using the registered outputs mode for the HardCopy II M4K memory blocks, the

outputs are cleared on power up. The designer needs to take these into consideration when designing logic that might evaluate the initial power-up values of the memory block.

HardCopy II embedded memory consists of M4K and M-RAM memory blocks and have a one-to-one mapping from Stratix II M4K and M-RAM resources. Table 2–4 shows the size and features of the different RAM blocks.

For more information on the Stratix II memory block features, refer to the *Stratix II Device Handbook*.

PLLs and Clock Networks

Both HardCopy II enhanced and fast PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs are used for general-purpose clock management, supporting multiplication, division, phase shifting, and programmable duty cycle. In addition, enhanced PLLs support external clock feedback mode, spread-spectrum clocking, and counter cascading. Fast PLLs offer high speed outputs to manage the high-speed differential I/O interfaces.

All Stratix II PLL features are supported by HardCopy II PLLs.

Similar to Stratix II FPGAs, HardCopy II devices also support a power-down mode where unused clock networks can be disabled. HardCopy II and Stratix II clock control blocks support dynamic selection of the input clock from up to four possible sources, giving the designer the flexibility to choose from multiple (up to four) clock sources.

Table 2–4. HardCopy II Embedded Memory Features (Part 1 of 2) *Notes (1), (2), (3)*

Feature	M4K Blocks	M-RAM Blocks
Maximum performance *(1)*, *(4)*	350 MHz	350 MHz
Total RAM bits (including parity bits)	4,608	589,824
Configurations	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144
Parity bits	✓	✓
Byte enable	✓	✓
Pack mode	✓	✓
Address clock enable	✓	✓
Single-port memory	✓	✓
Simple dual-port memory	✓	✓
True dual-port memory	✓	✓
Embedded shift register	✓	
ROM	✓	
FIFO buffer	✓	✓
Simple dual-port mixed width support	✓	✓
True dual-port mixed width support	✓	✓
Memory initialization file (**.mif**)	Not supported, except in ROM mode	Not supported
Mixed-clock mode	✓	✓
Power-up condition *(2)*	Outputs unknown	Outputs unknown
Register clears *(3)*	Output registers only	Output registers only
Same-port read-during-write	New data available at positive clock edge	New data available at positive clock edge
Mixed-port read-during-write	Outputs set to unknown or old data	Unknown output

Table 2–4. HardCopy II Embedded Memory Features (Part 2 of 2) Notes (1), (2), (3)		
Feature	**M4K Blocks**	**M-RAM Blocks**

Note to Table 2–4:
(1) Maximum performance information is preliminary until device characterization.
(2) The memory cells power up randomly, so reads before writes are not valid. Make sure you write to the memory location before you read it.
(3) Even though the output register is cleared, the memory cells power up randomly. So reads before write are not valid. Make sure you write to the memory location first before reading it.
(4) Violating the setup or hold time requirements on the address registers could corrupt the memory contents. This applies to both read and write operations.

Enhanced and Fast PLLs

The number of PLLs available differs based on density (Table 2–5).

Table 2–5. HardCopy II PLLs					
Feature	**HC210W**	**HC210**	**HC220**	**HC230**	**HC240**
Enhanced PLLs	2	2	2	4	4
Fast PLLs	2	2	2	4	8

The target HardCopy II device may not support the same number of enhanced PLLs as the prototyping Stratix II FPGA. However, since HardCopy II enhanced PLLs and fast PLLs offer a similar feature set (Table 2–7 on page 2–13), a fast PLL could be used in place of an enhanced PLL. The type of PLL used in the design should be chosen using the Quartus II software to accommodate the resources available in the HardCopy II device.

Table 2–6 shows which PLLs are available in each device density. Figure 2–3 shows the location of each PLL. During the prototyping stage using the FPGA, you must select the appropriate number of enhanced and fast PLLs that will be used in your HardCopy II device. Use Table 2–6 to ensure that the FPGA prototyping design uses the same PLL resources available in the HardCopy II device.

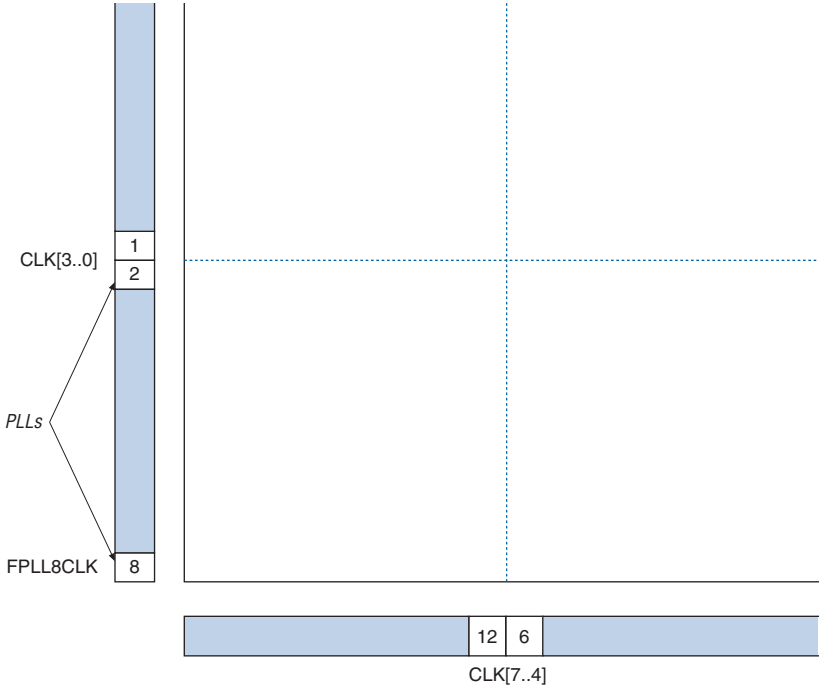
Table 2–6. HardCopy II PLLs Available (Part 1 of 2) Note (1)												
Device	**Fast PLLs**								**Enhanced PLLs**			
	1	**2**	**3**	**4**	**7**	**8**	**9**	**10**	**5**	**6**	**11**	**12**
HC210W	✓	✓							✓	✓		
HC210	✓	✓							✓	✓		

Table 2–6. HardCopy II PLLs Available (Part 2 of 2) *Note (1)*

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5	6	11	12
HC220	✓	✓							✓	✓		
HC230	✓	✓			✓	✓			✓	✓	✓	✓
HC240	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note to Table 2–6:
(1) PLL performance in the HC210W device may differ from the Stratix II FPGA prototype.

Figure 2–3. HardCopy II PLL Locations *Notes (1), (2)*



Notes to Figure 2–3:
(1) The PLLs may be located in the periphery or in the core of the device.
(2) This is the die-level top view of the device and is only a graphical representation of the PLL locations.

PLL functionality in HardCopy II devices remains the same as in Stratix II FPGA PLLs. Therefore, the HardCopy II PLLs support PLL reconfiguration (the PLL can be dynamically configured in user mode).

HardCopy II enhanced and fast PLLs support a one-to-one mapping from Stratix II PLL resources. Table 2–7 shows the features of the different PLLs. For more information on the Stratix II PLL features, refer to the *Stratix II Device Handbook*.

Table 2–7. HardCopy II PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*	Down to 125-ps increments *(3)*
Clock switchover	✓	✓ *(4)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread-spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of clock outputs per PLL *(5)*	6	4
Number of dedicated external clock outputs per PLL	Three differential or six singled-ended	*(6)*
Number of feedback clock inputs per PLL	1 *(7)*	

Notes to Table 2–7:

(1) For enhanced PLLs, *m* and *n* range from 1 to 512 and post-scale counters range from 1 to 512 with 50% duty cycle. For non-50% duty-cycle clock outputs, post-scale counters range from 1 to 256.

(2) For fast PLLs, *n* can range from 1 to 4. The post-scale and *m* counters range from 1 to 32. For non-50% duty-cycle clock outputs, post-scale counters range from 1 to 16.

(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by eight. The supported phase shift range is from 125 to 250 ps. HardCopy II devices can shift all output frequencies in increments of at least 45° . Smaller degree increments are possible depending on the frequency and divide parameters. For non-50% duty cycle clock outputs post-scale counters range from 1 to 256.

(4) HardCopy II fast PLLs only support manual clock switchover.

(5) The clock outputs can be driven to internal clock networks or to a pin.

(6) The PLL clock outputs of the fast PLLs can drive to any I/O pin to be used as an external clock output. For high-speed differential I/O pins, the device uses a data channel to generate the transmitter output clock (`txclkout`).

(7) If the design uses external feedback input pins, you will lose one (or two, if f_{BIN} is differential) dedicated external clock output pin.

Clock Networks

There are 16 clock pins (CLK[15..0]) in HardCopy II devices that can drive either the global- or regional-clock networks. The CLK pins can drive clock ports or data inputs.

HardCopy II devices provide 16 dedicated global-clock networks and 32 regional-clock networks; the same as in Stratix II FPGAs. These clocks are organized to provide 24 unique clock sources per device quadrant with low skew and delay. This clocking scheme provides up to 48 unique clock domains within the entire HardCopy II device. Table 2–8 lists the clock resources and features available in HardCopy II devices.

Table 2–8. Clock Network Resources and Features Available in HardCopy II Devices

Resources and Features	Availability
Number of global clock networks	16
Number of regional clock networks	32
Global clock input sources	Clock input pins, PLL outputs, logic array
Regional clock input sources	Clock input pins, PLL outputs, logic array
Number of unique clock sources in a quadrant	24 (16 global clocks and 8 regional clocks)
Number of unique clock sources in the entire device	48 (16 global clocks and 32 regional clocks)
Power-down mode	Global- and regional-clock networks, dual-regional-clock region
Clocking regions for high fan-out applications	Quadrant region, dual-regional, entire device via global- or regional-clock networks

HardCopy II devices also support the same features as the Stratix II clock control block, which is available for each global- and regional-clock network. The control block has two functions:

- Clock source selection (dynamic selection for global clocks): You user can either dynamically select between two PLL outputs, between two clock pins (CLKp or CLKn), or a combination of the clock pins or PLL outputs.
- Clock power-down (dynamic clock enable or disable): In HardCopy II devices, you can dynamically turn the clock off or on in user-mode.

I/O Structure and Features

The structure and features of the HardCopy II IOE remains the same as in Stratix II. Any feature implemented in Stratix II IOEs can be migrated to Hardcopy II IOEs.

The IOE feature set in HardCopy II devices can be classified in one of three categories:

- General purpose IOEs—The most commonly used I/O type in designs.
- Memory Interface IOEs—Includes features to interface with common external memory standards.
- High-speed IOEs—Supports high-speed data transmission and reception.

All I/O pins in Stratix II FPGAs support general-purpose I/O standards, which includes the LVTTL and LVCMOS I/O standards. In Stratix II FPGAs, the PCI clamping diode and memory interfaces are supported on the top and bottom I/O pins, while high-speed interfaces are supported on the left and right side I/O pins of the device.

The new general purpose IOEs in HardCopy II devices are a cost saving and area efficient advantage. The complex memory interface and the high-speed IOE circuitry is removed to save die area while still offering the more commonly-used features. The memory interface IOE supports all the features available in the general purpose IOE. The high-speed IOE also supports all the same features and I/O standards as the general purpose IOE, except for the PCI clamping diode (supported on the bottom general purpose IOEs in HC210 and HC220 devices).

In order to increase the I/O area efficiency of HardCopy II devices, the features available on any given IOE depends on the location.

Table 2–9 shows which I/O standards are supported by the different IOE types.

Table 2–9. HardCopy II Supported I/O Standards (Part 1 of 3)

I/O Standard	Type	V_{CCIO} Level (V)		Memory Interface IOEs	General Purpose IOEs	High-Speed IOEs
		Input	Output			
3.3-V LVTTL/ LVCMOS	Single-ended	3.3/2.5	3.3	✓	✓	✓
2.5-V LVTTL/ LVCMOS	Single-ended	3.3/2.5	2.5	✓	✓	✓
1.8-V LVTTL/ LVCMOS	Single-ended	1.8/1.5	1.8	✓	✓	✓
1.5-V LVCMOS	Single-ended	1.8/1.5	1.5	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5	2.5	✓		

Table 2–9. HardCopy II Supported I/O Standards (Part 2 of 3)

I/O Standard	Type	V_{CCIO} Level (V)		Memory Interface IOEs	General Purpose IOEs	High-Speed IOEs
		Input	Output			
SSTL-2 class II	Voltage referenced	2.5	2.5	✓		
SSTL-18 class I	Voltage referenced	1.8	1.8	✓		
SSTL-18 class II	Voltage referenced	1.8	1.8	✓		
1.8-V HSTL class I	Voltage referenced	1.8	1.8	✓		
1.8-V HSTL class II	Voltage referenced	1.8	1.8	✓		
1.5-V HSTL Class I	Voltage referenced	1.5	1.5	✓		
1.5-V HSTL Class II	Voltage referenced	1.5	1.5	✓		
PCI/PCI-X	Single-ended	3.3	3.3	✓ *(2)*	✓ *(2)*	
Differential SSTL-2 class I and II input	Pseudo differential *(1)*	3.3/2.5/ 1.8/1.5		*(3)*		
Differential SSTL-2 class I and II output	Pseudo differential *(1)*		2.5	*(3)*		
Differential SSTL-18 class I and II input	Pseudo differential *(1)*	3.3/2.5/ 1.8/1.5		*(3)*		
Differential SSTL-18 class I and II output	Pseudo differential *(1)*		1.8	*(3)*		
1.8-V differential HSTL class I and II input	Pseudo differential *(1)*	3.3/2.5/ 1.8/1.5		*(3)*		
1.8-V differential HSTL class I and II output	Pseudo Differential *(1)*		1.8	*(3)*		
1.5-V differential HSTL class I and II input	Pseudo differential *(1)*	3.3/2.5/ 1.8/1.5		*(3)*		
1.5-V differential HSTL class I and II output	Pseudo Differential *(1)*		1.5	*(3)*		
LVDS	Differential	2.5	2.5	*(5)*	*(4)*, *(6)*	✓
HyperTransport™ technology	Differential	2.5	2.5	*(5)*	*(4)*, *(6)*	✓

Table 2–9. HardCopy II Supported I/O Standards (Part 3 of 3)

I/O Standard	Type	V_{CCIO} Level (V)		Memory Interface IOEs	General Purpose IOEs	High-Speed IOEs
		Input	Output			
LVPECL	Differential	3.3/2.5/ 1.8/1.5	*(8)*	*(8)*	*(8)*	

Notes to Table 2–9:

(1) Pseudo-differential HSTL and SSTL inputs only use the positive-polarity input in the speed path. The negative input is not connected internally. Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. This is similar to a Stratix II device implementation.
(2) The PCI clamping diode is only supported on the I/O pins on the top and bottom sides of the device.
(3) This I/O standard is only supported on the DQS, CLK and PLL_FB input pins or on the PLL_OUT output pins.
(4) This I/O standard is only supported on the bottom CLK and PLL_FB input pins or on the bottom PLL_OUT output pins.
(5) This I/O standard is only supported on the CLK and PLL_FB input pins or on the PLL_OUT output pins.
(6) Also supported on CLK9 and CLK11 pins.
(7) This I/O standard is only supported on CLK and PLL_FB input pins.
(8) LVPECL input I/O standard is supported on the top and bottom CLK and PLL_FB input pins. LVPECL output I/O standard is supported on the top and bottom PLL_OUT output pins. LVPECL support is similar to Stratix II devices.

The three types of IOEs are located in different areas of the device and are described in the following sections. HardCopy II devices have eight I/O banks, just as in Stratix II FPGAs. Figures 2–4 through 2–6 show which I/O type each bank supports.

Figure 2–4. I/O Type Support in HC210 and HC220 Devices *Notes (1), (2)*

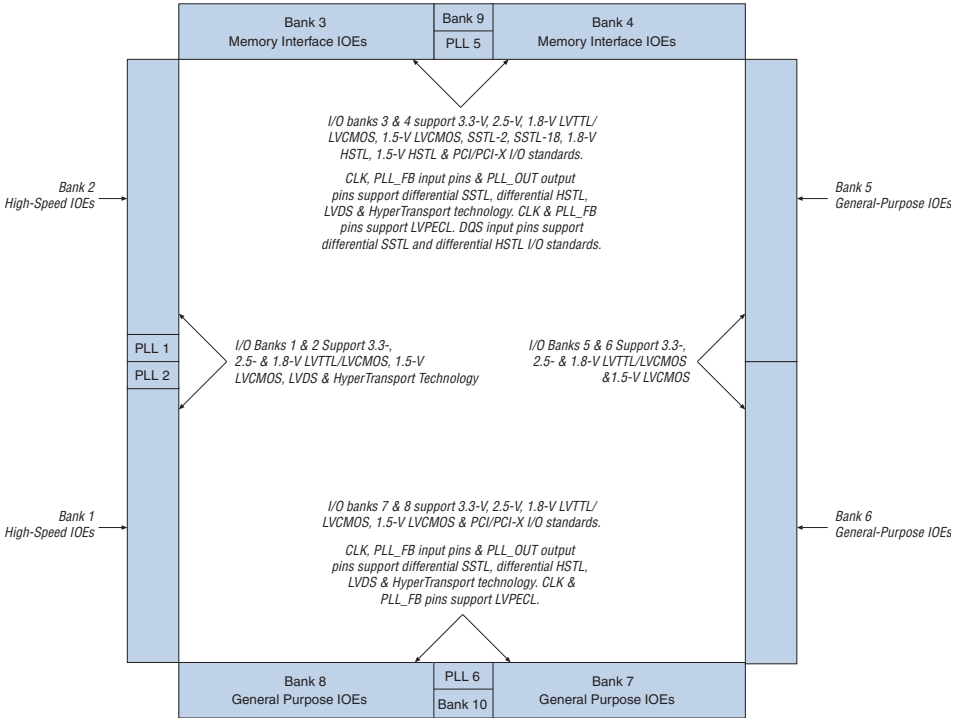


Figure 2–5. I/O Type Support in HC230 Devices *Notes (1), (2)*

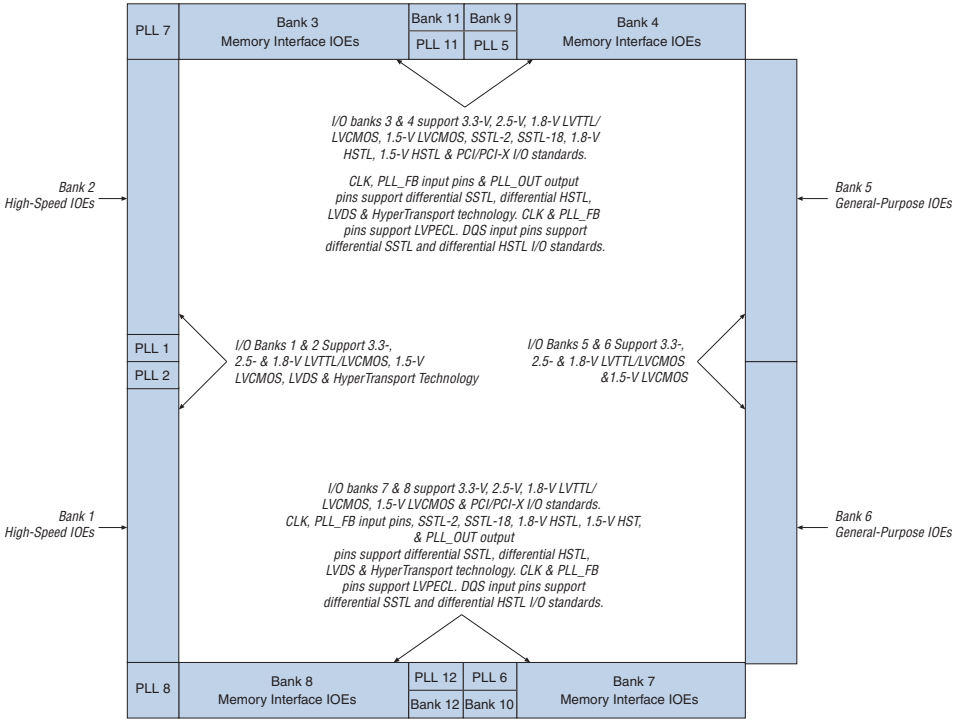
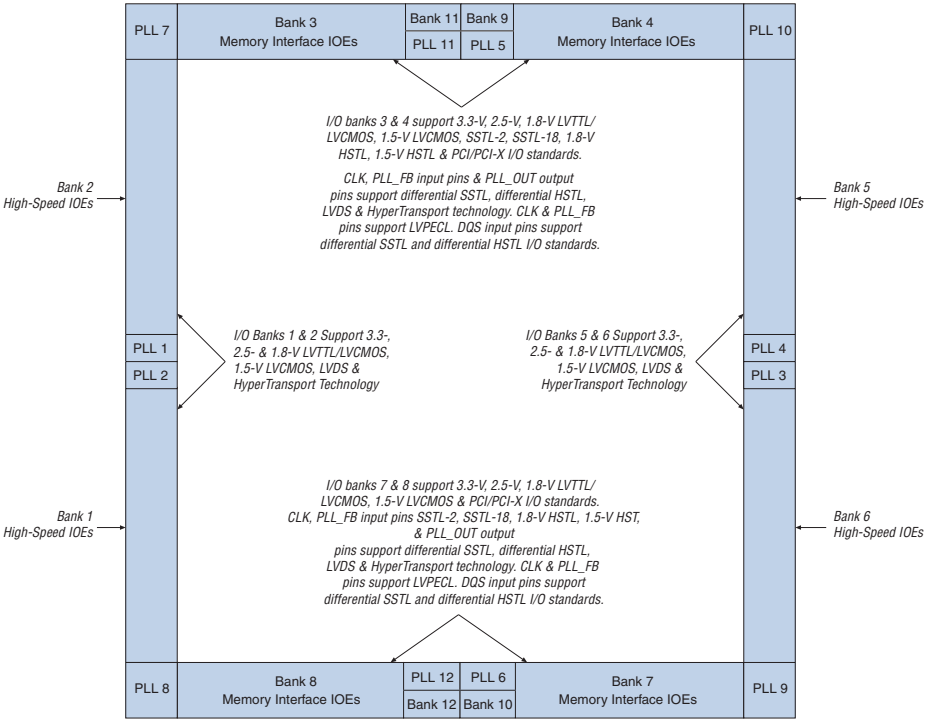


Figure 2–6. I/O Type Support in HC240 Devices *Notes (1), (2)*



Notes to Figures 2–4 through 2–6:

(1) In addition to supporting external memory interfaces, memory interface IOEs have the same features as general purpose IOEs. In addition to supporting high-speed I/O interfaces, high-speed IOEs have the same features as general purpose IOEs, except for the PCI clamping diode and LVPECL clock input support.

(2) This is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

When planning I/O placement for designs targeting HardCopy II devices, care should be taken to ensure the same I/O standards are supported in the same HardCopy II I/O banks as in the Stratix II I/O banks.

General Purpose IOE

The general purpose IOEs in HC210 and HC220 devices are located on the right side and at the bottom of the device. The general purpose IOEs in HC230 devices are located on the right side of the device. (Directions are based on a top view of the silicon die.) HC240 devices do not have general purpose IOEs. The general purpose IOE functionality is supported in the memory interface IOEs for these devices. The high-speed IOEs also

provide the same features as the general purpose IOEs except for the PCI clamping diode. In Stratix II FPGAs, all IOEs support the general purpose IOE features except the PCI diode, which is only supported on the top and bottom I/O pins.

The general purpose IOE has many features, including:

- Dedicated single-ended I/O buffers
- 3.3-V, 64-bit, 66 MHz PCI compliance
- 3.3-V, 64-bit, 133 MHz PCI-X 1.0 compliance
- JTAG boundary-scan test (BST) support
- On-chip driver series termination (non-calibrated)
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Open-drain outputs
- PCI clamping diode (supported on the bottom I/O pins only)
- Double data rate (DDR) registers

General purpose IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1

The general purpose `CLK` and `PLL_FB` input pins and the `PLL_OUT` output pins support the following I/O standards:

- LVDS
- HyperTransport technology
- LVPECL (on input clocks and `PLL_OUT` only)

The programmable drive strengths available vary depending on the I/O standard being used and are listed in Table 2–10.

Table 2–10. Programmable Drive Strength Support for General-Purpose IOEs (Part 1 of 2)

I/O Standard	Programmable Drive Strength Options (mA)
3.3-V LVTTL	4, 8, 12
3.3-V LVCMOS	4, 8
2.5-V LVTTL/LVCMOS	4, 8, 12

Table 2–10. Programmable Drive Strength Support for General-Purpose IOEs (Part 2 of 2)

I/O Standard	Programmable Drive Strength Options (mA)
1.8 V LVTTL/LVCMOS	2, 4, 6, 8
1.5 V LVCMOS	2, 4

General purpose IOEs support non-calibrated on-chip series termination. 50- and 25-Ω on-chip series termination is available for 3.3-V or 2.5-V I/O standards. 50-Ω on-chip series termination is available for 1.8- and 1.5-V I/O standards (pending characterization).

Memory Interface IOE

Memory interface IOEs in HC210 and HC220 devices are located on the top of the device. Memory interface IOEs in HC230 and HC240 devices are located on the top and the bottom of the device. In Stratix II FPGAs, the top and bottom IOEs support the memory interface IOE features.

The memory interface IOE has many features, including:

- Dedicated single-ended I/O buffers
- 3.3-V, 64-bit, 66 MHz PCI compliance
- 3.3-V, 64-bit, 133 MHz PCI-X 1.0 compliance
- JTAG BST support
- On-chip driver series termination
- V_{REF} pins
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Open-drain outputs
- PCI clamping diode
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The following I/O standards are supported when using the memory interface IOEs and can be used to interface to external memory, including DDR and DDR2 SDRAM, and QDRII, RLDRAM II, and SDR SRAM:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1

- SSTL-2 class I and II
- SSTL-18 class I and II
- 1.8-V HSTL class I and II
- 1.5-V HSTL class I and II

The memory interface DQS, CLK, and PLL_FB input pins and the PLL_OUT output pins support the following I/O standards:

- LVTTL/LVCMOS
- SSTL-2 class I and II
- SSTL-18 class I and II
- 1.8-V HSTL class I and II
- 1.5-V HSTL class I and II
- Differential SSTL-2 class I and II
- Differential SSTL-18 class I and II
- 1.8-V differential HSTL class I and II
- 1.5-V differential HSTL class I and II
- LVDS (not supported on DQS pins)
- HyperTransport technology (not supported on DQS pins)
- LVPECL on input clocks and PLL_OUT only (not supported on DQS pins)

Pseudo-differential HSTL and SSTL inputs are supported on clock and DQS pins, while outputs are supported on dedicated PLL_OUT and DQS pins. Pseudo-differential HSTL and SSTL I/O standards use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them. This I/O support is the same as in Stratix II FPGAs.

The functionality of all DQS circuitry in HardCopy II devices is the same as in Stratix II FPGAs. Table 2–11 shows the number of DQS/DQ groups supported in each HardCopy II device density and package.

Table 2–11. DQS and DQ Bus Mode Support (Part 1 of 2)

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
HC210W	484-pin FineLine BGA (Wire Bond)	4	2	0	0
HC210	484-pin FineLine BGA	4	2	0	0
HC220	672-pin FineLine BGA	9	4	2	0
	780-pin FineLine BGA	9	4	2	0
HC230	1,020-pin FineLine BGA	36	18	8	4

Table 2–11. DQS and DQ Bus Mode Support (Part 2 of 2)

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
HC240	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4

The programmable drive strengths available vary depending on the I/O standard used. The options are listed in Table 2–12.

Table 2–12. Programmable Drive Strength Support for Memory Interface IOEs

I/O Standard	Programmable Drive Strength Options (mA)
3.3-V LVTTL	4, 8, 12, 16, 20, 24
3.3-V LVCMOS	4, 8, 12, 16, 20, 24
2.5-V LVTTL/LVCMOS	4, 8, 12, 16
1.8-V LVTTL/LVCMOS	2, 4, 6, 8, 10, 12
1.5-V LVCMOS	2, 4, 6, 8
SSTL-2 class I	8, 12
SSTL-2 class II	16, 20, 24
SSTL-18 class I	4, 6, 8, 10, 12
SSTL-18 class II	8, 16, 18, 20
1.8-V HSTL class I	4, 6, 8, 10, 12
1.8-V HSTL class II	16, 18, 20
1.5-V HSTL class I	4, 6, 8, 10, 12
1.5-V HSTL class II	16, 18, 20

Memory interface IOEs support both non-calibrated and calibrated on-chip series termination. 50- and 25-Ω on-chip series termination is available for 3.3-, 2.5-, or 1.8-V I/O standards. 50-Ω on-chip series termination is available for 1.5- or 1.2-V I/O standards (pending characterization).

If on-chip series termination is enabled, programmable drive strength support is not available.

High-Speed IOE

High-speed IOEs in HC210, HC220, and HC230 devices are located on the left side of the device. High-speed IOEs in HC240 devices are located on the left and right sides of the device. (Directions are based on a top view of the silicon die.) Unlike Stratix II left and right side I/O pins, HardCopy II left and right side I/O pins do not support SSTL or HSTL I/O standards or the PCI clamping diode. In Stratix II FPGAs, the right and left IOEs support the high-speed IOE features.

The high-speed IOE has many features, including:

- Dedicated single-ended I/O buffers
- Differential I/O buffer
- JTAG BST support
- On-chip driver series termination (non-calibrated)
- On-chip termination for differential I/O standards
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Open-drain outputs
- Transmit serializer
- Receive deserializer
- Dynamic phase alignment (DPA)
- Double data rate (DDR) registers

The following I/O standards are supported when using high-speed IOEs:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- LVDS
- HyperTransport technology

The SERDES and DPA circuitry and functionality is the same in HardCopy II devices as in Stratix II FPGAs. HardCopy II devices support differential I/O standards at rates up to 1 Gbps when using DPA, and at rates up to 840 Mbps when not using DPA. Table 2–13 provides the number of differential channels per HardCopy II device.

Table 2–13. Number of Differential Channels in HardCopy II Devices *Notes (1), (2)*

Channel	HC210W	HC210	HC220		HC230	HC240	
	484-Pin FineLine BGA (Wire-Bond)	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Transmitter channels	13	19	29	29	44	88	116
Receiver channels	17	21	31	31	46	92	116

Notes to Table 2–13:
(1) The pin count does not include dedicated PLL input and output pins.
(2) The total number of receiver channels includes the non-dedicated clock channels that can optionally be used as data channels.

HardCopy II high-speed IOEs, which are on the left and/or right sides of the device, support fewer programmable drive strengths than Stratix II side IOEs. The programmable drive strengths available vary depending on the I/O standard being used. The options are listed in Table 2–14.

Table 2–14. Programmable Drive Strength Support for High-Speed IOEs

I/O Standard	Programmable Drive Strength Options (mA)
3.3-V LVTTL	4, 8, 12
3.3-V LVCMOS	4, 8
2.5-V LVTTL/LVCMOS	4, 8, 12
1.8-V LVTTL/LVCMOS	2, 4, 6, 8
1.5-V LVCMOS	2, 4

High-speed IOEs support non-calibrated on-chip series termination and differential termination on the receiver channels. 50- and 25-Ω on-chip series termination is available for 3.3- or 2.5-V I/O standards. 50-Ω on-chip series termination is available for 1.8- and 1.5-V I/O standards (pending characterization).

Power-Up Modes

The functionality of structured ASICs is determined before they are produced. Therefore, they do not require programmability. HardCopy II structured ASICs follow the same principle, enabling traditional ASIC-like power up. Although prototyping FPGAs require configuration upon power up, the HardCopy II structured ASICs do not need to be configured. HardCopy II devices do not support configuration and designers should take this into account in the prototyping-to-production development process. The HardCopy II device does not require a configuration device, but you must ensure that the *n*CE pin is low and that the *n*CONFIG and *n*STATUS pins are high after power up.

HardCopy II devices do not support FPGA configuration emulation and other configuration modes, including remote system upgrades and design security using configuration bitstream encryption.

HardCopy II devices support both instant on and instant on after 50 ms power-up modes. In the instant on power-up mode, the HardCopy II device is available for use shortly after the device powers up to a safe operating voltage. The on-chip power-on reset (POR) circuit will reset all registers. The *n*CE, *n*CONFIG, and *n*STATUS signals must be at the appropriate logic levels for the CONF_DONE output to be tristated once the POR has elapsed. This option is similar to an ASIC's functionality upon power up and is the most likely scenario in production.

In the instant on after 50 ms power-up mode, the HardCopy II device behaves similarly to the instant on mode, except that there is an additional delay of 50 ms, during which time the device will be held in reset. The CONF_DONE output is pulled low during this time, and then tri-stated after the 50 ms have elapsed.

For more information about which power-up modes HardCopy II devices support, refer to the *Power-Up Modes and Configuration Emulation in HardCopy Series Devices* chapter in the *HardCopy Series Handbook*.

Document Revision History

Table 2–15 shows the revision history for this chapter.

Table 2–15. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
September 2008, v2.5	Updated chapter number and metadata.	—
June 2007, v2.4	• Added Note 4 to Table 2–4.	—
December 2006 v2.3	• Updated Table 2–1, Table 2–4, and Table 2–11. • Added revision history.	—
March 2006, v2.2	• Updated Table 2–1, Table 2–9, Table 2–13. • Updated Figure 2–5 and Figure 2–6.	—
October 2005, v2.1	Updated graphics.	—
May 2005, v2.0	• Added Table 2–1. • Updated HCell information for DSP functions in the Functional Description section. • Updated Table 2–9. • Updated Figures 2–4, 2–5, and 2–6.	—
January 2005, v1.0	Added document to the HardCopy Series Handbook.	—