4. DC and Switching Specifications and Operating Conditions

H51018-3.3

Introduction

This chapter provides preliminary information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for HardCopy® II devices.

Absolute Maximum Ratings

HardCopy II devices are offered in both commercial and industrial grades. All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all HardCopy II devices. Table 4–1 contains the absolute maximum ratings for the HardCopy II device family.

Table 4–1. HardCopy II Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	-0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	-0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	-0.5	4.6	V
V_{CCA}	Analog power supply for PLLs	With respect to ground	-0.5	1.8	V
V_{CCD}	Digital power supply for PLLs	With respect to ground	-0.5	1.8	V
V_I	DC input voltage(4)	—	-0.5	4.6	V
I_{OUT}	DC output current, per pin	—	-25	40	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_J	Junction temperature	Ball-grid array (BGA) packages under bias	-55	125	°C

Notes to Table 4–1:

(1) Refer to the *Operating Requirements for Altera Devices Data Sheet* for more information.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to a 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–2. Maximum Duty Cycles in Voltage Transitions	
V_{IN} (V)	Maximum Duty Cycles
4	100%
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

Recommended Operating Conditions

Table 4–3 contains the HardCopy II device family's recommended operating conditions.

Table 4–3. HardCopy II Device Recommended Operating Conditions Note (1) (Part 1 of 2)					
Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	100 µs ≤ rise time ≤ 100 ms *(2)*	1.15	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	100 µs ≤ rise time ≤ 100 ms *(2)*, *(6)*	3.135 (3.0)	3.465 (3.6)	V
	Supply voltage for output buffers, 2.5-V operation	100 µs ≤ rise time ≤ 100 ms *(2)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	100 µs ≤ rise time ≤ 100 ms *(2)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 µs ≤ rise time ≤ 100 ms *(2)*	1.425	1.575	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers	100 µs ≤ rise time ≤ 100 ms *(3)*	3.135	3.465	V
V_{CCA}	Analog power supply for PLLs	100 µs ≤ rise time ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCD}	Digital power supply for PLLs	100 µs ≤ rise time ≤ 100 ms *(3)*	1.15	1.25	V
V_I	Input voltage	*(4)*, *(5)*	-0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V

Table 4–3. HardCopy II Device Recommended Operating Conditions Note (1) (Part 2 of 2)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C

Notes to Table 4–3:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
(2) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(3) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 µs to 100 ms. If V_{CCPD} is not ramped up within this specified time, the HardCopy II device will not power up successfully.
(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to a 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.
(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

DC Electrical Characteristics

Table 4–4 shows the HardCopy II device family's DC electrical characteristics.

Table 4–4. HardCopy II Device DC Operating Conditions Note (1) (Part 1 of 2)							
Symbol	**Parameter**	**Conditions**	**Device**	**Minimum**	**Typical**	**Maximum**	**Unit**
I_I	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V *(2)*	all	-10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V *(2)*	all	-10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	HC210W	—	0.09 *(3)*	*(5)*	A
			HC210	—	0.09 *(3)*	*(5)*	A
			HC220	—	0.19 *(3)*	*(5)*	A
			HC230	—	0.34 *(3)*	*(5)*	A
			HC240	—	0.52 *(3)*	*(5)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C V_{CCPD} = 3.3 V	HC210W	—	3 *(3)*	*(5)*	mA
			HC210	—	3 *(3)*	*(5)*	mA
			HC220	—	4 *(3)*	*(5)*	mA
			HC230	—	5 *(3)*	*(5)*	mA
			HC240	—	5 *(3)*	*(5)*	mA

Table 4–4. HardCopy II Device DC Operating Conditions Note (1) (Part 2 of 2)

Symbol	Parameter	Conditions	Device	Minimum	Typical	Maximum	Unit
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	HC210W	—	3 *(3)*	*(5)*	mA
			HC210	—	3 *(3)*	*(5)*	mA
			HC220	—	3 *(3)*	*(5)*	mA
			HC230	—	3 *(3)*	*(5)*	mA
			HC240	—	3 *(3)*	*(5)*	mA
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	V_I = 0; V_{CCIO} = 3.3 V	—	10	25	50	kΩ
		V_I = 0; V_{CCIO} = 2.5 V	—	15	35	70	kΩ
		V_I = 0; V_{CCIO} = 1.8 V	—	30	50	100	kΩ
		V_I = 0; V_{CCIO} = 1.8 V	—	40	75	150	kΩ
		V_I = 0; V_{CCIO} = 1.2 V	—	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	—	1	2	kΩ
			—				
			—				
			—				

Notes to Table 4–4:

(1) Typical values are for TA = 25° C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5-, 1.8-, 2.5-, and 3.3-V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3-, 2.5-, 1.8-, and 1.5-V).

(3) This specification is preliminary and pending further device characterization.

(4) Pin pull-up resistor values will lower if an external source drives the pin higher than V_{CCIO}.

(5) Maximum values depend on the actual T_J and design utilization. See the *PowerPlay Early Power Estimator* or the *Quartus II PowerPlay Power Analyzer* feature for maximum values.

I/O Standard Specifications

Tables 4–5 through 4–27 show the HardCopy II device family's I/O standard specifications.

Table 4–5. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output-supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	-0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = -4 mA *(2)*, *(3)*	2.4	—	V

Table 4–5. LVTTL Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*, *(3)*	—	0.45	V

Notes to Table 4–5:
(1) HardCopy II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
(2) Drive strength is programmable according to values in Table 2–10, Table 2–12, and Table 2–14.
(3) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section of volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–6. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output-supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	-0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = -0.1 mA *(2)*, *(3)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*, *(3)*	—	0.2	V

Notes to Table 4–6:
(1) HardCopy II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
(2) Drive strength is programmable according to values in Tables 2–10, 2–12, and 2–14.
(3) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–7. 2.5-V I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output-supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	-0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = -1 mA *(2)*, *(3)*	2.0	—	V

Table 4–7. 2.5-V I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*, *(3)*	—	0.4	V

Notes to Table 4–7:

(1) HardCopy II devices V_{CCIO} voltage-level support of 2.5 ± -5% is narrower than defined in the normal range of the EIA/JEDEC Standard.

(2) Drive strength is programmable according to values in Tables 2–10, 2–12, and 2–14.

(3) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output-supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage	—	-0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = -2 to -8 mA *(2)*, *(3)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(2)*, *(3)*	—	0.45	V

Notes to Table 4–8:

(1) HardCopy II devices V_{CCIO} voltage-level support of 1.8 ± -5% is narrower than defined in the normal range of the EIA/JEDEC Standard.

(2) Drive strength is programmable according to values in Tables 2–10, 2–12, and 2–14.

(3) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–9. 1.5-V I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output-supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	-0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = -2 mA *(2)*, *(3)*	0.75 × V_{CCIO}	—	V

Table 4–9. 1.5-V I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*, *(3)*	—	0.25 × V_{CCIO}	V

Notes to Table 4–9:

(1) HardCopy II devices V_{CCIO} voltage-level support of 1.5 ± -5% is narrower than defined in the normal range of the EIA/JEDEC Standard.

(2) Drive strength is programmable according to values in Tables 2–10, 2–12, and 2–14.

(3) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Figure 4–1 and Figure 4–2 show receiver input and transmitter waveforms, respectively, for all differential I/O LVPECL and HyperTransport technology.

Figure 4–1. Receiver Input Waveforms for Differential I/O Standards

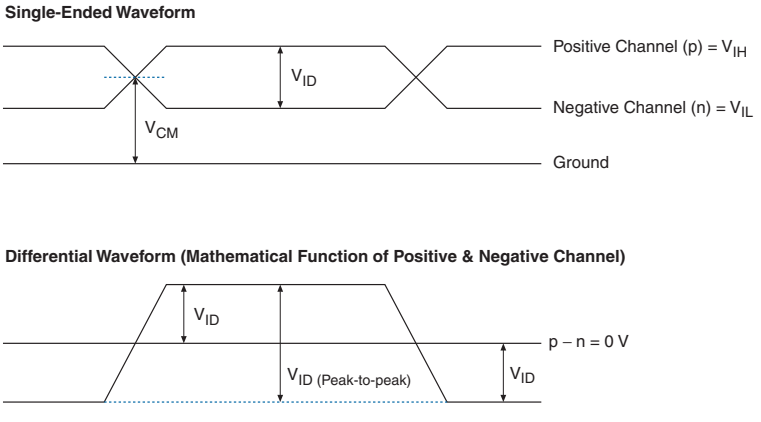


Figure 4–2. Transmiter Output Waveforms for Differential I/O Standards

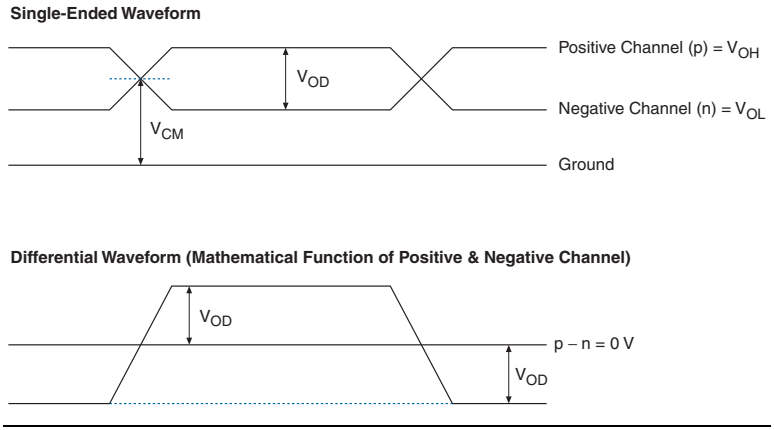


Table 4–10. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for I/O banks that support high-speed IOEs *(1)*, *(2)*	—	2.375	2.5	2.625	V
		—				
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125	—	1.375	V
R_L	Receiver differential input discrete resistor (external to HardCopy II devices)	—	90	100	110	Ω

Notes to Table 4–10:

(1) IOEs = I/O elements.

(2) For information on which I/O banks support high-speed IOEs, refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook*.

Table 4–11. 3.3-V LVDS I/O Specifications *Note (1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output and feedback pins in PLL banks 9, 10, 11, and 12 *(2)*	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	0.84	—	1.570	V
R_L	Receiver differential input discrete resistor (external to HardCopy II devices)	—	90	100	110	Ω

Notes to Table 4–11:

(1) Like Stratix II devices, 3.3-V LVDS is supported by the top and bottom clock input differential buffers, and by the PLL clock output and feedback pins.

(2) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output and feedback differential buffers are powered by `VCC_PLLOUT`. For differential clock output and feedback operation, connect `VCC_PLLOUT` to 3.3 V.

Table 4–12. LVPECL Specifications (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for I/O banks that support high-speed IOEs *(2)*	—	3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)	—	300	600	1,000	mV
V_{ICM}	Input common mode voltage	R_L = 100 Ω	1.0	—	2.5	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	—	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.650	—	2.275	V

Table 4–12. LVPECL Specifications (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_L	Receiver differential input discrete resistor (external to HardCopy II devices)	—	90	100	110	Ω

Notes to Table 4–12:

(1) Like Stratix II devices, LVPECL is supported by the top and bottom clock input differential buffers, and by the PLL clock output and feedback pins.

(2) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output and feedback differential buffers are powered by VCC_PLLOUT. For differential clock output and feedback operation, connect VCC_PLLOUT to 3.3 V.

Table 4–13. HyperTransport Technology Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for I/O banks that support high-speed IOEs *(1), (2)*	—	2.375	2.5	2.625	V
	Output and feedback pins in PLL banks 9, 10, 11, and 12	—	3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)	—	300	600	900	mV
V_{ICM}	Input common mode voltage	—	385	600	845	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	400	600	820	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω	—	—	75	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	440	600	780	V
ΔV_{OCM}	Change in V_{OCM} between high and low	R_L = 100 Ω	—	—	50	mV
R_L	Receiver differential input discrete resistor (external to HardCopy II devices)	—	90	100	110	Ω

Notes to Table 4–13:

(1) For information on which I/O banks support high-speed IOEs, refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook*.

(2) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output and feedback differential buffers are powered by VCC_PLLOUT. For differential clock output and feedback operation, connect VCC_PLLOUT to 3.3 V.

Table 4–14. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	3	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	-0.3	—	0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = -500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 × V_{CCIO}	V

Table 4–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	3	—	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	-0.3	—	0.35 × VCCIO	V
V_{IPU}	Input pull-up voltage	—	0.7 × V_{CCIO}	—	—	V
V_{OH}	High-level output voltage	I_{OUT} = -500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 × V_{CCIO}	V

Table 4–16. SSTL-18 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	VREF	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
$V_{IL(DC)}$	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
$V_{IL(AC)}$	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = -6.7 mA *(1)*, *(2)*	V_{TT} + 0.475	—	—	V

Table 4–16. SSTL-18 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*, *(2)*	—	—	V_{TT} – 0.475	V

Notes to Table 4–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section located in the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook*.

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–17. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
$V_{IL(DC)}$	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
$V_{IL(AC)}$	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = -13.4 mA *(1)*, *(2)*	V_{TT} – 0.28	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*, *(2)*	—	—	0.28	V

Notes to Table 4–17:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section located in the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook*.

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–18. SSTL-18 Differential Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.71	1.8	1.89	V
$V_{SWING(DC)}$	DC differential input voltage	—	0.25	—	—	V

Table 4–18. SSTL-18 Differential Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{X(AC)}$	AC differential input cross point voltage	—	$(V_{CCIO/2}) - 0.175$	—	$(V_{CCIO/2}) + 0.175$	V
$V_{SWING(AC)}$	AC differential input voltage	—	0.5	—	—	V
V_{ISO}	Input clock signal offset voltage	—	—	$0.5 \times V_{CCIO}$	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	—	± 200	—	V
$V_{OX(AC)}$	AC differential cross point voltage	—	$(V_{CCIO/2}) - 0.125$	—	$(V_{CCIO/2}) + 0.125$	V

Table 4–19. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
$V_{IH (DC)}$	High-level input voltage	—	$V_{REF} + 0.18$	—	3.0	V
$V_{IL (DC)}$	Low-level input voltage	—	-0.3	—	$V_{REF} - 0.18$	V
$V_{IH (AC)}$	High-level input voltage	—	$V_{REF} + 0.35$	—	—	V
$V_{IL (AC)}$	Low-level input voltage	—	—	—	$V_{REF} - 0.35$	V
V_{OH}	High-level output voltage	I_{OH} = -8.1 mA *(1)*, *(2)*	$V_{TT} + 0.57$	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*, *(2)*	—	—	$V_{TT} - 0.57$	V

Notes to Table 4–19:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section of the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook.*

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–20. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
$V_{IH\ (DC)}$	High-level input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V
$V_{IL\ (DC)}$	Low-level input voltage	—	-0.3	—	V_{REF} – 0.18	V
$V_{IH\ (AC)}$	High-level input voltage	—	V_{REF} + 0.35	—	—	V
$V_{IL\ (AC)}$	Low-level input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = -16.4 mA *(1)*, *(2)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*, *(2)*	—	—	V_{TT} – 0.76	V

Notes to Table 4–20:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section located in the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook*.

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–21. SSTL-2 Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	2.375	2.5	2.625	V
$V_{SWING\ (DC)}$	DC differential input voltage	—	0.36	—	—	V
$V_{X\ (AC)}$	AC differential input cross point voltage	—	$(V_{CCIO/2})$ – 0.2	—	$(V_{CCIO/2})$ + 0.2	V
$V_{SWING\ (AC)}$	AC differential input voltage	—	0.7	—	—	V
V_{ISO}	Input clock signal offset voltage	—	—	0.5 × V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	—	±200	—	V
$V_{OX\ (AC)}$	AC differential output cross point voltage	—	$(V_{CCIO/2})$ – 0.2	—	$(V_{CCIO/2})$ + 0.2	V

Table 4–22. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.425	1.5	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
$V_{IH\ (DC)}$	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
$V_{IL\ (DC)}$	DC low-level input voltage	—	-0.3	—	V_{REF} – 0.1	V
$V_{IH\ (AC)}$	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
$V_{IL(AC)}$	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*, *(2)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = -8 mA *(1)*, *(2)*	—	—	0.4	V

Notes to Table 4–22:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section located in the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook*.

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–23. 1.5-V HSTL Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.425	1.5	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
$V_{IH\ (DC)}$	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
$V_{IL\ (DC)}$	DC low-level input voltage	—	-0.3	—	V_{REF} – 0.1	V
$V_{IH\ (AC)}$	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
$V_{IL\ (AC)}$	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*, *(2)*	V_{CCIO} – 0.4	—	—	V

Table 4–23. 1.5-V HSTL Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = -16 mA *(1)*, *(2)*	—	—	0.4	V

Notes to Table 4–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown inthe *I/O Structure and Features* section of the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook.*

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–24. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.5	1.575	V
$V_{DIF\ (DC)}$	DC input differential voltage	—	0.2	—	—	V
$V_{CM\ (DC)}$	DC common mode input voltage	—	0.68	—	0.9	V
$V_{DIF\ (AC)}$	AC differential input voltage	—	0.4	—	—	V
$V_{OX\ (AC)}$	AC differential cross point voltage	—	0.68	—	0.9	V

Table 4–25. 1.8-V HSTL Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Input reference voltage	—	0.85	0.9	0.95	V
V_{TT}	Termination voltage	—	0.85	0.9	0.95	V
$V_{IH\ (DC)}$	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
$V_{IL\ (DC)}$	DC low-level input voltage	—	-0.3	—	V_{REF} – 0.1	V
$V_{IH(\ AC)}$	AC high-level input	—	V_{REF} + 0.2	—	—	V
$V_{IL\ (AC)}$	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*, *(2)*	V_{CCIO} – 0.4	—	—	V

Table 4–25. 1.8-V HSTL Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = -8 mA *(1)*, *(2)*	—	—	0.4	V

Notes to Table 4–25:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section located in the *Description, Architecture, and Features* chapter of the *HardCopy Series Devices Handbook*.

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–26. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output-supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Input reference voltage	—	0.85	0.9	0.95	V
V_{TT}	Termination voltage	—	0.85	0.9	0.95	V
$V_{IH\ (DC)}$	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
$V_{IL\ (DC)}$	DC low-level input voltage	—	-0.3	—	V_{REF} – 0.1	V
$V_{IH\ (AC)}$	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
$V_{IL\ (AC)}$	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*, *(2)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OL}= -16 mA *(1)*, *(2)*	—	—	0.4	V

Notes to Table 4–26:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *I/O Structure and Features* section located in the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy Series Devices Handbook*.

(2) Drive strength varies based on pin location. Refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook* for more information.

Table 4–27. 1.8-V Differential HSTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.8	1.89	V
$V_{DIF\ (DC)}$	DC input differential voltage	—	0.2	—	V_{CCIO} + 0.6 V	V
$V_{CM\ (DC)}$	DC common mode input voltage	—	0.78	—	1.12	V

Table 4–27. 1.8-V Differential HSTL Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{DIF\ (AC)}$	AC differential input voltage	—	0.4	—	V_{CCIO} + 0.6 V	V
$V_{OX\ (AC)}$	AC differential cross point voltage	—	0.68	—	0.9	V

Bus Hold Specifications

Table 4–28 shows the HardCopy II device family's bus hold specifications.

Table 4–28. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	25	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	-25	—	-30	—	-50	—	-70	—	µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}	—	-160	—	-200	—	-300	—	-500	µA
Bus-hold trip point	—	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination Specifications

Table 4–29 defines the specification for internal termination specification when using series or differential on-chip termination for HC210W devices only.

Table 4–29. Series On-Chip Termination Specification for I/O Banks Supporting Memory Interface IOEs for HC210W *Notes (1), (2), (3)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25 Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 10	± 15	%
	Internal series termination without calibration (25-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 30	± 30	%
50 Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 10	± 15	%
	Internal series termination without calibration (50-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 30	± 30	%
25 Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 10	± 15	%
	Internal series termination without calibration (25-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 30	± 30	%
50 Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 10	± 15	%
	Internal series termination without calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 30	± 30	%
50 Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.5 V	± 13	± 15	%
	Internal series termination without calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.5 V	± 36	± 36	%

Notes to Table 4–29:

(1) For information on which I/O banks support memory interface IOEs, refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook*.

(2) The resistance tolerances for calibrated SOCT and POCT are at the time of initial of calibration. If the temperature or voltage changes over time, the tolerance may also change.

(3) This table applies only to the HC210W device.

Tables 4–30 and 4–31 define the specification for internal termination specification when using series or differential on-chip termination.

Table 4–30. Series On-Chip Termination Specification for I/O Banks Supporting Memory Interface IOEs
Notes (1), (2), (3)

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25 Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	*± 5*	*± 10*	%
	Internal series termination without calibration (25-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 30	± 30	%
50 Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 5	± 10	%
	Internal series termination without calibration (50-Ω setting)	$V_{CC\ IO}$ = 3.3/2.5 V	± 30	± 30	%
25 Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 5	± 10	%
	Internal series termination without calibration (25-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 30	± 30	%
50 Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 5	± 10	%
	Internal series termination without calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.8 V	± 30	± 30	%
50 Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.5 V	*± 8*	± 10	%
	Internal series termination without calibration (50-Ω setting)	$V_{CC\ IO}$ = 1.5 V	± 36	± 36	%

Notes to Table 4–30:

(1) For information on which I/O banks support memory interface IOEs, refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook.*

(2) The resistance tolerances for calibrated SOCT and POCT are at the time of initial calibration. If the temperature or voltage changes over time, the tolerance may also change.

(3) This table applies only to HC210, HC220, HC230 and HC240 devices.

Table 4–31. Series and Differential On-Chip Termination Specification for I/O Banks Supporting High-Speed and General Purpose IOEs *Notes (1), (3), (4)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25 Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	± 30	± 30	%
50 Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8 V	± 30	± 30	%
50 Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	± 36	± 36	%
R_D *(2)*	Internal differential termination for LVDS or HyperTransport technology	—	± 20	± 25	%

Notes to Table 4–31:

(1) For information on which I/O banks support high-speed IOEs, refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook.*

(2) R_D is only supported on high-speed IOEs.

(3) The resistance tolerances for calibrated SOCT and POCT are at the time of initial calibration. If the temperature or voltage changes over time, the tolerance may also change.

(4) This table applies only to HC210, HC220, HC230, and HC240 devices.

Pin Capacitance

Table 4–32 shows the HardCopy II device family's pin capacitance.

Table 4–32. HardCopy II Device Capacitance *Note (1)* *(Part 1 of 2)*

Symbol	Parameter	HC210W Typical	HC210, HC220, HC230, HC240 Typical	Unit
C_{GPIO}	Input capacitance on I/O pins in I/O banks supporting general-purpose IOEs.	5.7	5.0	pF
C_{MIIO}	Input capacitance on I/O pins in I/O banks supporting memory interface IOEs.	5.7	5.0	pF
C_{HSIO}	Input capacitance on I/O pins in I/O banks supporting high-speed IOEs.	7.2	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins CLK[4..7] and CLK[12..15].	6.0	6.0	pF

Table 4–32. HardCopy II Device Capacitance Note (1) *(Part 2 of 2)*

Symbol	Parameter	HC210W Typical	HC210, HC220, HC230, HC240 Typical	Unit
C_{CLKLR}	Input capacitance on left/right clock inputs CLK0, CLK2, CLK8, CLK10.	4.3	6.1	pF
C_{CLKLR+}	Input capacitance on left/right clock inputs CLK1, CLK3, CLK9, and CLK11.	4.2	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 9, 10, 11, and 12.	6.9	6.7	pF

Note to Table 4–32:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ± 0.5 pF.

Maximum Input Clock Rates

Tables 4–33 and 4–34 show the maximum input clocking rates of HardCopy II I/Os.

Table 4–33. HardCopy II Maximum Input Clock Rates of HC210, HC220, HC230 and HC240 Devices (Part 1 of 2)

I/OStandard	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs	CLK [0..3, 8..11]	CLK [4..7, 12..15]	FPLL_CLK	PLL_FB	Unit
LVTTL	500	500	500	500	500	500	500	MHz
2.5 V	500	500	500	500	500	500	500	MHz
1.8 V	500	500	500	500	500	500	500	MHz
1.5 V	500	500	500	500	500	500	500	MHz
LVCMOS	500	500	500	500	500	500	500	MHz
SSTL2 class I	500	—	—	—	500	—	500	MHz
SSTL2 class II	500	—	—	—	500	—	500	MHz
SSTL18 class I	500	—	—	—	500	—	500	MHz
SSTL18 class II	500	—	—	—	500	—	500	MHz
1.5 V HSTL class I	500	—	—	—	500	—	500	MHz
1.5 V HSTL class II	500	—	—	—	500	—	500	MHz
1.8 V HSTL class I	500	—	—	—	500	—	500	MHz
1.8 V HSTL class II	500	—	—	—	500	—	500	MHz
PCI *(1)*	500	—	500	—	500	—	500	MHz

Table 4–33. HardCopy II Maximum Input Clock Rates of HC210, HC220, HC230 and HC240 Devices (Part 2 of 2)

I/OStandard	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs	CLK [0..3, 8..11]	CLK [4..7, 12..15]	FPLL_CLK	PLL_FB	Unit
PCI-X *(1)*	500	—	500	—	500	—	500	MHz
Differential SSTL2 class I *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
Differential SSTL2 class II *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
Differential SSTL18 class I *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
Differential SSTL18 class II *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
1.8-V Differential HSTL class I *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
1.8-V Differential HSTL class II *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
1.5-V Differential HSTL class I *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
1.5-V Differential HSTL class II *(2)*, *(3)*	500	—	—	—	500	—	500	MHz
LVDS	—	520	—	717	450	717	450	MHz
LVPECL	—	—	—	—	450	—	450	MHz
HyperTransport	—	520	—	717	—	717	—	MHz

Notes to Table 4–33:

(1) The PCI clamping diode is only supported on the top and bottom I/O pins.

(2) This I/O standard is only supported on the DQS, CLK, and PLL_FB input pins.

(3) For HC210 and HC220, differential HSTL/SSTL input is supported on top/bottom PLL_FB, the top clock pins and DQS pins located on the top I/Os.

Table 4–34. **HardCopy II Maximum Input Clock Rates of HC210W Devices** *Note (3)* ***(Part 1 of 2)***

I/O Standard	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs	CLK [0..3, 8..11]	CLK [4..7, 12..15]	FPLL_CLK	PLL_FB	Unit
LVTTL	350	350	350	350	350	350	350	MHz
2.5-V LVTTL/LVCMOS	350	350	350	350	350	350	350	MHz
1.8-V LVTTL/LVCMOS	350	350	350	350	350	350	350	MHz
1.5-V LVTTL/LVCMOS	270	270	270	270	270	270	270	MHz
LVCMOS	350	350	350	350	350	350	350	MHz
SSTL2 class I	350	—	—	—	350	—	350	MHz
SSTL2 class II	350	—	—	—	350	—	350	MHz
SSTL18 class I	350	—	—	—	350	—	350	MHz
SSTL18 class II	350	—	—	—	350	—	350	MHz
1.5-V HSTL class I	350	—	—	—	350	—	350	MHz
1.5-V HSTL class II	350	—	—	—	350	—	350	MHz
1.8-V HSTL class I	350	—	—	—	350	—	350	MHz
1.8-V HSTL class II	350	—	—	—	350	—	350	MHz
PCI *(1)*	315	—	315	—	315	—	315	MHz
PCI-X *(1)*	315	—	315	—	315	—	315	MHz
Differential SSTL2 class I *(2)*	—	—	—	—	350	—	350	MHz
Differential SSTL2 class II *(2)*	—	—	—	—	350	—	350	MHz
Differential SSTL18 class I *(2)*	—	—	—	—	350	—	350	MHz
Differential SSTL18 class II *(2)*	—	—	—	—	350	—	350	MHz
1.8-V differential HSTL class I *(2)*	—	—	—	—	350	—	350	MHz
1.8-V differential HSTL class II *(2)*	—	—	—	—	350	—	350	MHz
1.5-V differential HSTL class I *(2)*	—	—	—	—	350	—	350	MHz
1.5-V differential HSTL class II *(2)*	—	—	—	—	350	—	350	MHz
LVDS	—	320	—	320	320	320	320	MHz
LVPECL	—	—	—	—	320	—	320	MHz

Table 4–34. HardCopy II Maximum Input Clock Rates of HC210W Devices *Note (3)* *(Part 2 of 2)*								
I/O Standard	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs	CLK [0..3, 8..11]	CLK [4..7, 12..15]	FPLL_CLK	PLL_FB	Unit
HyperTransport	—	320	—	320	—	320	—	MHz

Notes to Table 4–34:
(1) The PCI clamping diode is only supported on the top and bottom I/O pins.
(2) For HC210W, differential HSTL/SSTL input is supported on the top clock pins, the DQS pins on the top I/O banks and top/bottom PLL_FB input pins.
(3) These numbers are preliminary and pending further silicon characterization.

Maximum Output Clock Rates

Tables 4–35 and 4–36 show the maximum output toggle rates of HardCopy II I/O's for all available drive strengths.

Table 4–35. HardCopy II Maximum Output Clock Rate of HC210, HC220, HC230 and HC240 Devices *Note (1)* *(Part 1 of 5)*									
I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] *(2)*	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
3.3-V LVTTL	4 mA	225	225	225	225	225	225	225	MHz
	8 mA	355	355	355	355	355	355	355	MHz
	12 mA	475	475	475	475	475	475	475	MHz
	16 mA	594	—	—	—	—	594	594	MHz
	20 mA	700	—	—	—	—	700	700	MHz
	24 mA *(3)*	794	—	—	—	—	794	794	MHz
3.3-V LVCMOS	4 mA	250	250	250	250	250	250	250	MHz
	8 mA	480	480	480	480	480	480	480	MHz
	12 mA	710	—	—	—	—	710	710	MHz
	16 mA	925	—	—	—	—	925	925	MHz
	20 mA	985	—	—	—	—	985	985	MHz
	24 mA *(3)*	1040	—	—	—	—	1040	1040	MHz

Table 4–35. HardCopy II Maximum Output Clock Rate of HC210, HC220, HC230 and HC240 Devices Note (1) (Part 2 of 5)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
2.5-V LVTTL / LVCMOS	4 mA	194	194	194	194	194	194	194	MHz
	8 mA	380	380	380	380	380	380	380	MHz
	12 mA	575	575	575	575	575	575	575	MHz
	16 mA (3)	845	—	—	—	—	845	845	MHz
1.8-V LVTTL / LVCMOS	2 mA	109	109	109	109	109	109	109	MHz
	4 mA	250	250	250	250	250	250	250	MHz
	6 mA	390	390	390	390	390	390	390	MHz
	8 mA	570	570	570	570	570	570	570	MHz
	10 mA	805	—	—	—	—	805	805	MHz
	12 mA (3)	1040	—	—	—	—	1040	1040	MHz
1.5-V LVTTL / LVCMOS	2 mA	200	200	200	200	200	200	200	MHz
	4 mA	370	370	370	370	370	370	370	MHz
	6 mA	430	—	—	—	—	430	430	MHz
	8 mA (3)	495	—	—	—	—	495	495	MHz
SSTL2 class I	8 mA	300	—	—	—	—	300	300	MHz
	12 mA (3)	400	—	—	—	—	400	400	MHz
SSTL2 class II	16 mA	350	—	—	—	—	350	350	MHz
	20 mA	350	—	—	—	—	350	350	MHz
	24 mA (3)	400	—	—	—	—	400	400	MHz
SSTL18 class I	4 mA	150	—	—	—	—	150	150	MHz
	6 mA	250	—	—	—	—	250	250	MHz
	8 mA	300	—	—	—	—	300	300	MHz
	10 mA	400	—	—	—	—	400	400	MHz
	12 mA (3)	550	—	—	—	—	550	550	MHz
SSTL18 class II	8 mA	200	—	—	—	—	200	200	MHz
	16 mA	350	—	—	—	—	350	350	MHz
	18 mA	400	—	—	—	—	400	400	MHz
	20 mA (3)	500	—	—	—	—	500	500	MHz

Table 4–35. HardCopy II Maximum Output Clock Rate of HC210, HC220, HC230 and HC240 Devices Note (1) (Part 3 of 5)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
1.8-V HSTL class I	4 mA	300	—	—	—	—	300	300	MHz
	6 mA	450	—	—	—	—	450	450	MHz
	8 mA	600	—	—	—	—	600	600	MHz
	10 mA	650	—	—	—	—	650	650	MHz
	12 mA (3)	700	—	—	—	—	700	700	MHz
1.8-V HSTL class II	16 mA	500	—	—	—	—	500	500	MHz
	18 mA	500	—	—	—	—	500	500	MHz
	20 mA (3)	550	—	—	—	—	550	550	MHz
1.5-V HSTL class I	4 mA	300	—	—	—	—	300	300	MHz
	6 mA	500	—	—	—	—	500	500	MHz
	8 mA	650	—	—	—	—	650	650	MHz
	10 mA	700	—	—	—	—	700	700	MHz
	12 mA (3)	700	—	—	—	—	700	700	MHz
1.5-V HSTL class II	16 mA	600	—	—	—	—	600	600	MHz
	18 mA	600	—	—	—	—	600	600	MHz
	20 mA (3)	650	—	—	—	—	650	650	MHz
PCI (4)	—	790	—	790	—	—	790	790	MHz
PCI-X (4)	—	790	—	790	—	—	790	790	MHz
LVDS	—	—	717	—	—	—	—	400	MHz
HyperTransport	—	—	717	—	—	—	—	—	MHz
LVPECL	—	—	—	—	—	—	—	400	MHz
Differential SSTL2 class I (5)	8 mA	300	—	—	—	—	300	300	MHz
	12 mA (3)	400	—	—	—	—	400	400	MHz
Differential SSTL2 class II (5)	16 mA	350	—	—	—	—	350	350	MHz
	20 mA (3)	350	—	—	—	—	350	350	MHz
	24 mA (3)	400	—	—	—	—	400	400	MHz

Table 4–35. HardCopy II Maximum Output Clock Rate of HC210, HC220, HC230 and HC240 Devices Note (1) (Part 4 of 5)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
Differential SSTL18 class I (5)	4 mA	150	—	—	—	—	150	150	MHz
	6 mA	250	—	—	—	—	250	250	MHz
	8 mA	300	—	—	—	—	300	300	MHz
	10 mA	400	—	—	—	—	400	400	MHz
	12 mA (3)	550	—	—	—	—	550	550	MHz
Differential SSTL18 class II (5)	8 mA	200	—	—	—	—	200	200	MHz
	16 mA	350	—	—	—	—	350	350	MHz
	18 mA	400	—	—	—	—	400	400	MHz
	20 mA (3)	500	—	—	—	—	500	500	MHz
1.8-V differential HSTL class I (5)	4 mA	300	—	—	—	—	300	300	MHz
	6 mA	450	—	—	—	—	450	450	MHz
	8 mA	600	—	—	—	—	600	600	MHz
	10 mA	650	—	—	—	—	650	650	MHz
	12 mA (3)	700	—	—	—	—	700	700	MHz
1.8-V differential HSTL class II (5)	16 mA	500	—	—	—	—	500	500	MHz
	18 mA	500	—	—	—	—	500	500	MHz
	20 mA (3)	550	—	—	—	—	550	550	MHz
1.5-V differential HSTL class I (5)	4 mA	300	—	—	—	—	300	300	MHz
	6 mA	500	—	—	—	—	500	500	MHz
	8 mA	650	—	—	—	—	650	650	MHz
	10 mA	700	—	—	—	—	700	700	MHz
	12 mA (3)	700	—	—	—	—	700	700	MHz

Table 4–35. HardCopy II Maximum Output Clock Rate of HC210, HC220, HC230 and HC240 Devices Note (1) (Part 5 of 5)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
1.5-V differential HSTL class II (5)	16 mA	600	—	—	—	—	600	600	MHz
	18 mA	600	—	—	—	—	600	600	MHz
	20 mA (3)	650	—	—	—	—	650	650	MHz

Notes to Table 4–35:

(1) The toggle rate applies to 0 pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5 pF.

(2) `CLK [1, 3, 9, 11]` and `FPLL_CLK` are dedicated input clocks, and are excluded from this table.

(3) This is the default setting in the Quartus® II software if supported by the pin location.

(4) The PCI clamping diode is only supported on the top and bottom I/O pins.

(5) Like Stratix II devices, differential HSTL and SSTL is supported only on the column `CLK`, `PLL_OUT` and memory interface `DQS` IOE pins. For HC210 and HC220, only the top column clock pins support Differential HSTL and SSTL.

Table 4–36. HardCopy II Maximum Output Clock Rate for HC210W Devices Notes (1), (6) (Part 1 of 4)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
3.3-V LVTTL	4 mA	100	100	100	100	100	100	100	MHz
	8 mA	170	170	170	170	170	170	170	MHz
	12 mA	230	230	230	230	230	230	230	MHz
	16 mA	240	—	—	—	—	240	240	MHz
	20 mA	280	—	—	—	—	280	280	MHz
	24 mA (3)	300	—	—	—	—	300	300	MHz
3.3-V LVCMOS	4 mA	175	175	175	175	175	175	175	MHz
	8 mA	230	230	230	230	230	230	230	MHz
	12 mA	260	—	—	—	—	260	260	MHz
	16 mA	270	—	—	—	—	270	270	MHz
	20 mA	290	—	—	—	—	290	290	MHz
	24 mA (3)	310	—	—	—	—	310	310	MHz

Table 4–36. HardCopy II Maximum Output Clock Rate for HC210W Devices *Notes (1), (6)* ***(Part 2 of 4)***

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] *(2)*	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
2.5-V LVTTL / LVCMOS	4 mA	136	136	136	136	136	136	136	MHz
	8 mA	230	230	230	230	230	230	230	MHz
	12 mA	370	370	370	370	370	370	370	MHz
	16 mA *(3)*	405	—	—	—	—	405	405	MHz
1.8-V LVTTL / LVCMOS	2 mA	77	77	77	77	77	77	77	MHz
	4 mA	150	150	150	150	150	150	150	MHz
	6 mA	180	180	180	180	180	180	180	MHz
	8 mA	200	200	200	200	200	200	200	MHz
	10 mA	250	—	—	—	—	250	250	MHz
	12 mA *(3)*	290	—	—	—	—	290	290	MHz
1.5-V LVTTL / LVCMOS	2 mA	60	60	60	60	60	60	60	MHz
	4 mA	110	110	110	110	110	110	110	MHz
	6 mA	150	—	—	—	—	150	150	MHz
	8 mA *(3)*	190	—	—	—	—	190	190	MHz
SSTL2 class I	8 mA	210	—	—	—	—	210	210	MHz
	12 mA *(3)*	280	—	—	—	—	280	280	MHz
SSTL2 class II	16 mA	245	—	—	—	—	245	245	MHz
	20 mA	245	—	—	—	—	245	245	MHz
	24 mA *(3)*	280	—	—	—	—	280	280	MHz
SSTL18 class I	4 mA	105	—	—	—	—	105	105	MHz
	6 mA	175	—	—	—	—	175	175	MHz
	8 mA	210	—	—	—	—	210	210	MHz
	10 mA	220	—	—	—	—	220	220	MHz
	12 mA *(3)*	230	—	—	—	—	230	230	MHz
SSTL18 class II	8 mA	140	—	—	—	—	140	140	MHz
	16 mA	220	—	—	—	—	220	220	MHz
	18 mA	220	—	—	—	—	220	220	MHz
	20 mA *(3)*	350	—	—	—	—	350	350	MHz

Table 4–36. HardCopy II Maximum Output Clock Rate for HC210W Devices *Notes (1), (6)* ***(Part 3 of 4)***

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] *(2)*	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
1.8-V HSTL class I	4 mA	210	—	—	—	—	210	210	MHz
	6 mA	210	—	—	—	—	210	210	MHz
	8 mA	220	—	—	—	—	220	220	MHz
	10 mA	250	—	—	—	—	250	250	MHz
	12 mA *(3)*	270	—	—	—	—	270	270	MHz
1.8-V HSTL class II	16 mA	190	—	—	—	—	190	190	MHz
	18 mA	200	—	—	—	—	200	200	MHz
	20 mA *(3)*	210	—	—	—	—	210	210	MHz
1.5-V HSTL class I	4 mA	150	—	—	—	—	150	150	MHz
	6 mA	160	—	—	—	—	160	160	MHz
	8 mA	170	—	—	—	—	170	170	MHz
	10 mA	180	—	—	—	—	180	180	MHz
	12 mA *(3)*	190	—	—	—	—	190	190	MHz
1.5-V HSTL class II	16 mA	170	—	—	—	—	170	170	MHz
	18 mA	170	—	—	—	—	170	170	MHz
	20 mA *(3)*	170	—	—	—	—	170	170	MHz
PCI *(4)*	—	315	—	315	—	—	315	315	MHz
PCI-X *(4)*	—	315	—	315	—	—	315	315	MHz
LVDS	—	—	320	—	—	—	—	280	MHz
HyperTransport	—	—	320	—	—	—	—	—	MHz
LVPECL	—	—	—	—	—	—	—	280	MHz
Differential SSTL2 class I *(5)*	8 mA	210	—	—	—	—	210	210	MHz
	12 mA *(3)*	280	—	—	—	—	280	280	MHz
Differential SSTL2 class II *(5)*	16 mA	245	—	—	—	—	245	245	MHz
	20 mA	245	—	—	—	—	245	245	MHz
	24 mA *(3)*	280	—	—	—	—	280	280	MHz
Differential SSTL18 class I *(5)*	4 mA	105	—	—	—	—	105	105	MHz
	6 mA	175	—	—	—	—	175	175	MHz
	8 mA	210	—	—	—	—	210	210	MHz
	10 mA	220	—	—	—	—	220	220	MHz
	12 mA *(3)*	230	—	—	—	—	230	230	MHz

Table 4–36. HardCopy II Maximum Output Clock Rate for HC210W Devices *Notes (1), (6)* *(Part 4 of 4)*

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] *(2)*	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
Differential SSTL18 class II *(5)*	8 mA	140	—	—	—	—	140	140	MHz
	16 mA	220	—	—	—	—	220	220	MHz
	18 mA	220	—	—	—	—	220	220	MHz
	20 mA *(3)*	220	—	—	—	—	220	220	MHz
1.8-V differential HSTL class I *(5)*	4 mA	210	—	—	—	—	210	210	MHz
	6 mA	210	—	—	—	—	210	210	MHz
	8 mA	220	—	—	—	—	220	220	MHz
	10 mA	250	—	—	—	—	250	250	MHz
	12 mA *(3)*	270	—	—	—	—	270	270	MHz
1.8-V differential HSTL class II *(5)*	16 mA	190	—	—	—	—	190	190	MHz
	18 mA	200	—	—	—	—	200	200	MHz
	20 mA *(3)*	210	—	—	—	—	210	210	MHz
1.5-V differential HSTL class I *(5)*	4 mA	150	—	—	—	—	150	150	MHz
	6 mA	160	—	—	—	—	160	160	MHz
	8 mA	170	—	—	—	—	170	170	MHz
	10 mA	180	—	—	—	—	180	180	MHz
	12 mA *(3)*	190	—	—	—	—	190	190	MHz
1.5-V differential HSTL class II *(5)*	16 mA	170	—	—	—	—	170	170	MHz
	18 mA	170	—	—	—	—	170	170	MHz
	20 mA *(3)*	170	—	—	—	—	170	170	MHz

Notes to Table 4–36:

(1) The toggle rate applies to 0 pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5 pF.

(2) `CLK [1, 3, 9, 11]` and `FPLL_CLK` are dedicated input clocks, and excluded from this table.

(3) This is the default setting in the Quartus II software if supported by the pin location.

(4) The PCI clamping diode is only supported on the top and bottom I/O pins.

(5) Like Stratix II devices, differential HSTL and SSTL is supported only on the column `CLK`, `PLL_OUT` and memory interface `DQS` IOE pins. For HC210 and HC220, only the top column clock pins support Differential HSTL and SSTL.

(6) These numbers are preliminary and pending further silicon characterization.

Tables 4–37 and 4–38 show the maximum output toggle rates of HardCopy II I/Os using OCT.

Table 4–37. HardCopy II Maximum Output Clock Rate for HC210, HC220, HC230 and HC240 Devices (OCT) Note (1) (Part 1 of 2)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
3.3-V LVTTL	OCT 50 Ω	400	400	400	400	400	400	400	MHz
2.5-V LVTTL	OCT 50 Ω	350	350	350	350	350	350	350	MHz
1.8-V LVTTL	OCT 50 Ω	550	550	550	550	550	550	550	MHz
3.3-V LVCMOS	OCT 50 Ω	350	350	350	350	350	350	350	MHz
1.5-V LVCMOS	OCT 50 Ω	450	450	450	450	450	450	450	MHz
SSTL-2 Class I	OCT 50 Ω	500	—	—	—	—	500	500	MHz
SSTL-2 Class II	OCT 25 Ω	550	—	—	—	—	550	550	MHz
SSTL-18 Class I	OCT 50 Ω	400	—	—	—	—	400	400	MHz
SSTL-18 Class II	OCT 25 Ω	500	—	—	—	—	500	500	MHz
1.5-V HSTL Class I	OCT 50 Ω	550	—	—	—	—	550	550	MHz
1.8-V HSTL Class I	OCT 50 Ω	600	—	—	—	—	600	600	MHz
1.8-V HSTL Class II	OCT 50 Ω	500	—	—	—	—	500	500	MHz
Differential SSTL-2 Class I (3)	OCT 50 Ω	500	—	—	—	—	500	500	MHz
Differential SSTL-2 Class II (3)	OCT 25 Ω	550	—	—	—	—	550	550	MHz
Differential SSTL-18 Class I (3)	OCT 50 Ω	400	—	—	—	—	400	400	MHz
Differential SSTL-18 Class II (3)	OCT 25 Ω	500	—	—	—	—	500	500	MHz
1.8-V Differential HSTL Class I (3)	OCT 50 Ω	600	—	—	—	—	600	600	MHz
1.8-V Differential HSTL Class II (3)	OCT 25 Ω	500	—	—	—	—	500	500	MHz

Table 4–37. HardCopy II Maximum Output Clock Rate for HC210, HC220, HC230 and HC240 Devices (OCT) Note (1) (Part 2 of 2)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
1.5-V Differential HSTL Class I (3)	OCT 50 Ω	550	—	—	—	—	550	550	MHz

Notes to Table 4–37:

(1) The toggle rate applies to 0 pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5 pF.

(2) `CLK [1, 3, 9, 11]` and `FPLL_CLK` are dedicated input clocks, and excluded from this table.

(3) Like Stratix II devices, differential HSTL and SSTL is supported only on the column `CLK`, `PLL_OUT` and memory interface `DQS` IOE pins. For HC210 and HC220, only the top column clock pins support Differential HSTL and SSTL.

Table 4–38. HardCopy II Maximum Output Clock Rate for HC210W using OCT Notes (1), (4) (Part 1 of 2)

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] (2)	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
3.3-V LVTTL	OCT 50 Ω	280	280	280	280	280	280	280	MHz
2.5-V LVTTL	OCT 50 Ω	245	245	245	245	245	245	245	MHz
1.8-V LVTTL	OCT 50 Ω	290	290	290	290	290	290	290	MHz
3.3-V LVCMOS	OCT 50 Ω	245	245	245	245	245	245	245	MHz
1.5-V LVCMOS	OCT 50 Ω	190	190	190	190	190	190	190	MHz
SSTL-2 Class I	OCT 50 Ω	280	—	—	—	—	280	280	MHz
SSTL-2 Class II	OCT 25 Ω	280	—	—	—	—	280	280	MHz
SSTL-18 Class I	OCT 50 Ω	230	—	—	—	—	230	230	MHz
SSTL-18 Class II	OCT 25 Ω	220	—	—	—	—	220	220	MHz
1.5-V HSTL Class I	OCT 50 Ω	190	—	—	—	—	190	190	MHz
1.8-V HSTL Class I	OCT 50 Ω	270	—	—	—	—	270	270	MHz
1.8-V HSTL Class II	OCT 50 Ω	210	—	—	—	—	210	210	MHz

Table 4–38. HardCopy II Maximum Output Clock Rate for HC210W using OCT *Notes (1), (4)* *(Part 2 of 2)*

I/O Standard	Drive Strength	Memory Interface IOEs	High Speed IOEs	General Purpose IOEs		CLK [0, 2, 8, 10] *(2)*	CLK [4..7, 12..15]	PLL_OUT	Unit
				Bottom Column	Right Row				
Differential SSTL-2 Class I *(3)*	OCT 50 Ω	280	—	—	—	—	280	280	MHz
Differential SSTL-2 Class II *(3)*	OCT 25 Ω	280	—	—	—	—	280	280	MHz
Differential SSTL-18 Class I *(3)*	OCT 50 Ω	230	—	—	—	—	230	230	MHz
Differential SSTL-18 Class II *(3)*	OCT 25 Ω	220	—	—	—	—	220	220	MHz
1.8-V Differential HSTL Class I *(3)*	OCT 50 Ω	270	—	—	—	—	270	270	MHz
1.8-V Differential HSTL Class II *(3)*	OCT 25 Ω	210	—	—	—	—	210	210	MHz
1.5-V Differential HSTL Class I *(3)*	OCT 50 Ω	190	—	—	—	—	190	190	MHz

Notes to Table 4–38:

(1) The toggle rate applies to 0 pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5 pF.

(2) `CLK [1, 3, 9, 11]` and `FPLL_CLK` are dedicated input clocks, and excluded from this table.

(3) Like Stratix II devices, differential HSTL and SSTL is supported only on the column `CLK`, `PLL_OUT` and memory interface `DQS` IOE pins. For HC210 and HC220, only the top column clock pins support differential HSTL and SSTL.

(4) These numbers are preliminary and pending further silicon characterization.

HighSpeed I/O Specifications

Table 4–39 provides high-speed timing specifications definitions.

Table 4–39. HighSpeed Timing Specifications and Definitions (Part 1 of 2)

HighSpeed Timing Specifications	Definitions
t_C	Highspeed receiver/transmitter input and output clock period.
f_{HSCLK}	Highspeed receiver/transmitter input and output clock frequency.
J	De-serialization factor (width of parallel data bus).

Table 4–39. HighSpeed Timing Specifications and Definitions (Part 2 of 2)

HighSpeed Timing Specifications	Definitions
W	PLL multiplication factor
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = tC/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including tCO variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter (peak-to-peak)	Peak-to-peak input jitter on highspeed PLLs.
Output jitter (peak-to-peak)	Peak-to-peak output jitter on highspeed PLLs.
t_{DUTY}	Duty cycle on highspeed transmitter output clock.
t_{LOCK}	Lock time for highspeed transmitter and receiver PLLs.

Table 4–40 shows the high-speed I/O timing specifications for HC210W F484 WireBond devices.

Table 4–40. HardCopy II High-Speed I/O Specifications for HC210W Device Notes (1), (2) (Part 1 of 2)

Symbol	Conditions	Min	Typ	Max	Unit
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16	—	320	MHz
	W = 1 (SERDES bypass, LVDS only)	16	—	320	MHz
	W = 1 (SERDES used, LVDS only)	150	—	320	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150	—	640	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*	—	640	Mbps
	J = 1 t(LVDS only)	*(4)*	—	320	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150	—	640	Mbps
TCCS	All differential standards	—	—	240	ps
SW	All differential standards	400	—	—	ps
Output jitter	—	—	—	*(5)*	ps

Table 4–40. HardCopy II High-Speed I/O Specifications for HC210W Device Notes (1), (2) (Part 2 of 2)

Symbol	Conditions			Min	Typ	Max	Unit
Output t_{RISE}	All differential I/O standards			—	—	(5)	ps
Output t_{FALL}	All differential I/O standards			—	—	(5)	ps
t_{DUTY}	—	—	—	45	50	55	%
DPA run length	—	—	—	—	—	6,400	UI
DPA jitter tolerance (peak-to-peak)	—	—	—	(5)	—	—	UI
DPA lock time	Standard	Training Pattern	Transition Density	—	—	—	Number of repetitions
	—	—	—	—	—	—	
	SPI4	0000000000 1111111111	10%	(5)	—	—	
	Parallel Rapid I/O	10010000	25%	(5)	—	—	
	—	10010000	50%	(5)	—	—	
	Miscellaneous	10101010	100%	(5)	—	—	
	—	10101010	—	(5)	—	—	

Notes to Table 4–40:

(1) These numbers are preliminary and pending further silicon characterization.
(2) When J = 4 to 10, the SERDES block is used.
When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 640.
(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.
(5) Contact the Altera Applications Group for more information.

Table 4–41 shows the high-speed I/O timing specifications for HC210, HC220, HC230 and HC240 HardCopy II devices.

Table 4–41. HardCopy II High-Speed I/O Specifications for HC210, HC220, HC230 and HC240 Devices Note (1) (Part 1 of 2)

Symbol	Conditions	Min	Typ	Max	Unit
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) (2)	16	—	520	MHz
	W = 1 (SERDES bypass, LVDS only)	16	—	500	MHz
	W = 1 (SERDES used, LVDS only)	150	—	717	MHz

Table 4–41. **HardCopy II High-Speed I/O Specifications for HC210, HC220, HC230 and HC240 Devices** *Note (1)* ***(Part 2 of 2)***

Symbol	Conditions			Min	Typ	Max	Unit
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150	—	1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(3)*	—	760	Mbps
	J = 1 (LVDS only)			*(3)*	—	500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150	—	1,040	Mbps
TCCS	All differential standards			—	—	200	ps
SW	All differential standards			330	—	—	ps
Output jitter	—			—	—	190	ps
Output t_{RISE}	All differential I/O standards			—	—	160	ps
Output t_{FALL}	All differential I/O standards			—	—	180	ps
t_{DUTY}	—			45	50	55	%
DPA run length	—			—	—	6,400	UI
DPA jitter tolerance (peak-to-peak)	—			0.44	—	—	UI
DPA lock time	Standard	Training Pattern	Transition Density	—	—	—	Number of repetitions
	—	—	—	—	—	—	
	SPI4	0000000000 1111111111	10%	256	—	—	
	Parallel Rapid I/O	10010000	25%	256	—	—	
	—	10010000	50%	256	—	—	
	Miscellaneous	10101010	100%	256	—	—	
	—	10101010	—	256	—	—	

Notes to Table 4–41:

(1) When J = 4 to 10, the SERDES block is used.
When J = 1 or 2, the SERDES block is bypassed.

(2) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤1,040.

(3) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.

PLL Timing Specifications

Tables 4–42 and 4–43 describe the HardCopy II PLL specifications when operating in both the commercial junction temperature range (0° to 85° C) and the industrial junction temperature range (–40° to 100° C), except for the clock switchover feature. Like the Stratix II devices, the clock switchover feature is only supported from the 0° to 100° C junction temperature range.

Table 4–42. HardCopy II Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency for HC210, HC220, HC230 and HC240 devices	2	—	500	MHz
	Input clock frequency for the HC210W device	2	—	320 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	2	—	420	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤ 0.85 MHz	—	0.5	—	ns (pp)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz	—	1	—	ns (pp)
$t_{OUTJITTER}$	Dedicated clock output period jitter for HC210, HC220, HC230 and HC240 devices	—	—	250 ps for ≥ 100 MHz outclk 25 mUI for < 100 MHz outclk	ps or mUI
	Dedicated clock output period jitter for HC210W device	—	—	300 ps for ≥ 100 MHz outclk 30 mUI for < 100 MHz outclk	ps or mUI
t_{FCOMP}	External feedback compensation time	—	—	10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*	—	550	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%).	45	50	55	%
$f_{SCANCLK}$	Scanclk frequency	—	—	100	MHz
$t_{CONFIGEPLL}$	Time required to reconfigure scan chains for enhanced PLLs	—	$174/f_{SCANCLK}$	—	ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*	—	*(1)*	MHz

Table 4–42. HardCopy II Enhanced PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Unit
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of device configuration	—	0.03	1	ms
t_{DLOCK}	Time required for the PLL to lock dynamically after automatic clock switchover between two identical clock frequencies	—	—	1	ms
$f_{SWITCHOVER}$	Frequency range where the clock switchover performs properly	4	—	500	MHz
f_{CLKW}	PLL closed loop bandwidth	0.13	1.2	16.9	MHz
f_{VCO}	PLL VCO operating range for HC210, HC220, HC230 and HC240 devices	300	—	1,040	MHz
	PLL VCO operating range for HC210W devices	300	—	840	MHz
f_{SS}	Spread spectrum modulation frequency	100	—	500	MHz
% spread	Percent down spread for a given clock frequency	0.4	0.5	0.6	%
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 15	ps
t_{ARESET}	Minimum pulse width on ARESET signal.	10 *(3)*	—	—	ns
		500 *(4)*	—	—	ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scan done goes high.	500	—	—	ns

Notes to Table 4–42:

(1) Limited by I/O f_{MAX}.

(2) If the counter cascading feature of the PLL is used, there is no minimum output clock frequency.

(3) Applicable when the PLL input clock has been running continuously for at least 10 µs.

(4) Applicable when the PLL input clock has stopped toggling or has been running continuously for less than 10 µs.

Table 4–43. HardCopy II Fast PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency for HC210, HC220, HC230 and HC240 devices	16	—	717	MHz
	Input clock frequency for the HC210W device	16	—	320 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	16	—	500	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz	—	0.5	—	ns (pp)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz	—	1	—	ns (pp)
f_{VCO}	Upper VCO frequency range for HC210, HC220, HC230 and HC240 devices	300	—	1,040	MHz
	Upper VCO frequency range for HC210W devices	300	—	840	MHz
	Lower VCO frequency range for HC210, HC220, HC230 and HC240 devices	150	—	520	MHz
	Lower VCO frequency range for HC210W device	150	—	420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875	—	550	MHz
	PLL output frequency to LVDS or DPA clock for HC210, HC220, HC230 and HC240 devices	150	—	1,040	MHz
	PLL output frequency to LVDS or DPA clock for HC210W devices	150	—	840	MHz
f_{OUT_IO}	PLL clock output frequency to regular I/O pin	4.6875	—	*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs	—	$75/f_{SCANCLK}$	—	ns
f_{CLBW}	PLL closed loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration	—	0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns

Table 4–43. HardCopy II Fast PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Unit
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scan done goes high.	500	—	—	ns

Note to Table 4–43:
(1) Limited by I/O f_{MAX}.

External Memory Interface Specifications

Table 4–44 summarizes the maximum clock rate that HardCopy II devices can support with external memory devices.

Table 4–44. HardCopy II Maximum Clock Rate Support for External Memory Interfaces Note (1)

Memory Standards	HardCopy II Device				Unit
	Wire Bond Package HC210W *(2)*		Flip Chip Package HC210 / HC220 / HC230 / HC240 *(3)*		
	Com (C)	Ind (I)	Com (C)	Ind (I)	
DDR	150	133	200	200	MHz
DDR2 *(7)*	150	133	267	233	MHz
QDRII *(6)*	150	133	250	233 *(5)*	MHz
RLDRAMII *(6)*	150	133	250 *(4)*	*233 (4)*	MHz

Notes to Table 4–44:
(1) HardCopy II devices do not support PLL-based external memory interface except for SDR SDRAMs which do not require the DLL.
(2) HC210W supports memory interface on the top I/O banks.
(3) HC210 and HC220 support memory interface on the top I/O banks. HC230 and HC240 support memory interface on the top and bottom I/O banks.
(4) You will need to under-clock a 300 MHz memory device.
(5) You will need to under-clock a 250 MHz memory device.
(6) Based on a DDIO scheme with the 1.8-V HSTL I/O standard.
(7) Based on the PLL dedicated scheme. Use the same F_{MAX} specification for Static-PHY and Auto-PHY since the write-side is limited by the new tDS/tH specification.

Tables 4–45 through 4–51 contain HardCopy II device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–45. DLL Frequency Range Specifications

Frequency Mode	Frequency Range	Resolution (Degrees)
0	100 to 175	30
1	150 to 230	22.5
2	200 to 310	30
3	240 to 350	36

Table 4–46 lists the maximum delay in the fast timing model for the HardCopy II DQS delay buffer. Multiply the number of delay buffers that you are using in the DQS logic block to get the maximum delay achievable in your system. For example, if you implement a 90° phase shift at 200 MHz, you use three delay buffers in mode 2. The maximum achievable delay from the DQS block is then 3 × .416 ps = 1.248 ns.

Table 4–46. DQS Delay Buffer Maximum Delay in Fast Timing Model

DLL Frequency Mode	Maximum Delay Per Delay Buffer	Unit
0	0.833	ns
1, 2, 3	0.416	ns

Table 4–47. DQS Period Jitter Specifications for DLL-Delayed Clock (tDQS_JITTER) Note (1)

Number of DQS Delay Buffer Stages *(2)*	Commercial	Industrial	Unit
1	80	110	ps
2	110	130	ps
3	130	180	ps
4	160	210	ps

Notes to Table 4–47:
(1) Peak-to-peak period jitter on the phase shifted DQS clock.
(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 4–48. DQS Phase Jitter Specifications for DLL-Delayed Clock (tDQS PHASE_JITTER) *Note (1)*		
Number of DQS Delay Buffer Stages *(2)*	**DQS Phase Jitter**	**Unit**
1	30	ps
2	60	ps
3	90	ps
4	120	ps

Notes to Table 4–48:
(1) Peak-to-peak phase jitter on the phase shifted DDS clock (digital jitter is caused by DLL tracking).
(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 4–49. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (tDQS_PSERR) *Note (1)*		
Number of DQS Delay Buffer Stages *(2)*)	**HC210, HC220, HC230 HC240**	**Unit**
1	30	ps
2	60	ps
3	90	ps
4	120	ps

Notes to Table 4–49:
(1) This error specification is the absolute maximum and minimum error. For example, skew on three delay buffer stages with an HC240 device is 105 ps or ± 52.5 ps.
(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 4–50. DQS Bus Clock Skew Adder Specifications (tDQS_CLOCK_SKEW_ADDER) Note (1)

Mode	DQS Clock Skew Adder	Unit
×4 DQ per DQS	40	ps
×9 DQ per DQS	70	ps
×18 DQ per DQS	75	ps
×36 DQ per DQS	95	ps

Note to Table 4–50:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×4 DQ group is 40 ps or ± 20 ps.

Table 4–51. DQS Phase Offset Delay Per Stage Note (1)

HardCopy II Devices	Min	Max	Unit
All	9	14	ps

Note to Table 4–51
(1) The delay settings are linear. The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3. The typical value equals the average of the minimum and maximum values.

Hot Socketing

HardCopy II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a HardCopy II device in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature in HardCopy II devices allow:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up, so they do no disrupt bus operation when HardCopy II I/Os are inserted in the system.
- Signal pins do not drive the V_{CCIO}, V_{CCPD}, or V_{CCINT} power supplies.
- External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

In a hot socketing situation, a device's output buffers are turned off during system power-up or power-down. To simplify board design, HardCopy II devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}). For mixed-voltage environments, you can drive signals into the device before or during power-up or power-down without damaging the device.

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms. All VCC supplies must power down within 100 ms of each other to prevent the I/O pins from driving out. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

- The hot socketing DC specification is $| I_{IOPIN} | < 300$ µA.
- The hot socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

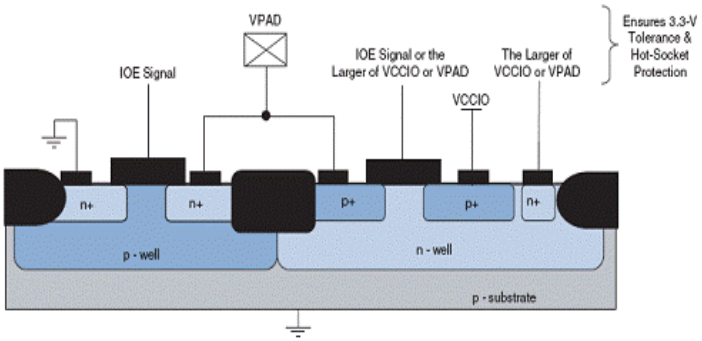
The DC specification applies when all VCC supplies to the device are stable in the powered-up or powered-down conditions. The AC specification applies when the device is being powered up or powered down in any of the conditions mentioned above.

Electrostatic Discharge

Electrostatic discharge (ESD) protection is a design practice that is integrated in Altera FPGAs and structured ASIC devices. HardCopy II devices are no exception, and they are designed with ESD protection on all I/O and power pins.

Figure 4–3 shows a typical HardCopy II CMOS I/O buffer structure which will be used to explain ESD protection.

Figure 4–3. Transistor-Level Diagram of HardCopy II Device I/O Buffers

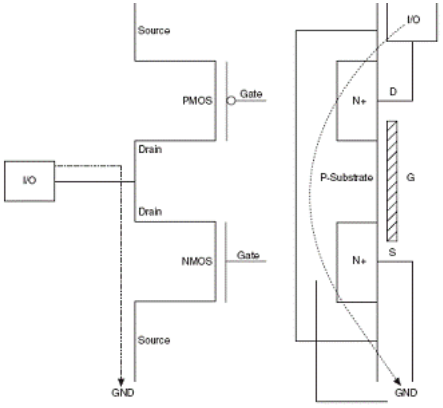


The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/PSubstrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turns on to discharge ESD current from I/O pin to GND.

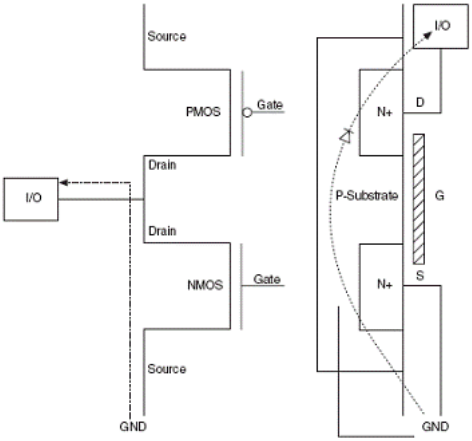
The dashed line (see Figure 4–4) shows the ESD current discharge path during a positive ESD zap.

Figure 4–4. ESD Protection During Positive Voltage Zap



When the I/O pin receives a negative ESD zap at the pin that is less than -0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Hence, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–5.

Figure 4–5. ESD Protection During Negative Voltage Zap



Details of ESD protection are also outlined in the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices* white paper located on the Altera website at www.altera.com.

For information on ESD results of Altera products, please see the Reliability Report on the Altera website at www.altera.com.

Document Revision History

Table 4–52 shows the revision history for this chapter.

Table 4–52. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
September 2008, v3.3	Updated chapter number and metadata.	—
September 2007 v3.2	• Updated Table 4–33 and Table 4–34. • Updated drive strength value in Table 4–36. • Changed f_{IN} and f_{INPFD} from 4 to 2 MHz in Table 4–42. • Added industrial values to Table 4–44.	Minor updates to correct information in tables.
June 2007 v3.1	• Changed V to V_{IH} in Table 4–16 • Updated data for V_{IH} in Table 4–17 • Added Table 4–29 • Updated Table 4–44	—
December 2006 v3.0	Major updates with new electrical characterization data • Updated data in Table 4–1, Table 4–3, Table 4–4, Table 4–5,Table 4–10, Table 4–12, Table 4–13, Table 4–19, Table 4–20, Table 4–27 to Table 4–31. Added Table 4–11 and Tables 4–36 to Table 4–50. • Merged Tables 4–27 to Table 4–32 into new Tables 4–32 to Table 4–33. • Merged Tables 4–33 to Table 4–36 into new Tables 4–34 to Table 4–35. • Added revision history	A major update to the chapter due to new electrical characterization data availability.
October 2005, v2.1	Updated graphics.	—
May 2005, v2.0	Updated various tables throughout chapter.	—
January 2005 v1.0	Added document to the HardCopy Series Handbook.	—