8. Migrating Stratix II Device Resources to HardCopy II Devices

H51024-1.4

Introduction

Altera® HardCopy® II devices and Stratix® II devices are both manufactured on a 1.2-V, 90-nm process technology and offer many similar features. Designers can use the Quartus® II software to migrate their Stratix II design to a HardCopy II device. The Quartus II software ensures that the design revision targeting a HardCopy II device retains the same functionality as the original Stratix II design.

Beginning with version 5.0 of the Quartus II software, you can select a HardCopy II companion device from the **Device Settings** dialog box (Device menu). Selecting a HardCopy II device as a companion device is similar to adding another Stratix II device in the migration device chain. The Quartus II software compiles the design to use the common resources available in all of the selected Stratix II devices and the selected HardCopy II devices. The HardCopy II companion device becomes the target device when you switch to the HardCopy II flow from this Stratix II flow later in the Quartus II project compilation.

For more information on compiling with Stratix II and HardCopy II companion revisions using Quartus II software, refer to the *Quartus II Support for HardCopy II Devices* chapter of the *HardCopy Series Devices Handbook*.

When you select a HardCopy II companion device, you can set the Quartus II Compiler to limit the design to the minimum resource availability of memory blocks and available logic for digital signal processing (DSP) from either the targeted Stratix II or HardCopy II companion device. Additional limitations also include I/O pin assignments and phase-locked loops (PLLs). This document is a guide for designers migrating Stratix II designs into HardCopy II devices. This document highlights resources that are not supported by the selected Stratix II and HardCopy II companion device pair or any resource differences between Stratix II devices and the HardCopy II device.

This document includes the following topics:

- Stratix II and HardCopy II Migration Options
- I/O Support and Planning
- External Memory Interface Support
- On-Chip Termination
- Stratix II and HardCopy II Companion Memory Blocks
- PLL Planning and Utilization

- Global and Local Signals
- Stratix II ALM Adaptation into HardCopy II Logic
- HardCopy II DSP Implementation from Stratix II DSP Blocks
- JTAG BST and Extended Functions
- Power Up and Configuration Compatibility

Stratix II and HardCopy II Migration Options

The Quartus II software allows you to migrate between different Stratix II devices in the same package. When compiling Stratix II designs in the Quartus II software, you can specify one Stratix II target device and one or more Stratix II migration devices. When you specify at least one migration device, the Quartus II Compiler constrains the overall design's I/O pins and other resource assignments to the minimum resources available in any of the selected migration devices. This feature allows vertical migration between devices using the same package footprint. To create the proper configuration file for one of the Stratix II devices selected in the migration devices menu, select that device as a target device.

The introduction of HardCopy II provides an additional seamless migration path for Stratix II devices. After you select a particular Stratix II device, the Quartus II software provides migration options in the **Settings** dialog box. For example, if your design targets the EP2S130 device in the 1,020-pin FineLine BGA® package, the Quartus II software provides the EP2S90 and EP2S180 devices in the 1,020-pin FineLine BGA package as migration options as well as the HC230 device in the 1,020-pin FineLine BGA package.

Conversely, the HardCopy II architecture allows you to design a structured ASIC and then prototype with a wide range of Stratix II devices. If the target device is a HardCopy II HC220 device in the 780-pin FineLine BGA package, you can select the Stratix II EP2S90 or EP2S130 device in the 780-pin FineLine BGA package as prototype devices. Table 8–1 shows vertical migration options by package.

Table 8–1. Stratix II and HardCopy II Migration Options *Note (1)*						
Device	**FineLine BGA Package**					
	484 Pins	**672 Pins**	**780 Pins**	**1,020 Pins**	**1,020 Pins**	**1,508 Pins**
HardCopy II	HC210	HC220	HC220	HC230	HC240	HC240
Stratix II	EP2S30 EP2S60 EP2S90*(2)*	EP2S60	EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180	EP2S180

Notes to Table 8–1:

(1) Table 8–1 does not include the HC210W device. For information on the HC210W device, contact the Altera Applications Group.

(2) This is a Hybrid FineLine BGA package. For more details, refer to the *Package Information for Stratix II Devices* chapter in volume 2 of the *Stratix Device Handbook*.

Beginning with version 5.0 of the Quartus II software, when you compile a design targeting a HardCopy II device, you will need to select a target Stratix II device and a HardCopy II companion device for compilation. Table 8–2 lists the available HardCopy II and Stratix II companion pairs. These pairs are retained in most resource availability tables in this chapter to show the maximum resources available that are supported by either device of the companion pair.

Table 8–2. Stratix II and HardCopy II Companion Devices (Part 1 of 2) *Note (1)*		
Package	**Companion Pair**	
	HardCopy II Device	**Stratix II Device**
484-pin FineLine BGA	HC210	EP2S30
484-pin FineLine BGA	HC210	EP2S60
484-pin Hybrid FineLine BGA	HC210	EP2S90*(2)*
672-pin FineLine BGA	HC220	EP2S60
780-pin FineLine BGA	HC220	EP2S90
780-pin FineLine BGA	HC220	EP2S130
1,020-pin FineLine BGA	HC230	EP2S90
1,020-pin FineLine BGA	HC230	EP2S130

Table 8–2. Stratix II and HardCopy II Companion Devices (Part 2 of 2) Note (1)

Package	Companion Pair	
	HardCopy II Device	Stratix II Device
1,020-pin FineLine BGA	HC230	EP2S180
1,020-pin FineLine BGA	HC240	EP2S180
1,508-pin FineLine BGA	HC240	EP2S180

Notes to Table 8–2:

(1) Table 8–2 does not include the HC210W device. For information on the HC210W device, contact the Altera Applications Group.

(2) This is a Hybrid FineLine BGA package. For more details, refer to the *Package Information for Stratix II Devices* chapter in volume 2 of the *Stratix Device Handbook*.

When the Quartus II software successfully compiles a design, the HardCopy II Device Resource Guide in the Fitter Compilation Report contains information on migration compatibility to a HardCopy II device. Use this information to select the optimal HardCopy II device for the prototype Stratix II device based on resource requirements and package preference.

Table 8–3 shows the available resources for prototyping on a Stratix II device when choosing a HardCopy II device. This chapter examines each resource availability in greater detail.

Table 8–3. Stratix II and HardCopy II Companion Devices Resource Availability Guide (Part 1 of 2) Note (1)

Stratix II and HardCopy II Companion Devices	Package	Stratix II ALMs (2)	HardCopy II Prototyping Resources						
			ASIC Gates for Logic	User I/O Pins (3)	M4K Blocks	M-RAM Blocks	Total RAM Bits	18 × 18 Multipliers	PLLs
EP2S30 HC210	484-pin FineLine BGA	13,552	360K	334	144	0	663,552	64	4
EP2S60 HC210	484-pin FineLine BGA	24,176	720K	334	190	0	875,520	144	4
EP2S90 HC210	484-pin FineLine BGA	36,384	1 M	308	190	0	875,520	192	4
EP2S60 HC220	672-pin FineLine BGA	24,176	720K	492	255	2	2,354,688	144	4
EP2S90 HC220	780-pin FineLine BGA	36,384	1 M	494	408	2	3,059,712	192	4

Table 8–3. Stratix II and HardCopy II Companion Devices Resource Availability Guide (Part 2 of 2) Note (1)

Stratix II and HardCopy II Companion Devices	Package	Stratix II ALMs (2)	HardCopy II Prototyping Resources						
			ASIC Gates for Logic	User I/O Pins (3)	M4K Blocks	M-RAM Blocks	Total RAM Bits	18 × 18 Multipliers	PLLs
EP2S130 HC220	780-pin FineLine BGA	53,016	1.6 M	494	408	2	3,059,712	252	4
EP2S90 HC230	1,020-pin FineLine BGA	36,384	1 M	698	408	4	4,239,360	192	8
EP2S130 HC230	1,020-pin FineLine BGA	53,016	1.6 M	698	609	6	6,345,216	252	8
EP2S180 HC230	1,020-pin FineLine BGA	71,760	2.2 M	698	614	6	6,368,256	384	8
EP2S180 HC240	1,020-pin FineLine BGA	71,760	2.2 M	742	768 (4)	9	8,847,360	384	12
EP2S180 HC240	1,508-pin FineLine BGA	71,760	2.2 M	951	768 (4)	9	8,847,360	384	12

Notes to Table 8–3:

(1) Table 8–3 does not include the HC210W device. For information on the HC210W device, contact the Altera Applications Group.
(2) ALM: adaptive logic module.
(3) User I/O pin counts are preliminary. The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not included in this pin count.
(4) The total number of usable M4K blocks is limited to 768 to allow migration compatibility when prototyping with an EP2S180 device.

I/O Support and Planning

HardCopy II companion devices offer pin-to-pin compatibility with the Stratix II prototype device, which makes them drop-in replacements for the FPGAs. Therefore, you can use HardCopy II devices with the same system board and software developed for prototyping and field trials, enabling the fastest time-to market for high-volume production.

HardCopy II devices offer up to 951 user I/O pins. Table 8–4 lists all available I/O pin counts when assigning a Stratix II device while selecting a HardCopy II companion device. If a Stratix II design uses I/O pins that are not available in both the Stratix II device and the HardCopy II companion device, the Quartus II software issues a no-fit error. Therefore, it is important to monitor pin assignments based on the Stratix II device and the HardCopy II companion device.

Table 8–4. Package Options and I/O Pin Counts for Stratix II and HardCopy II Companion Devices Notes (1), (2)

Stratix II Device	HC210	HC220		HC230 (3)	HC240 (4)	
	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S30	334					
EP2S60	334	492				
EP2S90	308		494	698		
EP2S130			494	698		
EP2S180				698	742	951

Notes to Table 8–4:

(1) User I/O pin counts are preliminary. The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not included in this pin count. The `PLL_ENA` pin is not available as a general purpose I/O pin and can only be used to enable the PLLs in this device.

(2) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(3) The I/O pin counts for all HC230 combinations include four dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`) that can be used for data inputs.

(4) The I/O pin counts for HC240 combinations include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

HardCopy II devices offer three distinct types of I/O elements (IOEs) which support a variety of I/O features to match Stratix II IOEs. These are memory interface IOEs, high-speed IOEs, and general purpose IOEs.

Memory interface IOEs support popular I/O standards used by external memory devices, including single-ended standards from LVTTL, LVCMOS to SSTL, and HSTL voltage referenced (V_{REF}) type I/O standards. Memory interface IOEs also have PCI clamp circuitry for PCI support.

High-speed IOEs support differential applications utilizing LVDS and HyperTransport technology. High-speed IOEs also support single-ended LVTTL and LVCMOS I/O standards, but do not support V_{REF} I/O standards.

General purpose IOEs support LVTTL and LVCMOS I/O standards. General purpose IOEs on the bottom I/O banks (banks 7 and 8) also have PCI clamping circuitry to support the PCI interface on HardCopy II devices.

For more information on HardCopy II IOEs, refer to the *HardCopy II Description, Architecture, and Features* chapter of the *HardCopy Series Handbook*.

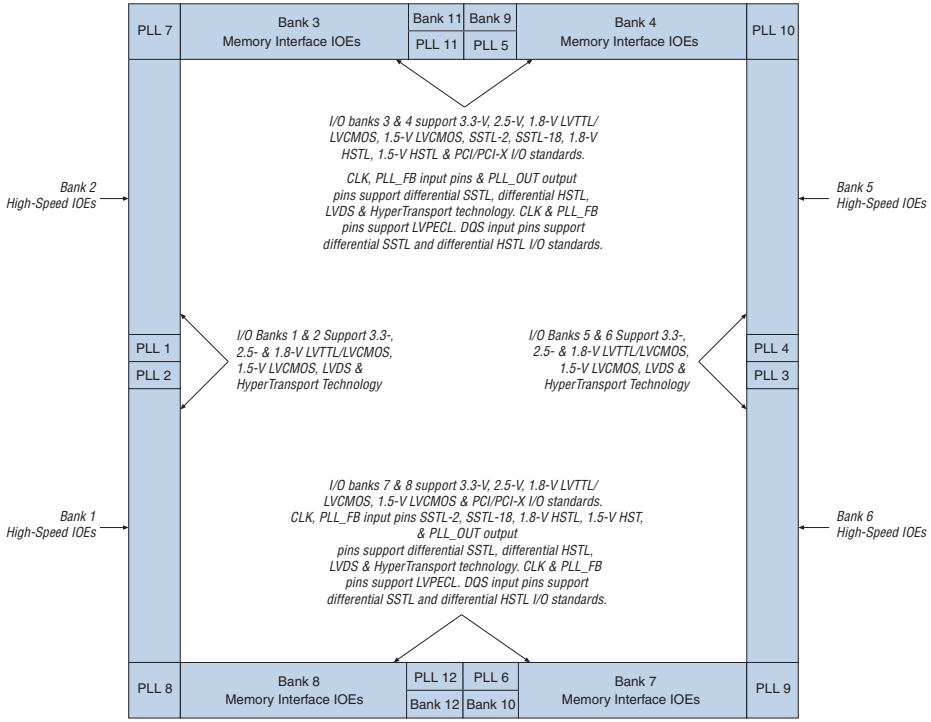
HardCopy II I/O Banks

HardCopy II devices have eight general I/O banks and up to four enhanced PLL external clock output banks (banks 9, 10, 11, 12). HC210 and HC220 devices only have PLL output banks 9 and 10. Figure 8–1 shows the HardCopy II I/O banks and the relative PLL positions.

The left side I/O banks 1 and 2 are high speed IOE banks on all HardCopy II devices. The right side I/O banks 5 and 6 are general purpose IOEs on HC210, HC220, and HC230 devices, but high speed IOEs on HC240 devices.

The top I/O banks 3 and 4 are memory interface IOEs on all HardCopy II devices. The bottom I/O banks 7 and 8 are general purpose IOEs on HC210 and HC220 but memory interface IOEs on HC230 and HC240 devices. The general purpose IOEs on the bottom of the device support PCI clamping, but the general purpose IOEs on the right side do not.

Figure 8–1. HardCopy II HC240 I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 8–1:

(1) Figure 8–1 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only. Refer to the pin list and Quartus II software for exact locations.

(2) Differential HSTL and differential SSTL standards are available for bidirectional operations on DQS pin and input only operations on PLL clock input pins; LVDS, LVPECL, and HyperTransport standards are available for input only operations on PLL clock input pins. Refer to "Differential I/O Termination" on page 8–20 for more details.

(3) HardCopy II devices and the Quartus II software does not support differential SSTL and differential HSTL standards at left and right I/O banks. Side I/O banks do not have V_{REF} pins.

(4) Figure 8–1 shows the HC240 device. Other HardCopy II devices have fewer PLL blocks.

User I/O Count Per IOE Type and Bank Location

Table 8–5 lists the maximum I/O count per IOE type. This helps you select a HardCopy II device based on the I/O standard support requirement.

Table 8–5. HardCopy II Maximum User I/O Count Per IOE Type *Notes (1), (2)*

Device	Package	Memory Interface IOEs		General Purpose IOEs		High-Speed IOEs	
		Top	Bottom	Right	Bottom	Left	Right
HC210	484-pin FineLine BGA	87		84	79	84	
HC220	672-pin FineLine BGA	126		124	118	124	
HC220	780-pin FineLine BGA	126		124	120	124	
HC230 *(3)*	1,020-pin FineLine BGA	180	178	152		188	
HC240 *(4)*	1,020-pin FineLine BGA	184	182			188	188
HC240 *(4)*	1,508-pin FineLine BGA	238	233			240	240

Notes to Table 8–5:

(1) User I/O pin counts are preliminary. The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not included in this pin count. The `PLL_ENA` pin is not available as a general purpose I/O pin and can only be used to enable the PLLs in this device.

(2) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(3) The I/O pin counts for all HC230 combinations include four dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`) that can be used for data inputs.

(4) The I/O pin counts for HC240 combinations include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

HardCopy II Supported I/O Standards

Table 8–6 lists I/O standards that HardCopy II devices supports, separated by IOE type. This list only focuses on user I/O pins.

Table 8–6. Hardcopy II Supported I/O Standards on User I/O Pins (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level (V)		Memory Interface IOEs	General Purpose IOEs	High-Speed IOEs
		Input	Output			
3.3-V LVTTL/LVCMOS	Single-ended	3.3/2.5	3.3	✓	✓	✓
2.5-V LVTTL/LVCMOS	Single-ended	3.3/2.5	2.5	✓	✓	✓
1.8-V LVTTL/LVCMOS	Single-ended	1.8/1.5	1.8	✓	✓	✓
1.5-V LVCMOS	Single-ended	1.8/1.5	1.5	✓	✓	✓

Table 8–6. Hardcopy II Supported I/O Standards on User I/O Pins (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level (V)		Memory Interface IOEs	General Purpose IOEs	High-Speed IOEs
		Input	Output			
SSTL-2 class I and II	Voltage referenced	2.5	2.5	✓		
SSTL-18 class I and II	Voltage referenced	1.8	1.8	✓		
1.8-V HSTL class I and II	Voltage referenced	1.8	1.8	✓		
1.5-V HSTL class I and II	Voltage referenced	1.5	1.5	✓		
PCI / PCI-X	Single-ended	3.3	3.3	✓	*(1)*	
Differential SSTL-2 class I and II input	Pseudo differential *(3)*	3.3/2.5/ 1.8/1.5		*(2)*		
Differential SSTL-2 class I and II output	Pseudo differential *(3)*		2.5	*(2)*		
Differential SSTL-18 class I and II input	Pseudo differential *(3)*	3.3/2.5/ 1.8/1.5		*(2)*		
Differential SSTL-18 class I and II output	Pseudo differential *(3)*		1.8	*(2)*		
1.8-V differential HSTL class I and II input	Pseudo differential *(3)*	3.3/2.5/ 1.8/1.5			1.8/1.5	*(2)*
1.8-V differential HSTL class I and II output	Pseudo differential *(3)*		1.8	*(2)*		
1.5-V differential HSTL class I and II input	Pseudo differential *(3)*	3.3/2.5/ 1.8/1.5		*(2)*		
1.5-V differential HSTL class I and II output	Pseudo differential *(3)*		1.5	*(2)*		
LVDS	Differential	2.5	2.5			✓
HyperTransport™ technology	Differential	2.5	2.5			✓

Notes to Table 8–6:

(1) Like Stratix II devices, the optional PCI clamp is only available on column I/O pins. General purpose IOEs on the right row I/O pins do not support the PCI clamp.

(2) Similar to Stratix II devices, these I/O standards are only available on input clock pins, output clock pins in I/O banks 9, 10, 11, 12, and DQS pins in top I/O banks 3, 4 for all HardCopy II devices, and DQS pins in bottom I/O banks 7 and 8 for HC230 and HC240 devices.

(3) Pseudo-differential HSTL and SSTL inputs only use the positive polarity input in the speed path. The negative input is not connected internally. Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. This is similar to a Stratix II device implementation.

Table 8–7 lists the I/O standards that HardCopy II devices support. Table 8–7 is organized by clock input, clock output, and PLL feedback pins.

Table 8–7. Hardcopy II Supported I/O Standards of Input Clocks, Clock Out, and PLL Feedback (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level (V)		CLK[0..3, 8..11] *(1)*	CLK[4..7, 12..15] *(2)*	FPLL_CLK *(3)*	PLL_OUT *(4)*	PLL_FB *(5)*
		Input	Output					
3.3-V LVTTL / LVCMOS	Single-ended	3.3/2.5	3.3	✓	✓	✓	✓	✓
2.5-V LVTTL / LVCMOS	Single-ended	3.3/2.5	2.5	✓	✓	✓	✓	✓
1.8-V LVTTL / LVCMOS	Single-ended	1.8/1.5	1.8	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single-ended	1.8/1.5	1.5	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5	2.5		✓		✓	✓
SSTL-2 class II	Voltage referenced	2.5	2.5		✓		✓	✓
SSTL-18 class I	Voltage referenced	1.8	1.8		✓		✓	✓
SSTL-18 class II	Voltage referenced	1.8	1.8		✓		✓	✓
1.8-V HSTL class I	Voltage referenced	1.8	1.8		✓		✓	✓
1.8-V HSTL class II	Voltage referenced	1.8	1.8		✓		✓	✓
1.5-V HSTL class I	Voltage referenced	1.5	1.5		✓		✓	✓
1.5-V HSTL class II	Voltage referenced	1.5	1.5		✓		✓	✓
PCI / PCI-X	Single-ended	3.3	3.3		✓		✓	✓
Differential SSTL-2 class I and II input	Pseudo differential *(6)*	3.3/2.5/ 1.8/1.5			✓			✓
Differential SSTL-2 class I and II output	Pseudo differential *(6)*		2.5				✓	✓
Differential SSTL-18 class I and II input	Pseudo differential *(6)*	3.3/2.5/ 1.8/1.5			✓			✓

Table 8–7. Hardcopy II Supported I/O Standards of Input Clocks, Clock Out, and PLL Feedback (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level (V)		CLK[0..3, 8..11] *(1)*	CLK[4..7, 12..15] *(2)*	FPLL_CLK *(3)*	PLL_OUT *(4)*	PLL_FB *(5)*
		Input	Output					
Differential SSTL-18 class I and II output	Pseudo differential *(6)*		1.8				✓	✓
1.8-V differential HSTL class I and II input	Pseudo differential *(6)*	3.3/2.5/ 1.8/1.5			✓			✓
1.8-V differential HSTL class I and II output	Pseudo differential *(6)*		1.8				✓	✓
1.5-V differential HSTL class I and II input	Pseudo differential *(6)*	3.3/2.5/ 1.8/1.5			✓			✓
1.5-V differential HSTL class I and II output	Pseudo differential *(6)*		1.5				✓	✓
LVDS input	Differential	2.5		✓	✓	✓		✓
LVDS output	Differential		2.5				✓	✓
HyperTransport technology input	Differential	2.5		✓	✓	✓		✓
HyperTransport technology output	Differential		2.5V				✓	✓
LVPECL input	Differential	3.3/2.5/ 1.8/1.5	*(7)*		✓		✓	✓

Notes to Table 8–7:

(1) `CLK8` and `CLK10` pins on HC210, HC220, and HC230 devices do not support differential standards LVDS and HyperTransport technology. Only LVTTL is supported on these `CLK` pins for these devices.

(2) `CLK[4..7]` pins on HC210 and HC220 devices do not support SSTL, HSTL, differential SSTL, and HSTL input or output.

(3) HC230 only has two fast PLL clocks, `FPLL[7..8]CLK`. HC240 has four FPLL clocks, `FPLL[7..10]CLK`.

(4) HC210 and HC220 `PLL6_OUT` pins do not support SSTL, HSTL, differential SSTL, and HSTL input or output.

(5) HC210 and HC220 `PLL6_FB` pins do not support SSTL, HSTL, differential SSTL, and HSTL input or output.

(6) Pseudo-differential HSTL and SSTL inputs only use the positive polarity input in the speed path. The negative input is not connected internally. Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. This is similar to a Stratix II device implementation.

(7) This is not supported.

External Memory Interface Support

Like Stratix II devices, HardCopy II I/O pins have dedicated phase-shift circuitry for interfacing with external memory, including DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM. A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals.

For all HardCopy II devices, the top I/O banks (3 and 4) support DQ and DQS signals with DQ bus modes that vary from ×4, ×8/×9, ×16/×18 and up to ×32/×36. The top bank has a phase-shifting reference circuit that controls the compensated delay elements for all DQS pins on the top bank.

For the HC230 and HC240 HardCopy II devices, the bottom I/O banks (7 and 8) also support DQ and DQS signals with DQ bus modes from ×4, ×8/×9, ×16/×18 and ×32/×36. Similar to the top banks, the bottom I/O banks of these devices also have a phase-shifting reference circuit to control the delay elements at the bottom DQS pins.

Table 8–8 shows the number of DQ and DQS buses supported per companion device pair. *(3)*

Table 8–8. DQ and DQS Bus Mode support for Stratix II and HardCopy II Companion Devices (Part 1 of 2) *Note (1)*

Stratix II and HardCopy II Companion Devices	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S30 HC210 *(2)*	484-pin FineLine BGA	4	2		
EP2S60 HC210 *(2)*	484-pin FineLine BGA	4	2		
EP2S90 HC210 *(2)*	484-pin FineLine BGA	4	2		
EP2S60 HC220 *(2)*	672-pin FineLine BGA	9	4	2	
EP2S90 HC220 *(2)*	780-pin FineLine BGA	9	4	2	
EP2S130 HC220 *(2)*	780-pin FineLine BGA	9	4	2	
EP2S90 HC230 *(3)*	1,020-pin FineLine BGA	36	18	8	4
EP2S130 HC230 *(3)*	1,020-pin FineLine BGA	36	18	8	4

Table 8–8. DQ and DQS Bus Mode support for Stratix II and HardCopy II Companion Devices (Part 2 of 2) *Note (1)*

Stratix II and HardCopy II Companion Devices	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S180 HC230 *(3)*	1,020-pin FineLine BGA	36	18	8	4
EP2S180 HC240	1,020-pin FineLine BGA	36	18	8	4
EP2S180 HC240	1,508-pin FineLine BGA	36	18	8	4

Notes to Table 8–8:

(1) The DQ and DQS numbers are preliminary.

(2) HardCopy II devices HC210 and HC220 support memory interface in the top I/O banks only. Unlike their Stratix II companions, these devices cannot support DIMMs.

(3) Similar to their Stratix II companions, these device and package combinations can support two 64- or 72-bit DIMMs in ×4 and ×8/×9 modes.

LVDS, SERDES, and DPA Compatibility

HardCopy II devices offer up to 116 transmitter and receiver pairs. Similar to Stratix II devices, these differential I/O pins are located on row I/O pins. The HC240 device's left and right banks are high-speed IOEs which support differential transmission. The HC210, HC220, and HC230 devices only support differential transmission on the left banks. The LVDS and HyperTransport technology interface functionality, including the SERDES and DPA, is the same as Stratix II devices.

Table 8–9 shows the maximum differential channel supported by each HardCopy II and Stratix II companion pair.

Table 8–9. Differential Channels with Stratix II and HardCopy II Companion Devices (Part 1 of 2) *Note (1)*

Stratix II and HardCopy II Companion Devices	Package	Transmitters	Receivers
EP2S30 HC210 *(2)*	484-pin FineLine BGA	19	21
EP2S60 HC210 *(2)*	484-pin FineLine BGA	19	21
EP2S90 HC210 *(2)*	484-pin FineLine BGA	19	21

Table 8–9. Differential Channels with Stratix II and HardCopy II Companion Devices (Part 2 of 2) *Note (1)*

Stratix II and HardCopy II Companion Devices	Package	Transmitters	Receivers
EP2S60 HC220 *(2)*	672-pin FineLine BGA	29	31
EP2S90 HC220 *(2)*	780-pin FineLine BGA	29	31
EP2S130 HC220 *(2)*	780-pin FineLine BGA	29	31
EP2S90 HC230 *(2)*	1,020-pin FineLine BGA	44	46
EP2S130 HC230 *(2)*	1,020-pin FineLine BGA	44	46
EP2S180 HC230 *(2)*	1,020-pin FineLine BGA	44	46
EP2S180 HC240 *(3)*	1,020-pin FineLine BGA	88	92
EP2S180 HC240 *(3)*	1,508-pin FineLine BGA	116	116

Notes to Table 8–9:

(1) Pin count does not include dedicated PLL input and output pins.

(2) The total number of receiver channels for HC210, HC220, and HC230 devices include two non-dedicated clock channels that can optionally be used as data channels.

(3) The total number of receiver channels for HC240 devices include four non-dedicated clock channels that can optionally be used as data channels.

Programmable Drive Strength Support

The maximum current strength setting is the default setting in the Quartus II software and achieves maximum I/O performance. Stratix II device output buffers for each I/O pin have a programmable drive strength control for certain I/O standards.

HardCopy II support for these settings differs from that found in Stratix II devices. For compatibility with HardCopy II HC210 and HC220 devices, you must restrict the I/O drive settings of Stratix II companion devices, as shown in Table 8–10.

Table 8–10. HC210 and HC220 Device Programmable Drive Strengths

I/O Standard	I_{OH} and I_{OL} Current Strength Setting (mA) for Top Column I/O Pins	I_{OH} and I_{OL} Current Strength Setting (mA) for Bottom Column I/O Pins	I_{OH} and I_{OL} Current Strength Setting (mA) for Left Row I/O Pins	I_{OH} and I_{OL} Current Strength Setting (mA) for Right Row I/O Pins
3.3-V LVTTL	24, 20, 12, 8, 4 *(1)*	12, 8, 4 *(1)*	12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 12, 8, 4 *(1)*	8, 4 *(1)*	8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4 *(1)*	12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2 *(1)*	8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2 *(1)*	4, 2	4, 2
SSTL-2 class I	12, 8	*(2)*	*(3)*	*(3)*
SSTL-2 class II	24, 20, 16	*(2)*	*(3)*	*(3)*
SSTL-18 class I	12, 10, 8, 6, 4	*(2)*	*(3)*	*(3)*
SSTL-18 class II	20, 18, 16, 8	*(2)*	-	-
HSTL-18 class I	12, 10, 8, 6, 4	*(2)*	-	-
HSTL-18 class II	20, 18, 16	*(2)*	-	-
HSTL-15 class I	12, 10, 8, 6, 4	*(2)*	-	-
HSTL-15 class II	20, 18, 16	*(2)*	-	-

Notes to Table 8–10:

(1) HardCopy II devices do not support some of the settings available in the Stratix II prototype device. For more information, refer to the *Stratix II Device Family Data Sheet* in volume 1 of the *Stratix II Device Handbook*.

(2) HC220 and HC210 devices do not support memory interface standards on bottom I/O pins.

(3) Row I/O pins do not support SSTL I/O standards.

Similarly, when using HardCopy II HC230 and HC240 devices as companion devices, you must restrict the I/O drive settings, as shown in Table 8–11.

Table 8–11. HC230 and HC240 Device Programmable Drive Strengths

I/O Standard	I_{OH} and I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} and I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4 *(1)*	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4 *(1)*	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 class I	12, 8	*(2)*
SSTL-2 class II	24, 20, 16	*(2)*
SSTL-18 class I	12, 10, 8, 6, 4	*(2)*
SSTL-18 class II	20, 18, 16, 8	-
HSTL-18 class I	12, 10, 8, 6, 4	-
HSTL-18 class II	20, 18, 16	-
HSTL-15 class I	12, 10, 8, 6, 4	-
HSTL-15 class II	20, 18, 16	-

Notes to Table 8–11:

(1) HardCopy II devices do not support some of the settings available in the Stratix II prototype device. For more information, refer to the *Stratix II Device Family Data Sheet* in volume 1 of the *Stratix II Device Handbook*.

(2) Row I/O pins do not support SSTL I/O standards.

On-Chip Termination

Like Stratix II devices, HardCopy II devices feature on-chip termination (OCT) to provide I/O impedance matching and termination capabilities. To maintain compatibility with Stratix II prototype devices, HardCopy II devices support on-chip series termination (RS) for single-ended I/O standards and on-chip differential termination (RD) for differential I/O standards. However, some HardCopy II pins do not support the on-chip termination that may be available on the same Stratix II pin. This section highlights the termination schemes that HardCopy II devices support.

On-Chip Series Termination

Stratix II and HardCopy II devices support I/O driver on-chip series termination (RS) through drive-strength control for single-ended I/O standards. There are two ways to implement the RS in Stratix II and Hardcopy II devices:

- RS without calibration for both row and column I/O pins
- RS with calibration only for column I/O pins

On-Chip Series Termination without Calibration

HardCopy II devices support output-driver impedance matching to closely match the impedance of the transmission line. If you select matching impedance, you cannot select programmable-current drive strength. Table 8–12 lists the HardCopy II HC230 and HC240 output standards that support on-chip series termination without calibration.

Table 8–12. HC230 and HC240 Selectable I/O Drivers with On-Chip Series Termination without Calibration *Note (1)*

I/O Standard	Column I/O Pins	Row I/O Pins
3.3-V LVTTL	25 or 50 Ω	25 or 50 Ω
3.3-V LVCMOS	25 or 50 Ω	25 or 50 Ω
2.5-V LVTTL	25 or 50 Ω	25 or 50 Ω
2.5-V LVCMOS	25 or 50 Ω	25 or 50 Ω
1.8-V LVTTL	25 or 50 Ω	50 Ω
1.8-V LVCMOS	25 or 50 Ω	50 Ω
1.5-V LVTTL	50 Ω	
1.5-V LVCMOS	50 Ω	
2.5-V SSTL class I	50 Ω	*(2)*
2.5-V SSTL class II	25 Ω	*(2)*
1.8-V SSTL class I	50 Ω	*(2)*
1.8-V SSTL class II	25 Ω	
1.8-V HSTL class I	50 Ω	*(2)*
1.8-V HSTL class II	25 Ω	
1.5-V HSTL class I	*(3)*	

Notes to Table 8–12:

(1) These numbers are preliminary and pending silicon characterization.

(2) HardCopy II HC230 and HC240 devices do not support on-chip series termination with this I/O standard on these pins.

(3) Support pending HardCopy II characterization.

Table 8–13 lists the HardCopy II HC210 and HC220 output standards that support on-chip series termination without calibration.

Table 8–13. HC210 and HC220 Selectable I/O Drivers with On-Chip Series Termination without Calibration *Note (1)*

I/O Standard	Top Column I/O Pins	Bottom Column I/O Pins	Left Row I/O Pins	Right Row I/O Pins
3.3-V LVTTL	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω
3.3-V LVCMOS	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω
2.5-V LVTTL	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω
2.5-V LVCMOS	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω	25 or 50 Ω
1.8-V LVTTL	25 or 50 Ω	50 Ω	50 Ω	50 Ω
1.8-V LVCMOS	25 or 50 Ω	50 Ω	50 Ω	50 Ω
1.5-V LVTTL	*(3)*	*(2)*		
1.5-V LVCMOS	*(3)*	*(2)*		
2.5-V SSTL class I	50 Ω	*(2)*	*(2)*	*(2)*
2.5-V SSTL class II	25 Ω	*(2)*	*(2)*	*(2)*
1.8-V SSTL class I	50 Ω	*(2)*	*(2)*	*(2)*
1.8-V SSTL class II	25 Ω	*(2)*		
1.8-V HSTL class I	50 Ω	*(2)*	*(2)*	*(2)*
1.8-V HSTL class II	25 Ω	*(2)*		
1.5-V HSTL class I	*(3)*	*(2)*		

Notes to Table 8–13:

(1) All these numbers are preliminary and pending silicon characterization.

(2) HardCopy II HC210 and HC220 devices do not support on-chip series termination with this I/O standard on these pins.

(3) Support pending HardCopy II characterization.

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/O pins in the top and bottom banks. HC230 and HC240 devices also support on-chip series termination with calibration in column I/O pins in the top and bottom banks, but HC220 and HC210 devices only support this feature on the top I/O banks. Table 8–14 lists available I/O standards on the HardCopy II devices that support calibrated-series termination.

Table 8–14. HardCopy II Selectable I/O Drivers with On-Chip Series Termination with Calibration *Note (1)*

I/O Standard	HC230, HC240 Column I/O Pins	HC210, HC220 Top Column I/O Pins *(2)*
3.3-V LVTTL	25 or 50 Ω	25 or 50 Ω
3.3-V LVCMOS	25 or 50 Ω	25 or 50 Ω
2.5-V LVTTL	25 or 50 Ω	25 or 50 Ω
2.5-V LVCMOS	25 or 50 Ω	25 or 50 Ω
1.8-V LVTTL	25 or 50 Ω	25 or 50 Ω
1.8-V LVCMOS	25 or 50 Ω	25 or 50 Ω
1.5-V LVTTL	*(3)*	50 Ω
1.5-V LVCMOS	*(3)*	50 Ω
2.5-V SSTL class I	50 Ω	50 Ω
2.5-V SSTL class II	25 Ω	50 Ω
1.8-V SSTL class I	50 Ω	50 Ω
1.8-V SSTL class II	25 Ω	25 Ω
1.8-V HSTL class I	50 Ω	50 Ω
1.8-V HSTL class II	25 Ω	25 Ω
1.5-V HSTL class I	*(3)*	50 Ω

Notes to Table 8–14:

(1) These numbers are preliminary and pending silicon characterization.
(2) HardCopy II HC210 and HC220 devices do not support on-chip series termination with calibration on bottom I/O pins.
(3) Support pending HardCopy II characterization.

Differential I/O Termination

Similar to the FPGA, HardCopy II devices provide an on-chip 100-Ω differential termination option on each differential receiver channel for LVDS and HyperTransport technology standards. When using an HC240 device as a companion device, differential termination is supported on all row I/O pins that support LVDS and HyperTransport technology standards.

When using HC230, HC220, and HC210 devices, only the left row I/O pins support differential termination. The right row I/O pins do not support LVDS and HyperTransport technology standards.

Table 8–15 shows the differential termination support.

Table 8–15. HardCopy II I/O Banks Supporting 100-Ω Differential Termination *Notes (1), (2)*

I/O Standard	HC240 Left and Right Banks (1, 2, 5 and 6)	HC240 Top and Bottom Banks (3, 4, 7 through 12)	HC230, HC210, HC220 Left Banks (1 and 2)	HC230, HC210, HC220 Other Banks (3 to 12)
LVDS	✓		✓	
HyperTransport technology	✓		✓	
Clock Inputs *(3)*	✓		✓	

Notes to Table 8–15:
(1) HC230, HC220, and HC210 device left clock pins `CLK0` and `CLK2` support differential on-chip termination.
(2) All other clock pins, including `FPLL[7..10]CLK`, do not support differential on-chip termination.
(3) HardCopy II HC240 device clock pins `CLK0`, `CLK2`, `CLK8`, and `CLK10` support differential on-chip termination, similar to Stratix II devices.

Stratix II and HardCopy II Companion Memory Blocks

HardCopy II device RAM bit offerings range from 663 kbits to 8.8 Mbits. HardCopy II memory blocks are functionally equivalent to the Stratix II memory blocks. HardCopy II memory blocks can implement various Stratix II device memory configurations, including simple and true dual port modes, FIFO, parity bits, ROM modes, and all other features, as listed in the *HardCopy II Description, Architecture, and Features* chapter of the *HardCopy Series Handbook*. One difference between HardCopy II and Stratix II devices is that HardCopy II devices do not support M512 blocks. Additionally, you cannot pre-load HardCopy II M4K blocks with a Memory Initialization File (**.mif**) when used as RAM.

Table 8–16 shows all the memory block offerings when compiling for a Stratix II FPGA in conjunction with a HardCopy II companion device. Use Table 8–16 as a guide when optimizing memory requirements for selected Stratix II and HardCopy II pairs.

Table 8–16. Total RAM Blocks for Stratix II and HardCopy II Companion Devices (Part 1 of 2)

Stratix II and HardCopy II Companion Devices	Package	M4K Blocks	M-RAM Blocks	Total RAM Bits
EP2S30 HC210	484-pin FineLine BGA	144	0	663,552
EP2S60 HC210	484-pin FineLine BGA	190	0	875,520

Table 8–16. Total RAM Blocks for Stratix II and HardCopy II Companion Devices (Part 2 of 2)

Stratix II and HardCopy II Companion Devices	Package	M4K Blocks	M-RAM Blocks	Total RAM Bits
EP2S90 HC210	484-pin FineLine BGA	190	0	875,520
EP2S60 HC220	672-pin FineLine BGA	255	2	2,354,688
EP2S90 HC220	780-pin FineLine BGA	408	2	3,059,712
EP2S130 HC220	780-pin FineLine BGA	408	2	3,059,712
EP2S90 HC230	1,020-pin FineLine BGA	408	4	4,239,360
EP2S130 HC230	1,020-pin FineLine BGA	609	6	6,345,216
EP2S180 HC230	1,020-pin FineLine BGA	614	6	6,368,256
EP2S180 HC240	1,020-pin FineLine BGA	768*(1)*	9	8,847,360
EP2S180 HC240	1,508-pin FineLine BGA	768*(1)*	9	8,847,360

Note to Table 8–16

(1) The total number of usable M4K blocks is limited to 768 to allow migration compatibility when prototyping with an EP2S180 device.

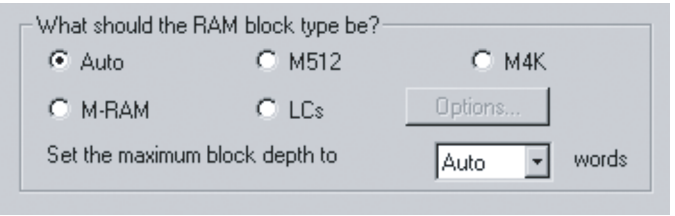
Table 8–16 does not list M512 blocks because they are not supported in HardCopy II devices. Also, the HC210 devices do not offer M-RAM blocks. Some compatibility guidelines are discussed in the next sections.

M512 Options

HardCopy II devices do not support M512 blocks. When compiling Stratix II designs with Hardcopy II companions devices in the Quartus II software, you must check the **Limit DSP and RAM to HardCopy II Resources** box in the **Device Settings** dialog box (Assignments Menu). This automatically places all memory blocks in the available HardCopy II resources. If you do not check this box, the Quartus II software may use memory resources not available in the HardCopy II device but available in the Stratix II device, such as M512 blocks. However, migration into HardCopy II devices is not allowed and this is indicated in the Quartus II fitter report.

Your HardCopy II design can use M4K memory blocks to implement memory designs instead of M512 blocks. Quartus II megafunctions offer various memory implementations that use M4K blocks. When using the Quartus II MegaWizard® Plug-In Manager to configure the megafunction, Altera recommends selecting the **Auto** option to allow the Quartus II software to determine how the design is implemented in the memory blocks (Figure 8–2). This allows the Quartus II software to optimize memory selection based on memory size and placement requirements into the available memory blocks of the selected HardCopy II and Stratix II companion pair.

Figure 8–2. Quartus II MegaFunction RAM selection



You can select logic cells in the megafunction to implement small-memory blocks in your design. This implements the memory design in Stratix II ALMs or HardCopy II HCells. However, there may be power and performance trade-offs when choosing between an M4K or M-RAM block or using the ALMs (or HCells). HardCopy II devices power down unused M4K blocks, M-RAM blocks, and HCells.

Implementing memory blocks using logic cells, as seen in Figure 8–2, allows you to select a memory implementation functionally equivalent to M512 blocks or a non-equivalent option to save resources. Altera recommends setting the option to a functionally equivalent version with the M512 blocks.

For very small memory implementations such as a 8 × 16 single port RAM, the M4K or M-RAM blocks will be under-utilized, and may be less power efficient than a small number of HCells. If you select the logic cell option, only a fraction of ALMs are required in the Stratix II device, which translates into a small number HCells used in the HardCopy II device. However, when performance is a key factor, or your design requires ALMs to implement other logic, it may be more efficient to use M4K blocks. Altera recommends using the Quartus II software to analyze performance trade-offs between the given options.

M4K Utilization

HardCopy II M4K block functionality is similar to Stratix II M4K blocks. You cannot pre-load HardCopy II M4K blocks with a memory initialization file (**.mif**) when used as RAM. Also, unlike Stratix II devices, the HardCopy II M4K RAM contents and their output registers are unknown after power up. However, if the HardCopy II M4K block is designated as ROM, it powers up with the ROM contents. When designing M4K blocks as RAM, Altera recommends writing to the block before reading from it to avoid reading unknown initial power-up data conditions. One advantage over Stratix II RAM blocks is unused M4K blocks are disconnected from the power rails, optimizing overall power consumption.

M-RAM Compatibility

HardCopy II M-RAM blocks share the same functionality as Stratix II M-RAM blocks. One key feature with HardCopy II M-RAM blocks is power optimization when the M-RAM block is not used. Unused M-RAM blocks are disconnected from the power rails, optimizing overall power consumption.

Some Stratix II devices (engineering sample devices and Revision A production devices) have M-RAM functionality that differs slightly from current Stratix II production devices. HardCopy II M-RAM functionality only matches that of current Stratix II devices. Hence, in order to maintain proper compatibility, compiling only for current production Stratix II devices is supported. More information on the Stratix II M-RAM errata can be found in the *Stratix II FPGA Family Errata Sheet* available on the Altera website (**www.altera.com**).

Table 8–17 lists the M4K and M-RAM block supported features. This information can also be found in the *HardCopy II Description, Architecture, and Features* chapter of the *HardCopy Series Handbook*.

Table 8–17. HardCopy II Embedded Memory Features (Part 1 of 2)

Feature	M4K Blocks	M-RAM Blocks
Total RAM bits (including parity bits)	4,608	589,824
Configurations	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144
Parity bits	✓	✓
Byte enable	✓	✓
Pack mode	✓	✓
Address clock enable	✓	✓
Single-port memory	✓	✓
Simple dual-port memory	✓	✓
True dual-port memory	✓	✓
Embedded shift register	✓	—
ROM	✓	—
FIFO buffer	✓	✓
Simple dual-port mixed width support	✓	✓
True dual-port mixed width support	✓	✓
Memory initialization file (**.mif**)	*(1)*	—
Mixed-clock mode	✓	✓
Power-up condition	Outputs unknown	Outputs unknown
Register clears	Output registers only	Output registers only
Same-port read-during-write	New data available at positive clock edge	New data available at positive clock edge

Table 8–17. HardCopy II Embedded Memory Features (Part 2 of 2)		
Feature	**M4K Blocks**	**M-RAM Blocks**
Mixed-port read-during-write	Outputs set to unknown or old data	Unknown output
Power down of unused RAM blocks *(2)*	✓	✓

Notes to Table 8–17:
(1) Stratix II M4K blocks support **.mif** file loading.
(2) Stratix II memory blocks remain powered up even when not used.

PLL Planning and Utilization

Stratix II devices support enhanced PLLs and fast PLLs. HardCopy II devices also support enhanced PLLs and fast PLLs, but with two variations:

- HardCopy II devices have a different number of PLLs than Stratix II devices.
- HardCopy II devices may support fewer I/O standards for clock inputs and outputs. This is explained in the I/O standards support section later in this chapter.

Table 8–18 shows which PLLs each HardCopy II and Stratix II device supports. The Stratix II reference columns are divided based on package, not density. Figures 8–3 to 8–5 show PLL number designations. The Stratix II devices support 6 or 12 PLLs depending on the package offering, and not the device density. The HardCopy II PLLs are not removed symmetrically from all four sides. In general, fast PLLs are removed from sides that do not support high speed IOEs since the primary use of the fast PLL on the sides is for high speed I/O interface functions.

Table 8–18. Stratix II / HardCopy II Companion Device PLL Availability Guide (Part 1 of 2)													
Stratix II and HardCopy II Companion Devices	**Package**	**Fast PLLs**								**Enhanced PLLs**			
		1	**2**	**3**	**4**	**7**	**8**	**9**	**10**	**5**	**6**	**11**	**12**
EP2S30 HC210 *(1)*	484-pin FineLine BGA	✓	✓							✓	✓		
EP2S60 HC210 *(1)*	484-pin FineLine BGA	✓	✓							✓	✓		
EP2S90 HC210 *(1)*	484-pin FineLine BGA	✓	✓							✓	✓		
EP2S60 HC220 *(1)*	672-pin FineLine BGA	✓	✓							✓	✓		

Table 8–18. Stratix II / HardCopy II Companion Device PLL Availability Guide (Part 2 of 2)

Stratix II and HardCopy II Companion Devices	Package	Fast PLLs								Enhanced PLLs			
		1	2	3	4	7	8	9	10	5	6	11	12
EP2S90 HC220 *(1)*	780-pin FineLine BGA	✓	✓							✓	✓		
EP2S130 HC220 *(1)*	780-pin FineLine BGA	✓	✓							✓	✓		
EP2S90 HC230 *(2)*	1,020-pin FineLine BGA	✓	✓			✓	✓			✓	✓	✓	✓
EP2S130 HC230 *(2)*	1,020-pin FineLine BGA	✓	✓			✓	✓			✓	✓	✓	✓
EP2S180 HC230 *(2)*	1,020-pin FineLine BGA	✓	✓			✓	✓			✓	✓	✓	✓
EP2S180 HC240	1,020-pin FineLine BGA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S180 HC240	1,508-pin FineLine BGA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

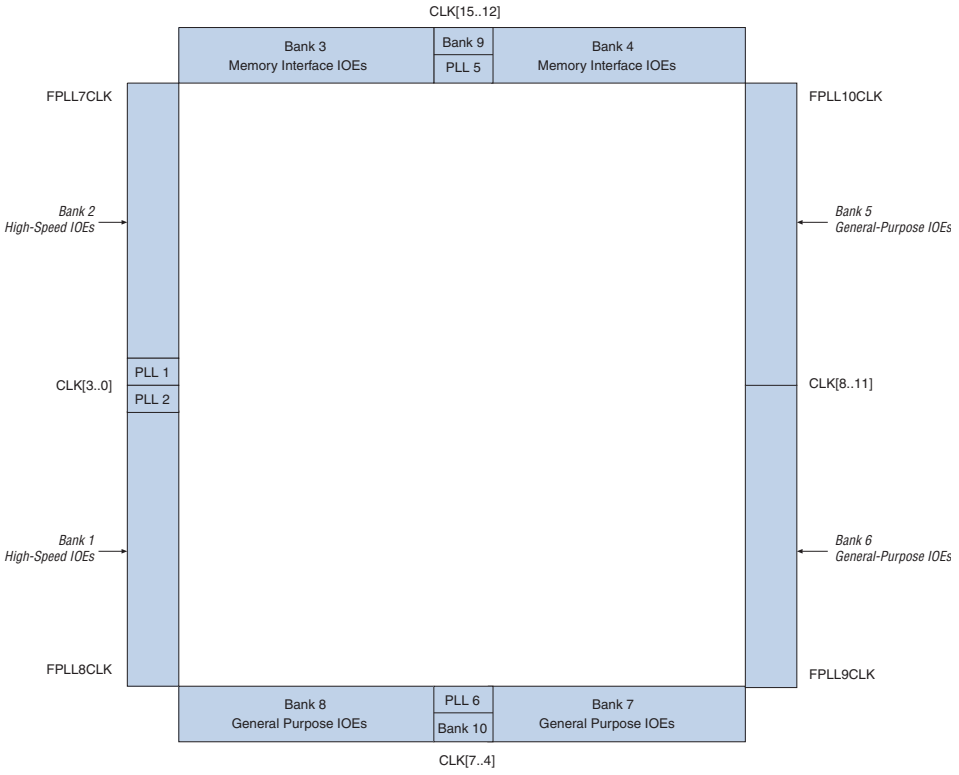
Notes to Table 8–18:
(1) HC210 and HC220 devices do not support fast PLLs 3, 4, 9, and 10, unlike Stratix II devices.
(2) HC230 devices do not support fast PLLs 3 and 4, unlike Stratix II devices.

HardCopy II PLLs are functionally identical to the Stratix II PLLs. The HardCopy II enhanced and fast PLLs support reconfiguration and are also reconfigurable for bandwidth and phase shift.

Figures 8–3 to 8–5 show the PLL locations for each HardCopy II device.

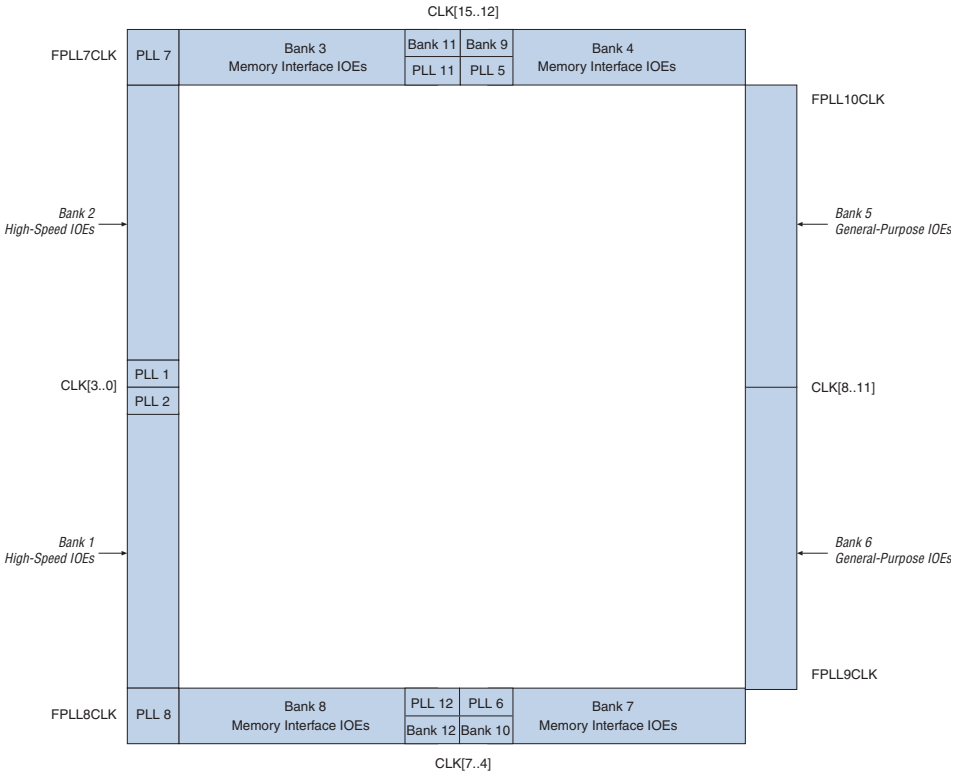
For HC210 and HC220 devices, fast PLLs 1 and 2 are located in the logic array of the device and enhanced PLLs 5 and 6 are located in the periphery next to the device's top and bottom I/O banks.

Figure 8–3. HC210 and HC220 PLL Locations



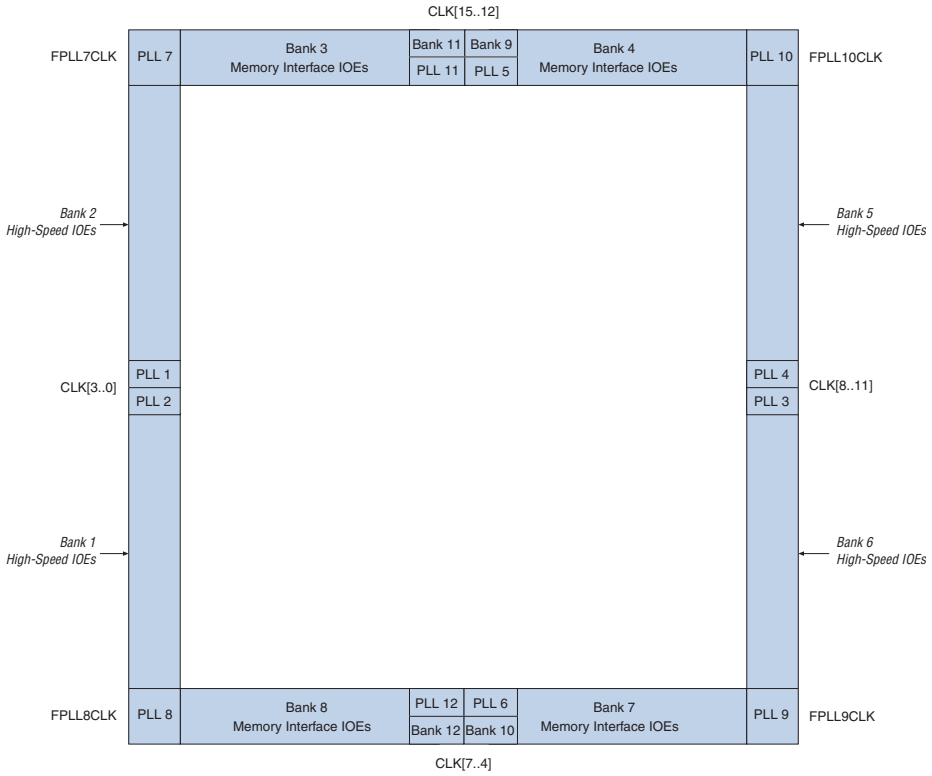
HC230 device fast PLLs 1, 2, 7, and 8 are located in the logic array, next to the device's left high-speed IOEs. HC230 device enhanced PLLs 5, 6, 11, and 12 are also located in the logic array, next to the top and bottom memory interface IOEs.

Figure 8–4. HC230 PLL Locations



HC240 device fast PLLs 1, 2, 7, and 8 are located in the logic array, next to the left high speed IOEs of the device. HC240 device fast PLLs 3, 4, 9, and 10 are located in the logic array, next to the right high speed IOEs. HC240 device enhanced PLLs 5, 6, 11, and 12 are located in the logic array, next to the top and bottom memory interface IOEs.

Figure 8–5. HC240 PLL Locations



Global and Local Signals

HardCopy II devices have 16 clock pins (`CLK[15..0]`) to drive either the global or local clock networks. Four clock pins drive each side of the device. This is similar to Stratix II devices; therefore, there are no limitations when compiling designs for Stratix II devices and HardCopy II companion devices.

Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock network has a clock control block, which controls the selection of the clock source and allows you to dynamically enable or disable the clock network to reduce power consumption.

Table 8–19 lists the clock resources available in HardCopy II devices.

Table 8–19. Clock Network Resources and Features Available in HardCopy II Devices

Resources and Features	Availability
Number of global clock networks	16
Number of regional clock networks	32
Global clock input sources	Clock input pins, PLL outputs, logic array
Regional clock input sources	Clock input pins, PLL outputs, logic array
Number of unique clock sources in a quadrant	24 (16 global clocks and 8 regional clocks)
Number of unique clock sources in the entire device	48 (16 global clocks and 32 regional clocks)
Power-down mode	Global and regional clock networks, dual-regional clock region
Clocking regions for high fan-out applications	Quadrant region, dual-regional, entire device via global or regional clock networks

Stratix II ALM Adaptation into HardCopy II Logic

The basic logic building block in the Stratix II architecture is the ALM. Each ALM contains a variety of look-up table- (LUT-) based resources, two programmable registers, two dedicated full adders, and various routing resources to and from the ALM.

HardCopy II devices do not have ALM blocks, but use a fine-grain architecture called HCells. HCells can implement all combinations of Stratix II ALM and DSP logic. Each HardCopy II companion device contains an abundance of HCells to implement a Stratix II design utilizing all available ALMs. Therefore, there are no compatibility constraints when compiling for HardCopy II devices.

When compiling a Stratix II design into a HardCopy II companion device, the Quartus II software replaces ALM blocks used in Stratix II with predefined HCell macros. Unused ALM resources are not implemented in HardCopy II devices. This allows for optimal placement of the HardCopy II floor plan and significant power savings.

Figure 8–6 shows an example of a Stratix II ALM block implementation using only one of the registers. When compiling this Stratix II design for a HardCopy II companion device, the Quartus II compiler replaces the

ALM block with a predetermined HCell macro that implements a register from its HardCopy II library of HCell macros. This macro entry has predetermined timing.

Figure 8–6. Stratix II ALM Simple Registered Input and Output

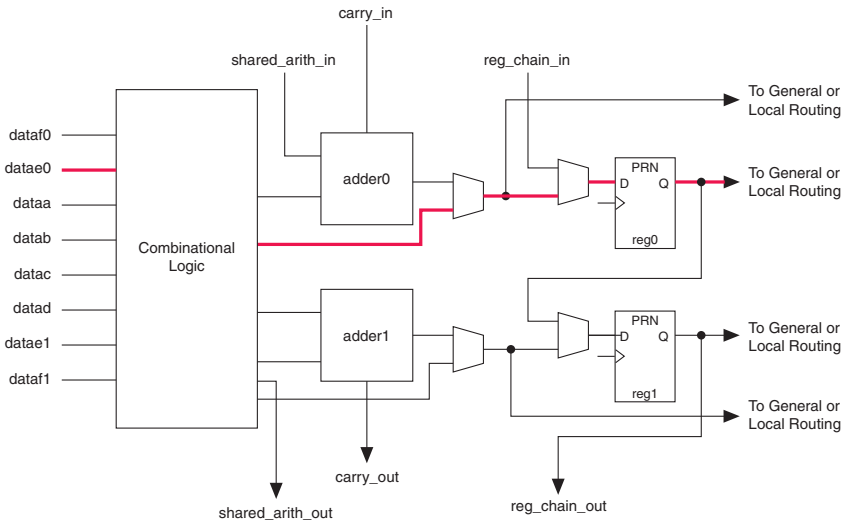
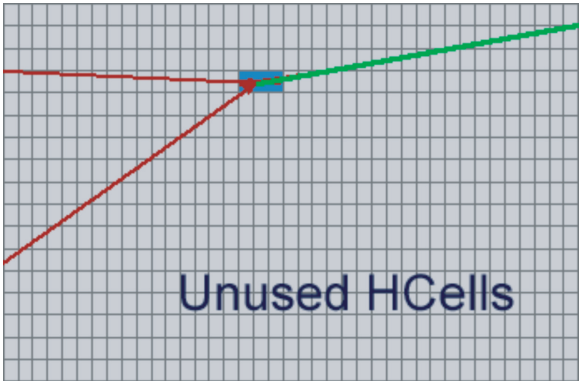


Figure 8–7 shows a HardCopy II ALM register implementation showing Clock, Data In, and Data Out originating from a small cluster of HCells. Unused HCells are reserved for other logic implementation or powered down.

Figure 8–7. HardCopy II Unused HCells



HardCopy II DSP Implementation from Stratix II DSP Blocks

Stratix II FPGAs have dedicated DSP blocks to implement various DSP functions. Stratix II DSP blocks consist of multipliers, an adder/subtractor/accumulator and a summation block, input and output interfaces, and input and output registers. The Quartus II software implements DSP functions in HardCopy II devices with HCells using predetermined logic implementations from its library of HCell macros, all of which have predetermined timing.

DSP blocks that are not used in the Stratix II design are not implemented in Hardcopy II devices. This preserves the HardCopy II logic for other implementations, saving resources and power. Furthermore, the HardCopy II DSP block placement can be optimized to meet the timing constraint requirements placed on the HardCopy II designs.

The HardCopy II DSP implementation is functionally equivalent to Stratix II DSP blocks and all features are supported except for dynamic-mode switching. You can set up Stratix II DSP blocks to dynamically switch between the following three modes:

- Up to four 18-bit independent multipliers
- Up to two 18-bit multiplier-accumulators
- One 36-bit multiplier

HardCopy II DSP implementation does not support dynamic switching. If this feature is used, the Quartus II software flags the DSP implementation and does not allow you to migrate the design. The fitter reports that all HardCopy II devices are not compatible with the design. To migrate your Stratix II design to a HardCopy II companion device, disable dynamic switching in the DSP blocks.

The total number of DSP blocks is dependent on the Stratix II device selected. HardCopy II devices will match the available DSP block resources in the Stratix II device. Table 8–20 lists available DSP implementations based on the selected Stratix II device.

Table 8–20. DSP Multiplier Availability for Stratix II and HardCopy II Companion Devices (Part 1 of 2)

Stratix II Device	HC210			HC220			HC230			HC240		
	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36
EP2S30	128	64	16									
EP2S60	288	144	36	288	144	36						
EP2S90 *(1)*	384	192	48	384	192	48	384	192	48			
EP2S130 *(1)*				504	252	63	504	252	63			

Table 8–20. DSP Multiplier Availability for Stratix II and HardCopy II Companion Devices (Part 2 of 2)

Stratix II Device	HC210			HC220			HC230			HC240		
	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36
EP2S180 *(1)*							768	384	96	768	384	96

Note to Table 8–20:

(1) If these Stratix II devices are selected with smaller HardCopy II companion devices, all Stratix II DSP resources may not be available if all the Stratix II ALM blocks are used and fully utilized. Quartus II will determine available resources for DSP and ALM implementation when compiling with HardCopy II devices.

Figure 8–8 shows an example of a Stratix II DSP block that uses only 1 of 8 available 9 × 9 multiplier blocks and an accumulator block to implement an 8 × 8 bit multiplication function with clock latency. When this DSP block is implemented in the HardCopy II design, the Quartus II Compiler chooses the appropriate entry from the macro library to implement the 9 × 9 multiplier and accumulator block which results in an optimized logic utilization and placement flexibility.

Figure 8–8. HardCopy II Floorplan of 8 × 8 DSP Block

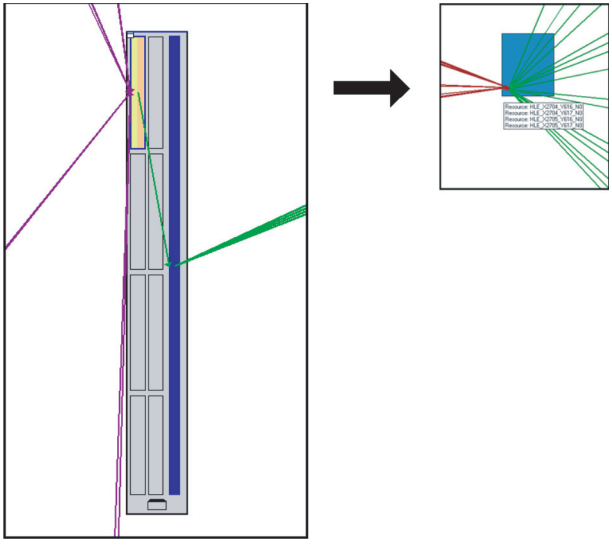
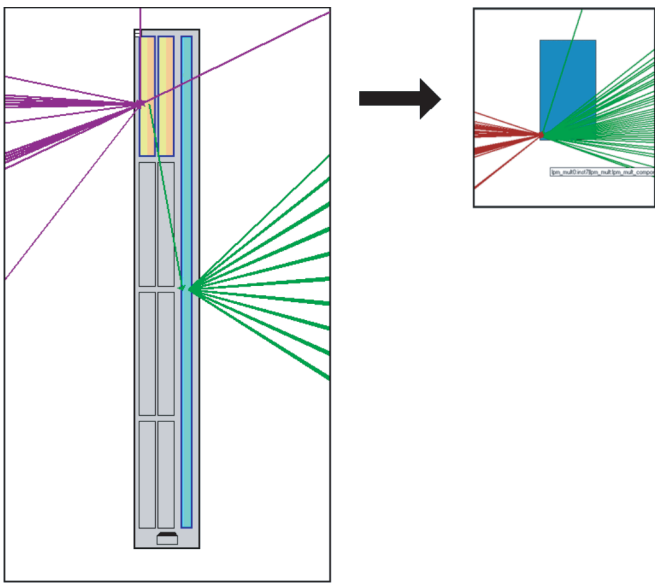


Figure 8–9 shows Quartus II floor plans of a Stratix II DSP block on the left and a HardCopy II DSP implementation on the right, both configured with an 18 × 18 multiply with accumulate function. In the HardCopy II implementation, the Quartus II software selected the appropriate DSP logic implementation from the macro library which results in an optimal utilization of the HardCopy II device's HCells. The unused sections of the Stratix II DSP block remain powered up, but these are not implemented in the HardCopy II device. Unused logic in HardCopy II devices are powered down.

Figure 8–9. HardCopy II Floorplan of 18 × 18 DSP Block



JTAG BST and Extended Functions

HardCopy II devices support the same boundary-scan test (BST) functionality as the Stratix II devices. However, since HardCopy II devices are mask-programmed, no reconfiguration is possible. Therefore, HardCopy II devices do not support instructions to reconfigure the device through the JTAG pins. For a list of supported features and instruction codes, refer to the *Boundary-Scan Support* chapter of the *HardCopy Series Handbook*.

One Stratix II feature utilizing JTAG pins is the Signal Tap II embedded logic analyzer (ELA). HardCopy II devices support the JTAG ELA feature. However, designing with this feature will use additional resources and may reduce peak performance in Stratix II and

HardCopy II devices. Unlike Stratix II devices, where this feature can be eliminated prior to compiling a final version of the design, HardCopy II devices are masked programmed and this feature will remain permanent in the HardCopy II device. Therefore, if the design requires optimal performance and resource utilization, Altera recommends using this feature on the Stratix II prototype device, but eliminating it prior to recompiling the design for a HardCopy II device.

Power Up and Configuration Compatibility

When designing a board with a Stratix II prototype device and its companion HardCopy II device, most configuration pins required by the Stratix II device are not required by the HardCopy II device. To maximize I/O pin counts with HardCopy II device utilization, Altera recommends minimizing power up and configuration pins that will not carry over from a Stratix II device into a HardCopy II device. Table 8–21 lists the dedicated and optional configuration pins that a Stratix II device can use and if their optional functionality is used on a HardCopy II device.

If the HardCopy II device can use the pin's optional function found in Stratix II devices, the Quartus II software allows you to set these pins as dual purpose pins. As dual purpose pins, they have I/O functionality after power up, reconfiguration and initialization. These pins will only switch to their I/O designation when the device enters user mode (when INIT_DONE is asserted). The design may require that some signals be present when the device transitions into user mode, so you should not use dual purpose pins because it may result in unstable operation after power up for both the HardCopy II and the Stratix II devices.

Table 8–21. Power Up and Configuration Pin Compatibility (Part 1 of 3)

Stratix II Pin Name		I/O Bank	HardCopy II Use	
Main Function	Optional Function		Main Function	Optional Function
MSEL3		B4		
MSEL2		B4		
MSEL1		B4		
MSEL0		B4		
VCCSEL		B8	✓	✓
*n*CONFIG		B8	✓	✓
*n*STATUS		B3	✓	✓
CONF_DONE		B3	✓	✓
*n*CE		B3	✓	✓

Table 8–21. Power Up and Configuration Pin Compatibility (Part 2 of 3)

Stratix II Pin Name		I/O Bank	HardCopy II Use	
Main Function	Optional Function		Main Function	Optional Function
*n*CEO		B7	✓	✓
PORSEL		B7	✓	✓
*n*IO_PULLUP		B7	✓	✓
PLL_ENA		B7	✓	✓
I/O pin	CLKUSR	B8	✓	
I/O pin	DEV_OE	B8	✓	✓
I/O pin	DEV_CLRn	B8	✓	✓
I/O pin	INIT_DONE	B3	✓	✓
DCLK		B3	✓	
I/O pin	DATA0	B3	✓	
I/O pin	DATA1	B3	✓	
I/O pin	DATA2	B3	✓	
I/O pin	DATA3	B3	✓	
I/O pin	DATA4	B3	✓	
I/O pin	DATA5	B3	✓	
I/O pin	DATA6	B3	✓	
I/O pin	DATA7	B3	✓	
I/O pin	RDYnBSY	B3	✓	
I/O pin	CRC_ERROR	B3	✓	
I/O pin	CS	B8	✓	
I/O pin	*n*CS	B8	✓	
I/O pin	*n*RS	B8	✓	
I/O pin	*n*WS	B8	✓	
I/O pin	RUnLU	B8	✓	
I/O pin	PGM2	B3	✓	
I/O pin	PGM1	B3	✓	
I/O pin	PGM0	B3	✓	

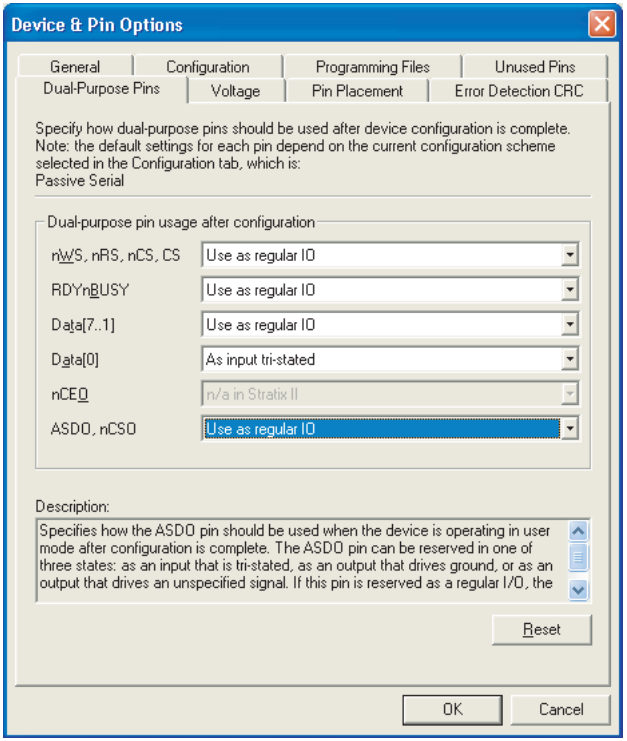
Table 8–21. Power Up and Configuration Pin Compatibility (Part 3 of 3)

Stratix II Pin Name		I/O Bank	HardCopy II Use	
Main Function	Optional Function		Main Function	Optional Function
I/O pin	ASDO	B3	✓	
I/O pin	*n*CSO	B3	✓	

Most optional configuration pins listed in Table 8–21 support the various configuration schemes available in Stratix II FPGAs. Parallel programming and remote update configuration modes utilize most of the pins in Table 8–21. HardCopy II devices are not configurable and do not support the Configuration Emulation mode. Therefore, Altera recommends that you minimize the configuration pin requirements of the Stratix II design; for example, by using the Passive Serial configuration mode.

If some of these dual-purpose pins are needed to configure the Stratix II FPGA, but will be unused after configuration, these pins will be completely unused on the HardCopy II device. Therefore, when migrating from the Stratix II device to the HardCopy II device, care must be taken when designing these pins on board. The removal of the Stratix II device and its corresponding configuration device may leave these pins floating on the HardCopy II device if such pins are assigned as inputs by the user, without any external means of driving them to a stable level. When selecting a Stratix II device and its device options, consider the after-configuration requirements of these pins and set them appropriately in the Quartus II software (Figure 8–10).

Figure 8–10. Device and Pin Options



For more information about HardCopy II power-up modes, refer to the *Power-Up Modes and Configuration Emulation in HardCopy Series Devices* chapter of the *HardCopy Series Handbook*.

Conclusion

HardCopy II devices provide a seamless migration path for Stratix II devices and supports the PLL, memory, logic, and I/O features offered on a Stratix II device. The HardCopy II device architecture also allows you to use a wide range of Stratix II devices for prototyping. HardCopy II devices offer pin-to-pin compatibility with Stratix II FPGAs, making HardCopy II devices drop-in replacements on systems designed with the Quartus II software and using Stratix II and HardCopy II companion devices. Use the Quartus II software to compile designs and determine available resources to guarantee fit and feature compatibility for Stratix II and HardCopy II companion devices.

More Information

For more information on migrating Stratix II designs to HardCopy II devices, Refer to the following sources:

- *HardCopy II Device Family Data Sheet* in the *HardCopy Series Handbook*
- *Quartus II Support for HardCopy II Devices*
- *Power-Up Modes and Configuration Emulation in HardCopy Series Devices* chapter in the *HardCopy Series Handbook*

Document Revision History

Table 8–22 shows the revision history for this chapter.

Table 8–22. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
September 2008, v1.4	Updated chapter number and metadata.	—
June 2007 v1.3	Changed “8K x 64” to “16K x 36” in Table 8–17.	—
	Completed typographical updates.	—
December 2006 v1.2	Added revision history.	—
March 2006	Formerly chapter 19; no content change.	—
October 2005 v1.1	Minor edits	—
May 2005 v1.0	Added document to the *HardCopy Series Handbook*.	—