

Arria V FPGA and SoC Features

View device ordering codes on [page 38](#).

| Product Line | Arria V GX FPGAs ¹ | | | | | | | | Arria V GT FPGAs ¹ | | | | Arria V GZ FPGAs ¹ | | | | Arria V SX SoCs ¹ | | Arria V ST SoCs ¹ | |
|--|---|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------------------------|-------------|-------------|-------------|-------------------------------|-----------|-----------|-----------|------------------------------|-------------------|------------------------------|-------------------|
| | 5AGXA1 | 5AGXA3 | 5AGXA5 | 5AGXA7 | 5AGXB1 | 5AGXB3 | 5AGXB5 | 5AGXB7 | 5AGTC3 | 5AGTC7 | 5AGTD3 | 5AGTD7 | 5AGZE1 | 5AGZE3 | 5AGZE5 | 5AGZE7 | 5ASXB3 | 5ASXB5 | 5ASTD3 | 5ASTD5 |
| Resources | | | | | | | | | | | | | | | | | | | | |
| LEs (K) | 75 | 156 | 190 | 242 | 300 | 362 | 420 | 504 | 156 | 242 | 362 | 504 | 220 | 360 | 400 | 450 | 350 | 462 | 350 | 462 |
| ALMs | 28,302 | 58,900 | 71,698 | 91,680 | 113,208 | 136,880 | 158,491 | 190,240 | 58,900 | 91,680 | 136,880 | 190,240 | 83,020 | 135,840 | 150,960 | 169,800 | 132,075 | 174,340 | 132,075 | 174,340 |
| Registers | 113,208 | 235,600 | 286,792 | 366,720 | 452,832 | 547,520 | 633,964 | 760,960 | 235,600 | 366,720 | 547,520 | 760,960 | 332,080 | 543,360 | 603,840 | 679,200 | 528,300 | 697,360 | 528,300 | 697,360 |
| M10K memory blocks | 800 | 1,051 | 1,180 | 1,366 | 1,510 | 1,726 | 2,054 | 2,414 | 1,051 | 1,366 | 1,726 | 2,414 | - | - | - | - | 1,729 | 2,282 | 1,729 | 2,282 |
| M20K memory blocks | - | - | - | - | - | - | - | - | - | - | - | - | 585 | 957 | 1,440 | 1,700 | - | - | - | - |
| M10K memory (Kb) | 8,000 | 10,510 | 11,800 | 13,660 | 15,100 | 17,260 | 20,540 | 24,140 | 10,510 | 13,660 | 17,260 | 24,140 | - | - | - | - | 17,290 | 22,820 | 17,290 | 22,820 |
| M20K memory (Kb) | - | - | - | - | - | - | - | - | - | - | - | - | 11,700 | 19,140 | 28,800 | 34,000 | - | - | - | - |
| MLAB memory (Kb) | 463 | 961 | 1,173 | 1,448 | 1,852 | 2,098 | 2,532 | 2,906 | 961 | 1,448 | 2,098 | 2,906 | 2,594 | 4,245 | 4,718 | 5,306 | 2,014 | 2,658 | 2,014 | 2,658 |
| Variable-precision DSP blocks | 240 | 396 | 600 | 800 | 920 | 1,045 | 1,092 | 1,156 | 396 | 800 | 1,045 | 1,156 | 800 | 1,044 | 1,092 | 1,139 | 809 | 1,090 | 809 | 1,090 |
| 18 x 18 multipliers | 480 | 792 | 1,200 | 1,600 | 1,840 | 2,090 | 2,184 | 2,312 | 792 | 1,600 | 2,090 | 2,312 | 1,600 | 2,088 | 2,184 | 2,278 | 1,618 | 2,180 | 1,618 | 2,180 |
| Clocks, Maximum I/O Pins, and Architectural Features | | | | | | | | | | | | | | | | | | | | |
| Processor cores (ARM Cortex-A9) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | Dual | Dual | Dual | Dual |
| Maximum CPU clock frequency (GHz) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 1.05 ² | 1.05 ² | 1.05 ² | 1.05 ² |
| Global clock networks | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| PLLs ³ (FPGA) | 10 | 10 | 12 | 12 | 12 | 12 | 16 | 16 | 10 | 12 | 12 | 16 | 20 | 20 | 24 | 24 | 14 | 14 | 14 | 14 |
| PLLs (HPS) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| I/O voltage levels supported (V) | 1.2, 1.5, 1.8, 2.5, 3.0, 3.3 ⁴ | | | | | | | | | | | | | | | | | | | |
| I/O standards supported | LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12 | | | | | | | | | | | | | | | | | | | |
| LVDS channels (receiver/transmitter) | 80/67 | 80/67 | 136/120 | 136/120 | 176/160 | 176/160 | 176/160 | 176/160 | 80/70 | 136/120 | 176/160 | 176/160 | 108/99 | 108/99 | 168/166 | 168/166 | 120/136 | 120/136 | 120/136 | 120/136 |
| Transceiver count (6.5536 Gbps) | 9 | 9 | 24 | 24 | 24 | 24 | 36 | 36 | 3 | 6 | 6 | 6 | - | - | - | - | 30 | 30 | 30 | 30 |
| Transceiver count (10.3125 Gbps) ⁵ | - | - | - | - | - | - | - | - | 4 | 12 | 12 | 20 | - | - | - | - | - | - | 16 | 16 |
| Transceiver count (12.5 Gbps) | - | - | - | - | - | - | - | - | - | - | - | - | 24 | 24 | 36 | 36 | - | - | - | - |
| PCIe hard IP blocks (Gen2 x4) | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 2 | 2 | 2 | - | - | - | - | 2 | 2 | 2 | 2 |
| PCIe hard IP blocks (Gen2 x8, Gen3) | - | - | - | - | - | - | - | - | - | - | - | - | 1 | 1 | 1 | 1 | - | - | - | - |
| GPIOs (FPGA) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 540 | 540 | 540 | 540 |
| GPIOs (HPS) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 208 | 208 | 208 | 208 |
| Hard memory controllers ⁶ (FPGA) | 2 | 2 | 4 | 4 | 4 | 4 | 4 | 4 | 2 | 4 | 4 | 4 | - | - | - | - | 3 | 3 | 3 | 3 |
| Hard memory controllers (HPS) | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 1 | 1 | 1 | 1 |
| Memory devices supported | DDR3, DDR2, DDR II+ ⁷ , QDR II, QDR II+, RDRAM II, RDRAM 3 ⁸ , LPDDR ⁷ , LPDDR2 ⁷ | | | | | | | | | | | | | | | | | | | |
| Package Options and I/O Pins: GPIO Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count | | | | | | | | | | | | | | | | | | | | |
| F672 pin (27 mm, 1.0 mm pitch) | 336 9,0 | 336 9,0 | 336 9,0 | 336 9,0 | - | - | - | - | 336 3,4 | - | - | - | - | - | - | - | - | - | - | - |
| H780 pin (29 mm, 1.0 mm pitch) | - | - | - | - | - | - | - | - | - | - | - | - | 342 12 | 342 12 | - | - | - | - | - | - |
| F896 pin (31 mm, 1.0 mm pitch) | 416 9,0 | 416 9,0 | 384 18,0 | 384 18,0 | 384 18,0 | 384 18,0 | - | - | 416 3,4 | 384 6,8 | 384 6,8 | - | - | - | - | - | 250, 208 12+0 | 250, 208 12+0 | 250, 208 12+6 | 250, 208 12+6 |
| F896 pin (31 mm, 1.0 mm pitch) | 320 9,0 | 320 9,0 | 320 9,0 | 320 9,0 | 320 9,0 | - | - | - | 320 3,4 | 320 3,4 | 320 3,4 | - | - | - | - | - | - | - | - | - |
| F1152 pin (35 mm, 1.0 mm pitch) | - | - | 544 24,0 | 544 24,0 | 544 24,0 | 544 24,0 | 544 24,0 | 544 24,0 | - | 544 6,12 | 544 6,12 | 544 6,12 | 414 24 | 414 24 | 534 24 | 534 24 | 385, 208 18+0 | 385, 208 18+0 | 385, 208 18+8 | 385, 208 18+8 |
| F1517 pin (40 mm, 1.0 mm pitch) | - | - | - | - | 704 24,0 | 704 24,0 | 704 36,0 | 704 36,0 | - | - | 704 6,12 | 704 6,20 | - | - | 674 36 | 674 36 | 540, 208 30+0 | 540, 208 30+0 | 540, 208 30+16 | 540, 208 30+16 |

Notes:
 1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
 2. 1.15 V operation.
 3. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
 4. 3.3 V compliant, requires a 3.0 V power supply.
 5. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels.
 6. With 16 and 32 bit ECC support.
 7. These memory interfaces are not available as Altera IP.
 8. This memory interface is only available for Arria V GZ devices.

336 9,0 For Arria V GX and GT devices, values on top indicate available user I/O pins and values at the bottom indicate the 6.5536 Gbps and 10.3125 Gbps transceiver count. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels. For Arria V GZ devices, values on top indicate available user I/O pins and values at the bottom indicate the 12.5 Gbps transceiver count.
250, 208 12+0 Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 6.5536 Gbps plus 10.3125 Gbps transceiver count.

