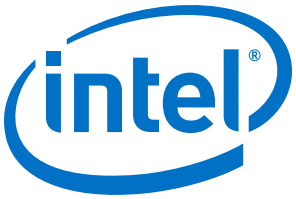

Arria 10 Transceiver CMU PLL IP Core Release Notes

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Contents

1 Arria 10 Transceiver CMU PLL IP Core Release Notes.....3
1.1 Arria 10 Transceiver CMU PLL IP Core v15.1 Revision History.....3
1.2 Arria 10 Transceiver CMU PLL IP Core v15.0 Revision History.....3
1.3 Arria 10 Transceiver CMU PLL IP Core v14.1 Revision History.....4
1.4 Arria 10 Transceiver CMU PLL IP Core v14.0 Revision History.....4
1.5 Arria 10 Transceiver CMU PLL IP Core v13.1 Revision History.....5

1 Arria 10 Transceiver CMU PLL IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Quartus Prime Design Suite Update Release Notes*.

Related Links

Quartus Prime Design Suite Update Release Notes

1.1 Arria 10 Transceiver CMU PLL IP Core v15.1 Revision History

Table 1. v15.1 November 2015

Description	Impact
Issue: ACDS 15.1 introduces a necessary fix for Arria 10 transceiver designs. This fix introduces a change that affects post-fit simulation for designs containing Arria 10 Transceiver Native PHY, Arria 10 Transceiver ATX PLL, Arria 10 Transceiver CMU PLL, and Arria 10 fPLL IP cores. `pll_powerdown` is not connected for HSSI PLL IPs. **Workaround:** Users requiring post-fit simulation of the transceiver PLLs in ACDS 15.1 need to disable the "Transceiver Reset Sequencer" for their design to produce a post-fit simulation netlist. However, this cannot and should not be used to produce the final bitstream for hardware. Hardware requires the "Transceiver Reset Sequencer" to be enabled. To disable the "Transceiver Reset Sequencer" in the Quartus Prime software, add the following QSF to the Quartus Settings File for the project: `set_global_assignment -name VERILOG_MACRO "ALTERA_XCVR_A10_ENABLE_ANALOG_RESETS=1"` This will completely disable the reset sequencer in the design and restore the old behavior. This method does not allow post-fit simulation of the "Transceiver Reset Sequencer" logic. **Resolution:** A modification to the PLL simulation models is planned for a subsequent release of ACDS 15.1 to remove the reset requirement.	`pll_powerdown` inputs to the Arria 10 Transceiver ATX PLL, Arria 10 Transceiver CMU PLL, and Arria 10 fPLL IP cores for Quartus Prime synthesis. As a result, the resulting generated post-fit simulation will not have a reset input connection for the PLL and post-fit simulation will likely fail.

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.2 Arria 10 Transceiver CMU PLL IP Core v15.0 Revision History

Table 2. v15.0 May 2015

Description	Impact
Removed the `hip_cal_done` port to avoid a fitter failure. Previously, this port was available when dynamic reconfiguration was enabled.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.3 Arria 10 Transceiver CMU PLL IP Core v14.1 Revision History

Table 3. v14.1 December 2014

Description	Impact
Verified in the Quartus II software v14.1	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.4 Arria 10 Transceiver CMU PLL IP Core v14.0 Revision History

Table 4. v14.0 Arria 10 Edition August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added support for Embedded debug feature. This feature enables you to write to the PLL control registers and read from status registers for the PLL instances in the design. This feature is available under the **Dynamic Reconfiguration** tab.	-
Added preset **GX 2500 Mbps Single Channel** for GX mode.	-
Changed the IP core to expose the `pll_cal_busy` port to the top level.	-
Changed the documentation link in IP Parameter Editor to refer to the *Arria 10 Transceiver PHY User Guide*.	-
Enhanced user warnings and information messages.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.5 Arria 10 Transceiver CMU PLL IP Core v13.1 Revision History

Table 5. v13.1 Arria 10 Edition December 2014

Description	Impact
Initial release for Arria 10 devices.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores