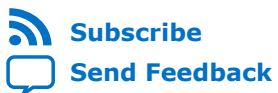




Intel[®] Acceleration Stack for Intel[®] Xeon[®] CPU with FPGAs Version 1.2.1 Release Notes

Updated for Intel[®] Acceleration Stack for Intel[®] Xeon[®] CPU with FPGAs: **1.2.1**



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Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs **DOES NOT** include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

About this Document

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 1.2.1 release.

Acronym List

Use the following table as a reference when reviewing the release notes.

Table 1. Acronyms

Acronyms	Expansion	Description
AFU	Accelerator Functional Unit	Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.
AF	Accelerator Function	Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream) in the Acceleration Stack installation directory tree and in source code comments.
ASE	AFU Simulation Environment	Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs.
FIM	FPGA Interface Manager	The FPGA hardware containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc. The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments. The Accelerator Function (AF) interfaces with the FIM at run time.
HSSI	High-speed Serial Interface	Reference to the multi-gigabit serial transceiver I/O in the FIM and the corresponding interface to the Accelerator Functional Unit (AFU).
OPAE	Open Programmable Acceleration Engine	The OPAE is a software framework for managing and accessing AFs.
PIM	Platform Interface Manager	An abstraction layer for managing top-level device ports and system-provided clock crossing.
PR	Partial Reconfiguration	The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function.



Minimum Requirements

The minimum requirements for the Intel Programmable Acceleration Card with Intel Arria® 10 GX FPGA must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 48 GB of free memory is a requirement only if you are compiling a hardware design
- Operating System:
 - Red Hat* Enterprise Linux* (RHEL) version 7.6
 - Ubuntu* version 18.04
- Board management controller (BMC) Firmware and Bootloader Version: 26895
- PACSign tool requires Python 3.0
- OPAE tools require Python 2.7
- OpenCL* RTE version 19.4.0.64



Intel Acceleration Stack Reference Table

Note: Intel recommends porting AFUs and workloads to the Intel Acceleration Stack v1.2.1. You must recompile and validate after you upgrade to the new release. The Intel Acceleration Stack v1.2.1 cannot be downgraded to previous versions.

Important: When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as 38d782e3-b612-5343-b934-2433e348ac4c.

Table 2. Intel Acceleration Stack Reference Table

Intel Acceleration Stack Version	FPGA Interface Manager (FIM) Version: Partial Reconfiguration (PR) Interface ID	OPAE Version	Intel Quartus® Prime Pro Edition ⁽¹⁾
1.2.1	38d782e3-b612-5343-b934-2433e348ac4c	1.1.2-2	19.2
1.2	69528db6-eb31-577a-8c36-68f9faa081f6	1.1.2	17.1.1
1.1	9926ab6d-6c92-5a68-aabc-a7d84c545738	1.0.2	17.1.1
1.0	ce489693-98f0-5f33-946d-560708be108a	0.13.1	17.0.0

⁽¹⁾ Use of the Intel Quartus Prime and related IP contained in this release is subject to the terms and conditions of the [End User License Agreement](#).

Intel Acceleration Stack v1.2.1 Enhancements

Table 3. New Feature List

Area	Enhancement
Operating System Support	<ul style="list-style-type: none"> • Ubuntu version 18.04, kernel 4.15 • RHEL version 7.6, kernel 3.10
Security Enhancements	<ul style="list-style-type: none"> • Root-of-Trust Implementation • Support for Intel MAX[®] 10 BMC firmware, Intel MAX 10 FPGA images and FPGA static region user image signing • New OPAE tools: <ul style="list-style-type: none"> – FPGA one-time secure update (<code>fpgaotsu</code>): Upgrades from unsecured MAX10 to a secured MAX10 – FPGA secure update (<code>fpgasupdate</code>): Remotely updates bitstreams securely. <code>fpgasupdate</code> replaces <code>fpgaflash</code>. – Super-RSU (<code>super-rsu</code>): Supports v1.2.1 package updates (Intel MAX 10 BMC firmware and FPGA image). – PACSign: Enables signing of bitstreams. To use this tool, you must have the capability to generate a public/private key pair and your hardware security module (HSM) must support a Public-Key Cryptography Standards (PKCS)#11 compatible application programming interface (API) to the PACSign tool.
Sample AFUs Supported	<p>The following unsigned AFU examples are provided with the Intel Acceleration Stack for Intel Xeon CPU with FPGAs:</p> <ul style="list-style-type: none"> • <code>dma_afu_unsigned.gbs</code> • <code>streaming_dma_afu_unsigned.gbs</code> • <code>eth_e2e_e10_unsigned.gbs</code> • <code>eth_e2e_e40_unsigned.gbs</code> • <code>hello_afu_unsigned.gbs</code> • <code>hello_intr_afu_unsigned.gbs</code> • <code>hello_mem_afu_unsigned.gbs</code> • <code>n1b_mode_0_unsigned.gbs</code> • <code>n1b_mode_0_stp_unsigned.gbs</code> • <code>n1b_mode_3_unsigned.gbs</code> <p><i>Note:</i> Each <code>*_unsigned.gbs</code> above is prepended with the necessary <code>block0</code> and <code>block1</code> headers but there are no hashes in these headers that have been signed with the root and code signing keys.</p>

Known Issues for the Intel Acceleration Stack v1.2.1

Table 4. Known Issues for the Intel Acceleration Stack v1.2.1

Known Issue	Details								
PCIe directed speed changes are not supported.	Only automatic down-training at boot time is supported.								
When an AFU workload exceeds board management controller sensor thresholds, the server may reboot.	<ul style="list-style-type: none"> An AFU workload may exceed the board management controller threshold before pacd can identify and act on the threshold violation. If this situation occurs, the board management controller removes the card from the PCIe bus and the server reboots before the pacd can perform a graceful shutdown. Workaround: None. Status: No planned fix. 								
Inconsistency in green_bs input port naming.	<ul style="list-style-type: none"> The names of the clock port inputs to the green_bs block do not correspond to resulting frequency provided from the dcp_io_pll block. 								
	<table border="1"> <thead> <tr> <th>dcp_io_pll port frequency provided to green_bs block clock input</th> <th>green_bs clock input port name</th> </tr> </thead> <tbody> <tr> <td>50 MHz</td> <td>Clk_100</td> </tr> <tr> <td>100 MHz</td> <td>Clk_200</td> </tr> <tr> <td>200 MHz</td> <td>Clk_400</td> </tr> </tbody> </table>	dcp_io_pll port frequency provided to green_bs block clock input	green_bs clock input port name	50 MHz	Clk_100	100 MHz	Clk_200	200 MHz	Clk_400
	dcp_io_pll port frequency provided to green_bs block clock input	green_bs clock input port name							
	50 MHz	Clk_100							
	100 MHz	Clk_200							
200 MHz	Clk_400								
The file can be found at a10_gx_pac_ias_1_2_1_pv/hw/lib/build/platform/green_bs.sv.									
<ul style="list-style-type: none"> Status: Fix targeted for a future version of the Intel Acceleration Stack. 									
setup_permissions.sh in OpenCL* prints error when connected to a virtual function in a virtual machine.	<ul style="list-style-type: none"> When you run the setup_permissions.sh script in a virtual machine to set permissions and system parameters for OpenCL, the following error displays: <pre>chmod: cannot access '/dev/intel-fpga-fme.*': No such file or directory.</pre> Virtual function does not have access to change permissions for FME sysfs entry files. Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack. 								
The fpgainfo error First Malformed Req returns 0xFFFFFFFFFFFFFFFF for streaming_dma_afu.gbs or dma_afu.gbs.	<ul style="list-style-type: none"> If you configure the streaming_dma_afu.gbs or dma_afu.gbs using fpgaconfig and then run fpgainfo errors, the command returns a First Malformed Req error of 0xFFFFFFFFFFFFFFFF. This error does not affect the functioning of the dma_afu or streaming_dma_afu block. Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack. 								
Virtual Function (VF) may fail to attach or detach when using the Linux Red Hat* 3.10 kernel.	The VF failure to attach or detach is a known issue with qemu/kvm and libvirt. Refer to the Red Hat website for more information about this issue.								

continued...



Known Issue	Details
<p>Packager issue with Ubuntu and compiling OpenCL kernels.</p>	<ul style="list-style-type: none"> Depending on the host environment setup, the packager tool may fail to run. This can prevent OpenCL kernel compiles on Ubuntu. Compiling OpenCL kernel in Ubuntu 18.04 fails with the following error: ERROR: packager tool failed to run. Check installation. Aborting compilation! Workaround: Edit the following file: <pre>\$OPAE_PLATFORM_ROOT/openccl/openccl_bsp/hardware/pac_a10/build/run.sh</pre> Change line: ADAPT_PACKAGER_BIN="python ./tools/packager.pyz" to ADAPT_PACKAGER_BIN="packager". Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>Flash fallback does not meet PCIe timeout.</p>	<ul style="list-style-type: none"> The host may hang or report a PCIe failure when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA. Workaround: Run the following super-rsu command to update the FPGA User image and BMC bootloader and firmware: <ul style="list-style-type: none"> For RHEL: <pre>sudo super-rsu /usr/share/opae/a10*/super*/*.json</pre> For Ubuntu: <pre>sudo super-rsu /usr/share/opae/a10-gx-pac/super-rsu/base/rsu-09C4.json</pre> Status: No planned fix.
<p>Unsupported transaction layer packet types.</p>	<ul style="list-style-type: none"> The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected. Workaround: None. Status: No planned fix.
<p>Board management controller does not verify the CRC in a PLDM request.</p>	<ul style="list-style-type: none"> The board management controller responds to PLDM packets regardless of the CRC value. Workaround: None. Status: No planned fix.
<p>Occasionally, <code>fgainfo</code> may not show the BMC version.</p>	<ul style="list-style-type: none"> Workaround: Power cycle the server. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>Limitation after updating the BMC image for 1000 times.</p>	<ul style="list-style-type: none"> After updating the BMC image in the on-chip flash for 1000 times, the subsequent use of <code>fgasupdate</code> will result in an I/O error. Workaround: Wait for 60 seconds before using the <code>fgasupdate</code> to update the BMC image. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>When <code>pacd</code> is triggered due to any of the sensors crossing the threshold, an error message is displayed during <code>pacd</code> process.</p>	<ul style="list-style-type: none"> Error messages: <pre>libopae-c sysfs.c:304:sysfs_write_u64() **ERROR** : Failed to write libopae-c reconf.c:217:clear_port_errors() **ERROR** : Failed to clear port errors libopae-c reconf.c:358:fpgaReconfigureSlot() **ERROR** : Failed to clear port errors</pre> You can ignore these error messages, they do not affect the functionality of <code>pacd</code>. Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>OpenCL kernels compiled for the Intel FPGA PAC with Intel Arria 10 GX may contain hold time violations.</p>	<ul style="list-style-type: none"> Workaround: Generate a new seed and recompile the kernel. For detailed instructions, refer to OpenCL on Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA Quick Start User Guide. Status: Fix targeted for a future version of the Intel Acceleration Stack.

continued...



Known Issue	Details
<p>The UNR threshold for 1.2v current reported by <code>pacd</code> is greater than the actual UNR for the sensor.</p>	<ul style="list-style-type: none"> This causes <code>pacd</code> to not handle graceful thermal shutdown as expected if UNR threshold for 1.2v current sensor is reached. Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>Incorrect message in <code>/var/log/messages</code>.</p>	<ul style="list-style-type: none"> You will observe the following messages: <pre>intel-pac-hssi intel-pac-hssi.0.auto: The HSSI config sysfs file is deprecated intel-pac-hssi intel-pac-hssi.0.auto: Please use the config_gsfp0 file instead</pre> <p>These messages can be ignored.</p> Workaround: Continue to use <code>hssi_mgmt/config sysfs</code> file with the provided ethernet design examples. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>Graceful shutdown is not supported when using a virtual machine.</p>	<ul style="list-style-type: none"> When a hypervisor is connected to a virtual function on a card, Intel PAC daemon (<code>pacd</code>) cannot perform graceful shutdown when the sensor thresholds are exceeded. In this case, the hypervisor and server reboot. This is a known limitation. Workaround: None. Status: No future plan to fix. <p>For more information, refer to the Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA.</p>
<p>When virtual functions (VF) or physical functions (PF) send multiple unaligned read or write requests to the Intel PAC with Intel Arria 10 GX FPGA registers, the host reboots.</p>	<ul style="list-style-type: none"> This issue only exists when using Red Hat Enterprise Linux (RHEL) version 7.6 Kernel 3.10.0-957. Workaround: None available. Status: This limitation is addressed in newer Linux kernels. Intel recommends upgrading from the Red Hat* Enterprise Linux (RHEL) version 7.6 Kernel 3.10.0-957 kernel. No fixes are planned for this version of the kernel.
<p>A typo in <code>board_env.xml</code>, listing the Intel Quartus Prime software version as 17.1.</p>	<ul style="list-style-type: none"> This issue does not cause any failures and can be ignored. Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>FPGA Client Driver (FCD) file names for Intel PAC with Intel Arria 10 GX FPGA and Intel FPGA PAC D5005 are identical.</p>	<ul style="list-style-type: none"> This may cause an error in linking the memory-mapped device (MMD) libraries if you change the installation of the Intel PAC with Intel Arria 10 GX FPGA to Intel FPGA PAC D5005 or vice versa. <p>To avoid this issue, ensure that the FCD file points to the MMD library (<code>libintel_opae_mmd.so</code>) from the intended <code>opencl_bsp</code> directory. Run the following command to verify:</p> <pre>cat /opt/Intel/OpenCL/Boards/dcp_bsp.fcd</pre> <p>Desired output:</p> <pre>\$OPAE_PLATFORM_ROOT/opencl/opencl_bsp/linux64/lib/libintel_opae_mmd.so</pre> <p>where the <code>\$OPAE_PLATFORM_ROOT</code> must point to your intended installation directory. For more information about installing the OpenCL BSP and setting up FCD file, refer to the OpenCL on Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA Quick Start User Guide.</p> <ul style="list-style-type: none"> Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack.
<p>The command <code>aocl diagnose reports Installable Client Driver (ICD) test</code> as failed.</p>	<ul style="list-style-type: none"> Workaround: Manually run the following two commands to copy the ICD files: <pre>sudo cp \$INTELFPGAOCLESDKROOT/Altera.icd /etc/OpenCL/vendors/</pre> <pre>sudo cp \$INTELFPGAOCLESDKROOT/Intel_FPGA_SSG_Emulator.icd /etc/OpenCL/vendors/</pre> Status: Fix targeted for a future version of the Intel Acceleration Stack.

continued...



Known Issue	Details
<p>pacd occasionally fails to start after cold or warm reboot.</p>	<ul style="list-style-type: none"> • If pacd is started as a systemd service and followed by a warm or cold reboot, pacd can occasionally fail to start. • Workaround: <ol style="list-style-type: none"> 1. If a warm or cold reboot is performed after setting up pacd as a systemd service, ensure pacd is running after the reboot. Otherwise, follow these steps (you must have root access to perform these steps): <ol style="list-style-type: none"> a. Remove the pacd lock file using: <pre style="background-color: #f0f0f0; padding: 2px;">sudo rm -f /tmp/pacd.lock</pre> b. Restart the pacd service with <code>systemctl start pacd.service</code> 2. Modify the pacd.service file: <ul style="list-style-type: none"> — Replace the line: <code>RestartPreventExitStatus=1</code> with <code>ExecStopPost=/bin/rm -f /tmp/pacd.lock</code> • Status: Fix targeted for a future version of the Intel Acceleration Stack.

Known Issues for the Intel Acceleration Stack v1.2.1 AFU Design Examples

Table 5. Known Issues for the Intel Acceleration Stack v1.2.1 AFU Design Examples

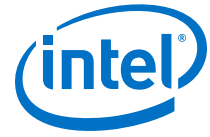
Known Issue	Details
Streaming DMA only supports access to host memory.	<ul style="list-style-type: none"> The streaming DMA basic building blocks (BBBs) can access host or FPGA memory, but the driver does not provide any means for accessing FPGA memory. Status: This limitation will be fixed in a future version of the driver.
DMA AFU test application does not compile for simulation.	<ul style="list-style-type: none"> Workaround: Include the following header in the <code>fpga_dma_test.c</code> file: <pre>#include <unistd.h></pre> Status: Fix targeted for a future version of the Intel Acceleration Stack.
DMA AFU simulation ends abruptly due to memory scheduling conflict.	<ul style="list-style-type: none"> Error message: <pre>ase_top.ase_top_generic.local_mem_model.b_emul[0].emif_ddr4.av5_bfm_inst_ddra.drive_response: Response transaction 33, cycle 3 - schedule conflict</pre> Workaround: None. Status: Fix targeted for a future version of the Intel Acceleration Stack.
Streaming DMA AFU fails to compile for simulation.	<ul style="list-style-type: none"> Workaround: To compile the AFU, comment out or modify the below lines in the Makefile: <pre>#CXXFLAGS += -D FPGA_DMA_DEBUG=0 -g -O2 -fPIC -D EMU_MODE=0 -Wall - Wno-unknown-pragmas -I\$(TBB_HOME)/include -fpermissive -std=c++11 CXXFLAGS += -D FPGA_DMA_DEBUG=0 -g -O2 -fPIC -D EMU_MODE=0 -Wall - Wno-unknown-pragmas -fpermissive -std=c++11 #LDFLAGS += -L\$(TBB_HOME)/lib/intel64_lin/gcc4.7/ #LDFLAGS += -L\$(TBB_LIB)</pre> Status: Fix targeted for a future version of the Intel Acceleration Stack.
Streaming DMA AFU does not work in simulation.	<ul style="list-style-type: none"> Streaming DMA AFU fails to generate simulation file due to a hardcoded path. Workaround: Update the line paths on lines 6031 and 10283 in <code>streaming_dma_test_system.qsys</code> from <code>/data/dunnikri/qshell/18.0.1/p4/afu/samples</code> to <code>../..</code> Status: Fix targeted for a future version of the Intel Acceleration Stack.



Resolved Issues from v1.2 to v1.2.1

Table 6. Issues Resolved from v1.2 to v1.2.1 of the Intel Acceleration Stack Software

Issue	Description
Invalid memory read fault may cause FIM to lock.	<ul style="list-style-type: none"> Running an AFU at this instance might return <i>accelerator not found</i>. The <code>fpgainfo</code> error indicates Non-Fatal and CompStat error (completion status error). The FIM locks after the AFU sends a memory read to invalid address. Workaround: Power cycle the system to reinitialize the Intel PAC with Intel Arria 10 GX FPGA and recover from this issue. Refer to the Knowledge Base entry for more information. Status: Fixed in the Intel Acceleration Stack v1.2.1.
Possible corruption of board management controller firmware during an in-band update.	<ul style="list-style-type: none"> The board management controller firmware may be corrupted when performing an in-band update using <code>fpgaflash</code>. This event prevents the Intel PAC with Intel Arria 10 GX FPGA from booting after the update. Workaround: The current installer implements a workaround that checks for data corruption and retries an update up to three times. If the update continues to fail after the three attempts you must relaunch the <code>fpgaflash</code> command without rebooting your host. Status: Fixed in the Intel Acceleration Stack v1.2.1.
The BMC may return incorrect sensor data.	<ul style="list-style-type: none"> The BMC may return incorrect sensor data to the <code>pacd</code> and <code>fpgainfo</code> tool. This incorrect data may cause <code>pacd</code> to interrupt the execution of applications using the Intel Programmable Acceleration Card (PAC) resulting in a system reboot. Workaround: No workaround available. Status: Fixed in the Intel Acceleration Stack v1.2.1.



Intel Acceleration Stack Release Notes Archives

Intel Acceleration Stack Version	User Guide
1.2	Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.2 Release Notes
1.1	Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.1 Release Notes
1.0	Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.0 Release Notes

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Intel Acceleration Stack for Intel Xeon CPU with FPGAs v1.2.1 Release Notes Revision History

Date	Acceleration Stack Version	Changes
2020.03.06	1.2.1 (compatible with Intel Quartus Prime Pro Edition 19.2)	<ul style="list-style-type: none"> Updated the following sections: <ul style="list-style-type: none"> – <i>Minimum Requirements</i> – <i>Intel Acceleration Stack Reference Table</i> – <i>Intel Acceleration Stack v1.2.1 Enhancements</i> – <i>Known Issues for the Intel Acceleration Stack v1.2.1</i> – <i>Resolved Issues</i> – <i>Intel Acceleration Stack Release Notes Archives</i> Added a new section: <i>Known Issues for the Intel Acceleration Stack v1.2.1 AFU Design Examples</i>
2019.03.08	1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Added known issue "Using <code>pacd</code> may result in false failures."
2019.02.23	1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Added note about upgrading to the Intel Acceleration Stack v1.2 in the <i>Intel Acceleration Stack Reference Table</i> section.
2018.12.04	1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Initial release.

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