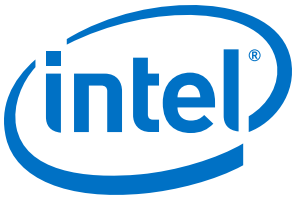

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 1.1 Release Notes

Intel FPGA Programmable Acceleration Card N3000

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.1**

RN-1219 | 2019.11.25
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Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs **DOES NOT** include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.1 Release Notes

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 1.1 for the Intel FPGA Programmable Acceleration Card N3000.

Minimum Requirements

The minimum requirements for the Intel FPGA PAC N3000 must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 48 GB of free memory (Intel Quartus® Prime Pro Edition software requires at least 48 GB for compiling a design targeting an Intel Arria® 10 FPGA device)
- Operating System:
  - Red Hat* Enterprise Linux* (RHEL) version 7.6 kernel 3.10
  - CentOS Linux version 7.6 kernel 3.10 or 4.19
- PACsign requires Python 3.6

Supported Features

Table 1. Features of the Intel Acceleration Stack v1.1 for Intel FPGA PAC N3000

Feature	Description
Configurations	• 2x2x25 GbE • 4x25 GbE • 8x10 GbE
OPAE	• FPGA enumeration • FME device access • AFU device access • FPGA memory-mapped I/O (MMIO) register access • Access Intel MAX® 10 board management controller (BMC) over SPI bus • Voltage and power monitoring through OPAE commands • Memory test over DMA • Network loopback (NLB) test • Graceful shutdown support using the `fpgad` tool • SEU detection • Data Plane Development Kit (DPDK) support

continued...

Feature	Description
Runtime and Development Installers	Enables easy installation of the release package for Intel FPGA PAC N3000
Security	• Intel MAX 10 Root-of-Trust Implementation • Support for Intel MAX 10 BMC firmware, Intel MAX 10 FPGA images and FPGA static region user image signing • New OPAE security tools: — FPGA one-time secure update (`fpgaotsu`): Upgrades from unsecured MAX10 to a secured MAX10 — FPGA secure update (`fpgasupdate`): Remotely updates bitstreams securely. `fpgasupdate` replaces `fpgaflash`. — Super-RSU (`super-rsu`): Supports v1.1 package updates (Intel MAX 10 BMC firmware and FPGA image). — PACSign: Enables signing of bitstreams. To use this tool, you must have the capability to generate a public/private key pair and your hardware security module (HSM) must support a Public-Key Cryptography Standards (PKCS)#11 compatible application programming interface (API) to the PACSign tool.
Programmable Forward Error Correcting (FEC)	Allows you to program the C827 Re-timers with Reed Solomon FEC (IEEE 802.3 Clause 108), Fire Code FEC (IEEE 802.3 Clause 74), or no-FEC for 25 GbE interfaces.

Intel Acceleration Stack v1.1 for Intel FPGA PAC N3000 Reference Table

The following table provides key firmware (FW) versions for this release. To identify the current firmware version in your Intel FPGA PAC N3000, use the OPAE command: `fpgainfo fme`.

Note: Only install OPAE tools and drivers that correspond to your specific software package.

Table 2. Reference Table

Design Configuration	PR Interface ID	Bitstream ID	Intel MAX 10 NIOS FW	Intel MAX 10 Build
2x2x25 GbE	a5d72a3c-c8b0-4939-912c-f715e5dc10ca	0x23000410010309	D.2.0.19	D.2.0.6
4x25 GbE	f3c99413-5081-4aadbced-07eb84a6d0bb	0x23000110010309	D.2.0.19	D.2.0.6
8x10 GbE	901dd697-ca79-4b05-b843-8138cefa2846	0x23000010010309	D.2.0.19	D.2.0.6

Known Issues

Table 3. Known Issues in Intel Acceleration Stack v1.1 for Intel FPGA PAC N3000

Known Issue	Details

`fpgainfo mac` command does not report correct MAC address.
This issue only applies to Intel FPGA PAC N3000 that is pre-production and has been upgraded to the Intel Acceleration Stack production version.
	• `fpgainfo mac` reports FFFFFFFF instead of correct MAC address as a card serial number.
	• Workaround: You can obtain the source MAC address using the following command:
	`$ ip link show <XL710 Interface Name>`
	For example:
	`$ ip link show p4p1`
	`92: p4p1: <BROADCAST,MULTICAST,UP,LOWER_UP> mtu 1500 qdisc mq state UP mode DEFAULT group default qlen 1000`
	`link/ether 64:4c:36:11:07:30 brd ff:ff:ff:ff:ff:ff`
	• Status: This limitation is fixed in the production version of the Intel FPGA PAC N3000.

DDR4 accesses with a burstcount of 64 are not supported.	• Burstcounts of 1, 2, 4, 8, 16 and 32 are supported. • Workaround: None. • Status: No planned fix.

False errors are reported when installing a configuration package.	• You may encounter an error similar to this 2x2x25 GbE report when installing configuration packages:
	`error running: ['yum', 'info', 'opae-one-time-update-n3000-25G.noarch']`
	`error running: ['yum', 'info', 'opae-super-rsu-n3000-2x2x25G.noarch']`
	You can ignore these errors.
	• Workaround: None.
	• Status: No planned fix.

Intel provided factory FPGA images may incur packet loss in FPGA when all ports are active and the packet size is not a multiple of 64.	• The provided FPGA factory images are intended to demonstrate all interfaces. The internal clock rate is not set for dropless packet transfer for all packet sizes. For more details on expected packet drop measurements for the baseline images, refer to Appendix: Intel Provided FPGA Factory Image Packet Drop on page 11. • Workaround: While using an aggregated internal packet bus for your Intel FPGA PAC N3000 design, set the clock rate to 285 MHz to have no packet drops for all packet sizes. The disaggregated and lightweight packet bus implementation options do not have this issue. • Status: No planned fix.
`fpgainfo bmc` may not return QSFP Supply Voltage if your QSFP module does not support supply voltage registers.	• The Intel MAX 10 BMC obtains the QSFP module voltage sensor value from the Supply Voltage registers beginning at offset 26, as listed in the Free Side Monitoring Values, Table 6-7, of the SFF-8636 Specification for Management Interface for 4-lane Modules and Cables, rev 2.10a. • Workaround: If your QSFP module does not support this register, please disregard the value returned by the Intel MAX 10 BMC when using the `fpgainfo bmc` command. • Status: No planned fix.

Resolved Issues

Table 4. Resolved Issues from Intel Acceleration Stack v1.1 Beta to Production for the Intel FPGA PAC N3000

Known Issue (Resolved)	Details
The link-up or link-down LED indicators are not reliable for 8x10G image.	• Workaround: None. • Status: This limitation is fixed in the production version of the Intel Acceleration Stack for the Intel FPGA PAC N3000.
First occurrence of error injection doesn't trigger interrupt correctly.	• Workaround: Perform initial injection and ignore lack of interrupt. Follow on injection works as expected. • Status: This limitation is fixed in the production version of the Intel Acceleration Stack for the Intel FPGA PAC N3000.
After configuring the Intel Arria 10 GT with the FPGA image (2x2x25G and 4x25G), the link up LED may show YELLOW, indicating 10G link up rather than 25G link up. You may also see that the LEDs are ON regardless of link up.	• Workaround: None. • Status: This limitation is fixed in the production version of the Intel Acceleration Stack for the Intel FPGA PAC N3000.
In 8x10G mode, the Ethernet jumbo frames (frames of length greater than 1518 Bytes) are not supported.	• Workaround: None. • Status: This limitation is fixed in the production version of the Intel Acceleration Stack for the Intel FPGA PAC N3000.
Insufficient resources after remote system update (RSU) when using the Intel XL710 Virtual Functions.	• Workaround: Power cycle the server. • Status: This limitation is fixed in the production version of the Intel Acceleration Stack for the Intel FPGA PAC N3000.

Component Information

Ensure you review the reference materials for the following Intel FPGA PAC N3000 components.

Broadcom* PEX8747 PCIe* Switch

Intel performs PCIe* compliance testing for the Intel FPGA PAC N3000. The following PCIe compliance tests are known to start in an invalid state when run on the Intel FPGA PAC N3000.

Note: None of the following PCIe compliance test failures affect the PCIe functionality or the Intel FPGA PAC functionality.

Table 5. PCIe Compliance Test Failures

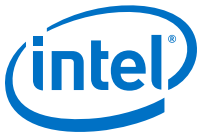
PCIe Compliance Test	Test Failure Reference
TD_1_42_ACS Extended Cap Structure Test	-
TD_1_50 Slot Capabilities2, Control2, and Status2 Registers Test	-
TD_2_7_Link Speed Test (2.5, 5.0, 8.0)	Broadcom* PEX 8749/48/47/33/32/25/24/23/17/16/13/12 Errata Refer to ***1.32*** *PEX 87xx Downstream Port Incorrectly Sets Link Status Register's "Link Autonomous Bandwidth Status" Bit for any Successful Speed Change Event*.
TD_2_9 Software Requested Link Equalization Test (2.5, 5.0, 8.0)	Broadcom PEX 8749/48/47/33/32/25/24/23/17/16/13/12 Errata Refer to ***1.32*** *PEX 87xx Downstream Port Incorrectly Sets Link Status Register's "Link Autonomous Bandwidth Status" Bit for any Successful Speed Change Event*.
Preset Configuration Test	Broadcom PEX 8749/48/47/33/32/25/24/23/17/16/13/12 Errata Refer to ***1.19*** *PEX 87xx Port Does Not Reject Illegal Coefficients for the Specified Condition*.
Gen 1 Rx Test	-

Related Information

- PCI*Express Architecture Configuration Space Test Specification Revision 3.0
  For more information about specific PCIe compliance tests.
- PCI*Express Architecture Link Layer and Transaction Layer Test Specification Revision 3.0
  For more information about specific PCIe compliance tests.

Intel Ethernet Controller XL710

Limitation	Details
For packets below 160 bytes, there is a hardware packet processing limit for the entire device of ~37 Mpps.	Refer to section *Intel® Ethernet Controller X710/ XXV710/XL710 Throughput Limit* in document: Intel® Ethernet Controller X710/ XXV710/XL710 Specification Update.
The Intel XL710 Ethernet controller on the Intel FPGA PAC N3000 does not support Wake-On-LAN.	-



Supported Software

The following software packages support the Intel FPGA PAC N3000. Ensure that you review the following references to comprehend any known issues.

Data Plane Development Kit (DPDK)

If you use the libraries contained in the Data Plane Development Kit, please refer to the version 19.08 release notes for latest information on features and known issues.

Related Information

DPDK v19.08 Release Notes

Intel Network Adapter Drivers

Intel provides drivers for the Intel Ethernet Controller XL710-BM2.

Table 6. Intel Ethernet Controller XL710-BM2 Driver Versions

Driver	Version
Intel Network Adapter Driver for PCIe 40 Gigabit Ethernet Network Connections under Linux	2.9.21
Intel Network Adapter Virtual Function Driver for Intel 40 Gigabit Ethernet Network Connections	3.7.53

Related Information

- Network Adapter Driver for PCIe 40 Gigabit Ethernet Network Connections Under Linux Support Page
- Intel Network Adapter Virtual Function Driver for Intel 40 Gigabit Ethernet Network Connections Support Page

Revision History for Intel Acceleration Stack for Intel Xeon CPU with FPGAs v1.1 Release Notes

Document Version	Changes
2019.11.25	Initial Release.

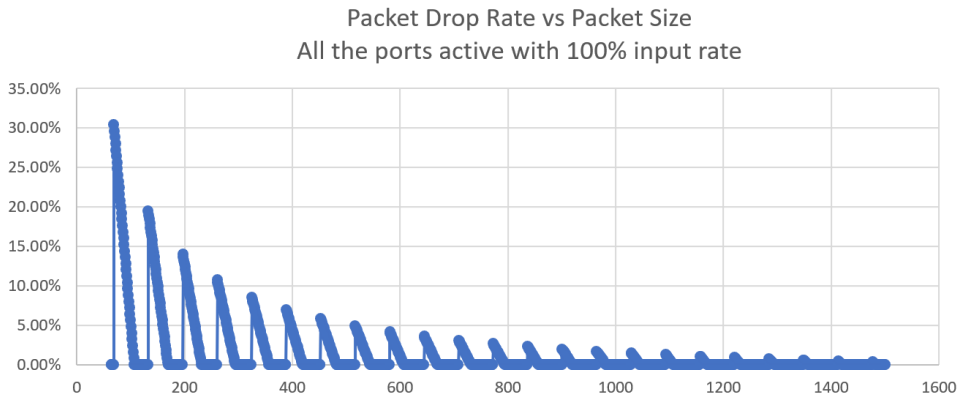
Appendix: Intel Provided FPGA Factory Image Packet Drop

The FPGA factory image multiplexes all the Ethernet ports into one 512-bit (64 byte) bus. This bus has enough bandwidth to transport all the Ethernet ports when the packet size is a multiple of 64 bytes. When packet sizes are not multiples of 64 bytes, the last transfer of the packet on the bus carries the remainder of packet and the unused byte lanes do not carry valid data. For these packets, the bus does not have sufficient bandwidth to carry all traffic for some packet sizes. As a result of lack of bandwidth, the packet drops.

During internal tests, if all ports are active with fixed size packets that are not multiples of 64 bytes, some packet loss may occur. The worst case is 69-byte packets where the cyclic redundancy check (four bytes) is stripped off, resulting in 65 bytes transferred on the internal bus. This packet transfer takes two clock cycles. The first clock cycle transfers 64 bytes and the second clock cycle transfers one byte.

The following figure shows the predicted packet loss rate for the 2x2x25G and 4x25G network configurations when all the ports have 100% input capacity and same packet size.

Figure 1. Predicted Packet Loss Rate for 2x2x25G and 4x25G Configurations



The following figure shows the predicted packet loss rate for the 8x10G network configuration when all the ports have 100% input capacity and same frame size. Packet loss only occurs for packet sizes between 69 bytes to 82 bytes.

Figure 2. Predicted Packet Loss Rate for 8x10G Configuration