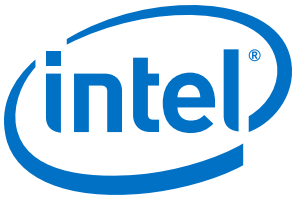

Serial Lite III Streaming Intel FPGA IP Core Release Notes

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Contents

1. Serial Lite III Streaming Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

Intel Quartus Prime Design Suite Update Release Notes

1.1. Serial Lite III Streaming Intel FPGA IP Core v18.1

Table 1. v18.1 September 2018

Description	Impact
Added E-Tile transceiver support up to 28.0 Gbps data rate with x4 lane. *Note:* The Serial Lite III Streaming IP with E-Tile transceiver supports only duplex core.	—
Added the following configuration and status registers: • TX Indirect Address • TX MAC Status • TX Lane#N MAC Status • TX Lane#N PCS Status • RX Indirect Address • RX MAC Status • RX Lane#N MAC Status • RX Lane#N PCS Status	—
Added the following bits in RX Error Status Register and RX Error Interrupt Enable Register: • Bit 11: RX Data Error • Bit 7: RX Adaptation FIFO Overflow • Bit 11: RX Data Error Interrupt Enable • Bit 7: RX Adaptation FIFO Overflow Interrupt Enable	—
Removed the following bits in RX Error Status Register and RX Error Interrupt Enable Register: • Bit 2: RX Loss of Frame Lock • Bit 2: RX Loss of Frame Lock Interrupt Enable	—
Riviera-PRO* simulator is not supported for Serial Lite III Streaming IP with E-Tile transceiver.	—
Added simulation, compilation, and hardware design example for Serial Lite III Streaming IP with E-Tile transceiver.	—

Related Information

- Serial Lite III Streaming Intel FPGA IP Core User Guide
- Errata for Serial Lite III Streaming Intel FPGA IP core in the Knowledge Base

- Intel FPGA Serial Lite III Streaming IP Core Design Example User Guide for Intel® Stratix® 10 Devices
- Intel® Arria® 10 Serial Lite III Streaming IP Core Design Example User Guide

1.2. SerialLite III Streaming Intel FPGA IP Core v18.0

Table 2. v18.0 May 2018

Description	Impact
Support 28 Gbps data rate with x4 lane for Intel® Stratix® 10 devices.	—
Sink core variation is now supported for more than 17.4 Gbps data rate in Intel Stratix 10 devices.	—
New Xcelium simulator tool support for Intel Stratix 10 and Intel Arria® 10 devices.	—
Renamed Intel FPGA SerialLite III Streaming IP core to the following IP core names per Intel rebranding: • Intel Stratix 10 devices: SerialLite III Streaming IP core to SerialLite III Streaming Intel FPGA IP core • Intel Arria 10 devices: Arria 10 SerialLite III Streaming IP core to SerialLite III Streaming Intel Arria 10 FPGA IP core • Stratix V and Arria V devices: SerialLite III Streaming IP core to SerialLite III Streaming Intel FPGA IP core	—

Related Information

- SerialLite III Streaming Intel FPGA IP Core User Guide
- Errata for SerialLite III Streaming Intel FPGA IP core in the Knowledge Base
- Intel FPGA SerialLite III Streaming IP Core Design Example User Guide for Intel Stratix 10 Devices
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide

1.3. Intel FPGA SerialLite III Streaming IP Core v17.1

Table 3. v17.1 November 2017

Description	Impact
Added support for Intel Stratix 10 devices. New features include: • 28 Gbps data rate with x1 lane and 25 Gbps data rate with x2 lane . • Basic and full streaming mode.	—
No simplex receiver mode support for more than 17.4 Gbps data rate in Intel Stratix 10 devices.	Simplex receiver mode for greater than 17.4 Gbps data rate in Intel Stratix 10 will be supported in future release.
In previous versions of the Intel FPGA SerialLite III Streaming IP core design example] for Intel Arria 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs required additional constraints. This issue has been fixed in Intel Quartus® Prime version 17.1.	If you are migrating earlier designs with these additional constraints to Intel Quartus Prime version 17.1, refer to the How to I compensate for the jitter of PLL cascading or non-dedicated clock path for

continued...

Description	Impact
	Arria 10 PLL reference clock? KDB link for more information.
SerialLite III Streaming IP core in Intel Stratix 10 devices does not support Riviera™-Pro 2017.02 simulator.	You may use Riviera-Pro simulator prior to 2017.02 version.

Related Information

- Intel FPGA SerialLite III Streaming IP Core User Guide
- Errata for Intel FPGA SerialLite III Streaming IP core in the Knowledge Base
- Intel FPGA SerialLite III Streaming IP Core Design Example User Guide for Intel Stratix 10 Devices
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide

1.4. SerialLite III Streaming IP Core v17.0

Table 4. v17.0 May 2017

Description	Impact
Design Example for Stratix 10 SerialLite III Streaming: • Added new hardware testing operations for standard clocking mode: — **Enable Slave Test Mode** Selecting this option disables the traffic generator/checker and enables the traffic to flow from sink to source. — **Disable Slave Test Mode** Selecting this option disables data flow from sink to source.	—

Related Information

- SerialLite III Streaming IP Core User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

1.5. SerialLite III Streaming IP Core v16.1

Table 5. v16.1 October 2016

Description	Impact
Added support for Stratix 10 devices.	—

Related Information

- SerialLite III Streaming IP Core User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

1.6. SerialLite III Streaming IP Core v16.0

Table 6. v16.0 May 2016

Description	Impact
Added a new parameter—**Enable Transceiver Native PHY ADME**.	—
New *Example Design* tab in the IP parameter editor.	Automatically generates both simulation and hardware design examples with the parameters you specify.
Renamed the parameter names in the IP parameter editor.	—
Support automatic generation of basic SignalTap® II Logic Analyzer files.	Simplifies generation of files for debugging.

Related Information

- SerialLite III Streaming IP Core User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

1.7. SerialLite III Streaming IP Core v15.1

Table 7. v15.1 November 2015

Description	Impact
Added a new parameter—**Burst Gap**.	—
For Arria 10 devices, the PMA width for Interlaken mode is changed to 64 bits.	IP Upgrade is compulsory if you are using Arria 10 devices. For Arria 10 devices, automatic upgrade will fail for IP core that uses Standard Clocking mode and was generated in a prior version of the Quartus II software. You must uncheck the **Auto Upgrade** option and click **Upgrade in Editor** to select a valid Transceiver Reference Clock frequency if the existing selection is invalid. For Stratix V and Arria V GZ devices, these changes are optional. If you do not upgrade your IP core, it does not have these new features.
For Arria 10 devices, the I/O PLL replaces the fractional PLL (fPLL) in generating the core clock and user clock signals.	
Updated the bit function in the `error_tx` signal.	
Updated the design example to support Arria 10 devices.	

Related Information

- SerialLite III Streaming IP Core User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

1.8. SerialLite III Streaming IP Core v15.0

Table 8. v15.0 May 2015

Description	Impact
Updated `sync_tx` and `sync_rx` signal bus width to 8-bits.	–
Design example now supports simulation testbench based on user configurations in the Seriallite III Streaming IP core parameter editor.	–

Related Information

- SerialLite III Streaming MegaCore Function User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base

1.9. SerialLite III Streaming IP Core v14.1

Table 9. Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added support for 17.4 Gbps data rate in variations that target an Arria 10 device. In the parameter editor, added support for the value of 17.4 Gbps for the **Transceiver data rate per lane** parameter in variations that target an Arria 10 device.		

Related Information

- SerialLite III Streaming MegaCore Function User Guide
- Errata for SerialLite III Streaming IP core in the Knowledge Base