
Streaming Multichannel Uncompressed Video in the Broadcast Environment

Designing video equipment for streaming multiple uncompressed video signals is a new challenge, especially with the demand for high-definition video streams. This white paper examines how a multichannel streaming PCIe DMA controller and other “building block” IP cores are combined within a Cyclone IV GX FPGA to support SD- and HD-SDI applications using an open-source video packet streaming-format protocol such as those used in non-linear editors, video servers, and video-capture applications.

Introduction

The advent of highly integrated digital circuits and powerful processors enabled the digitization of video, which in turn brought about a revolution in the streaming of both compressed and uncompressed video. In addition, the digital video data rate is increasing to accommodate the wider bandwidth required for high-definition (HD) applications. These changes translate into a requirement for more signal processing power.

Altera® Cyclone® IV GX FPGAs, with on-chip transceiver I/Os at speeds up to 3.125 Gbps, support the triple-rate serial digital interface (SDI) protocol from standard definition (SD) to HD at 1080p. Other video application protocols supported include Gigabit Ethernet (GbE), DisplayPort, and V-by-One (Vx1). Cyclone IV GX FPGAs also include an embedded PCI Express (PCIe) hard IP block that reduces FPGA resource usage and design time.

Video Streaming Background

Streaming video may involve either on-demand or live broadcast of compressed or uncompressed video. Most broadcast studio applications rely on uncompressed SDI to move video within the studio, typically between switchers, servers, and cameras, while compressed video streams are used in certain studio applications for video over Internet protocol. Uncompressed video streams provide low delay and provide for reduced compression artifacts. Compressed video may have more technical issues such as jitter, latency, and the loss of quality.

Video streaming consists of three steps:

1. Convert the incoming SDI stream into the 20-bit parallel domain
2. Convert the parallel signal to another interface standard, such as PCIe or Ethernet
3. Assign the video stream to a final destination

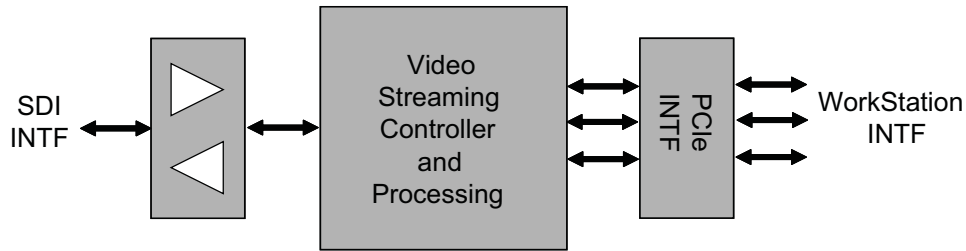
Broadcast Studio Trends

The transition to HD, and now to 1080p using 3G-SDI, is one of the latest broadcast technology trends. Another is implementation of tapeless workflows that offer integrated production and content management for multichannel and multiplatform applications. A tapeless workflow can stream video from ingest to playout while relying on the integration of production video servers, central storage, and related production management software.

A file-based workflow permits the development of a tapeless work environment. This solution provides flexibility and better management of ingested video as it is edited and finally uploaded to a broadcast server's playout device. A file-based system suits applications such as IP-based newsgathering, streaming to the Internet, and live and on-demand video streaming.

For now, it appears that triple-rate SDI data will be the typical interface used in tapeless and file-based systems. In this scenario, the SDI video is converted to a file format that can be edited in a workstation. [Figure 1](#) shows a PCIe bus used to receive and transmit the converted video stream to and from the SDI domain.

Figure 1. Tapeless and File-Based Video Streaming

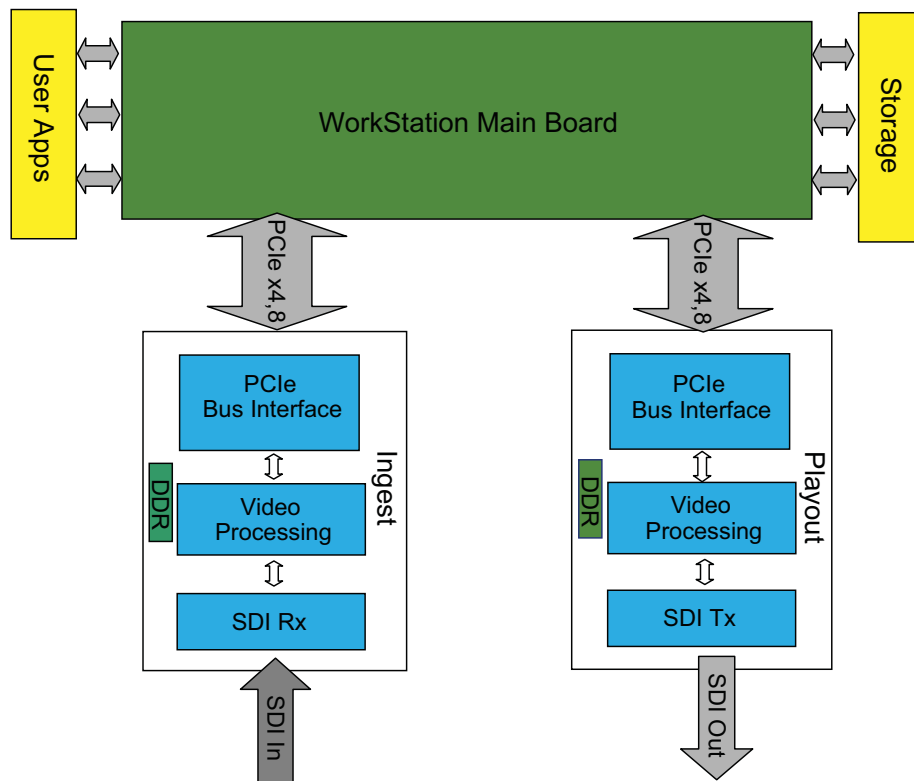


SDI-PCIe bridging is used in video servers and video I/O cards for non-linear editing. The basic building blocks are combined to implement video streaming with the PCIe bus, and use SDI cable equalizers and drivers as the front-end interfaces. The core of the video streaming and processing resides in the center block, where the Cyclone IV GX FPGA is used to create a custom implementation for specific solution requirements. The PCIe bus interface can also reside in the same FPGA.

Video-Server and Video-Capture Applications

A video-server and video-capture I/O card share the same basic hardware-architecture front end, as shown in Figure 2. Depending on the manufacturer, the ingest and playout functions can be located on a single card or separate cards. Some server applications provide the option of encoding or decoding the raw video using H.264 or MPEG2-HD in the video processing block.

Figure 2. SDI-PCIe Bridge



The PCIe block provides the video-streaming capability for the converted SDI signal to feed the workstation. This block is often a bottleneck, especially when processing multiple 3G-SDI streams at the same time. Because a 3G-SDI full-duplex video streaming over a PCIe card with four lanes translates to a data rate of 3.375 Gbps, the PCIe block

must be highly efficient and must provide high quality of service. The Cyclone IV GX FPGA's PCIe hard IP block supports PCIe Gen1 with a x1, x2, or x4 lane option and with endpoint and rootport functionality. Because this functionality is unique to Cyclone IV GX FPGAs, no other low-cost FPGA on the market provides it.

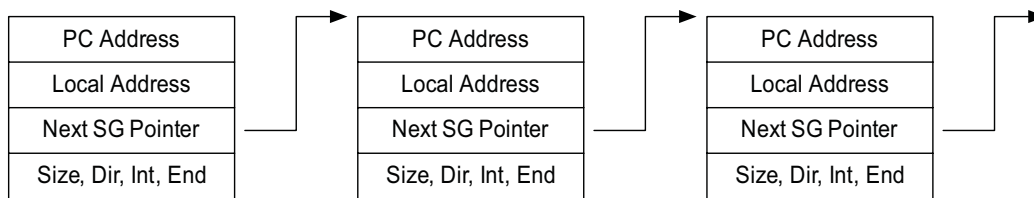
Implementing a 1080p SDI-PCI Express Bridge

The PCIe architecture within a modern PC has more than sufficient bandwidth to transfer several 1080p60 video streams. The challenge for the designer is to utilize this bandwidth without placing excessive demands on either the CPU or the local storage on the PCIe capture card. The choice of a direct memory access (DMA) controller is therefore central to the success of the project.

By packing three 20-bit pixels into two 32-bit words, an active video frame of 1920 pixels by 1080 lines use a little over 5.27 Mbytes. In an ideal world, the CPU creates a single DMA transfer that moves this video frame from the capture card into the system memory of the PC. Unfortunately, this transfer usually is impossible because system memory normally is allocated by the PC operating system in 4-Kbyte blocks, so there is no guarantee that a request for 5.27 Mbytes of memory will be stored in consecutive physical memory locations.

As a result of this limitation, most DMA controllers designed for the PC architecture support a scatter/gather mode (Figure 3). In this mode, the CPU creates a linked list of DMA instructions, each of which transfers just 4 Kbytes. The DMA controller processes each segment of this list in turn, automatically fetching the next entry on the list as needed. By doing so, the controller can be programmed to cope with the PC's fragmented memory allocation and still place little overhead on the CPU.

Figure 3. Scatter/Gather Mode



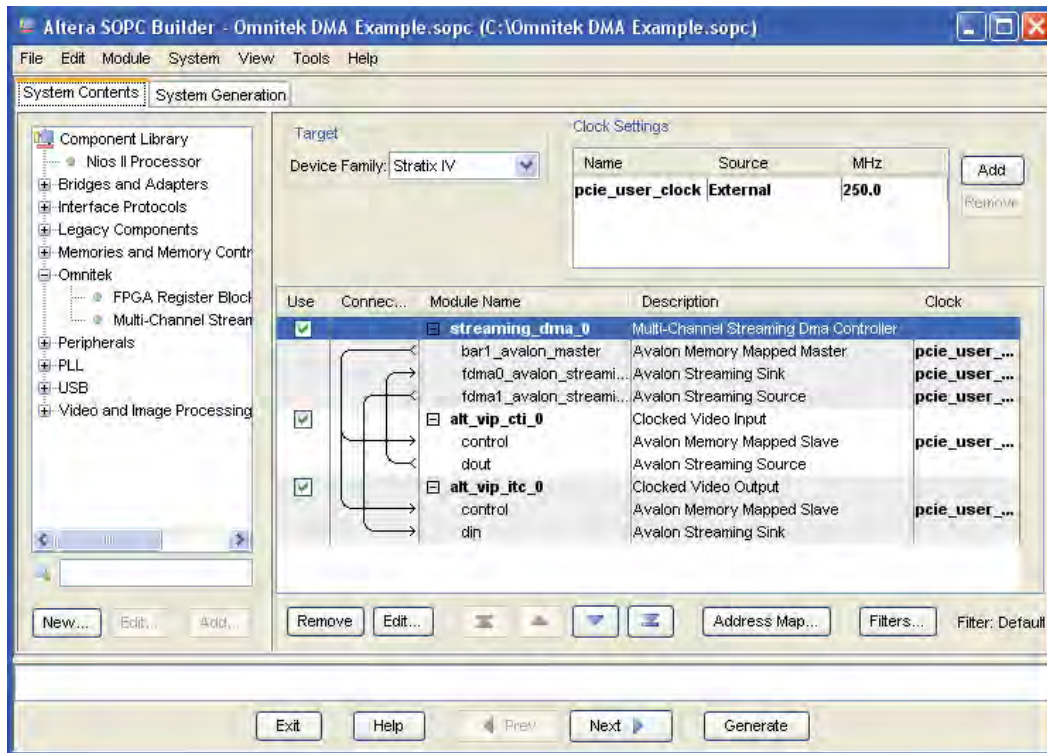
One drawback of PCIe is that, due to its complexity, it has a higher latency than previous bus architectures. This is particularly true for read transactions where the requestor must issue a packet to the completer asking for the data, which the completer then returns. This transaction therefore accrues twice the PCIe link latency. Several mechanisms have been included in the design of PCIe to mitigate the effect of this latency, such as supporting large packet sizes and multiple outstanding read requests.

If a DMA controller waits until the previous read completion is returned by the completer before issuing the following read request, the overall transfer performance from system memory to the capture card is poor. To improve this downstream efficiency, the DMA controller must support multiple outstanding read requests. This means that the DMA controller must always be looking ahead and issuing the following read requests, before the previous bus transaction has completed. In this way, the effects of the read latency on the overall bandwidth utilization are minimized.

The effect is still present, however, for each individual read access, and is a particular issue for scatter/gather DMA controllers. It is no longer acceptable for controllers to wait until the end of a scatter/gather segment before fetching the next set of instructions, because to do so would once again lower the overall efficiency of the system. Waiting also increases the local storage required to hold the extra video data while the next element of the linked list is retrieved.

DMA controllers supporting all of the required features are available as IP that can be fully integrated into the FPGA design flow. In addition, all of the blocks needed to build a 1080p SDI-PCIe bridge are available as IP cores from Altera and partner companies. Figure 4 illustrates the process of building a 1080p SDI-PCIe bridge using the SOPC Builder tool.

Figure 4. SOPC Builder Screenshot



The streaming_dma_0 component, part of the complete Quartus® design software schematic (Figure 5), includes both the complete PCIe interface and a scatter/gather DMA controller. The SOPC Builder environment uses Altera’s Avalon® Streaming (Avalon-ST) video interfaces to allow IP blocks from different vendors to communicate with each other. This SOPC Builder design is then connected to the SDI IP core to complete the hardware design (Figure 6).

Figure 5. Complete Quartus Schematic Design

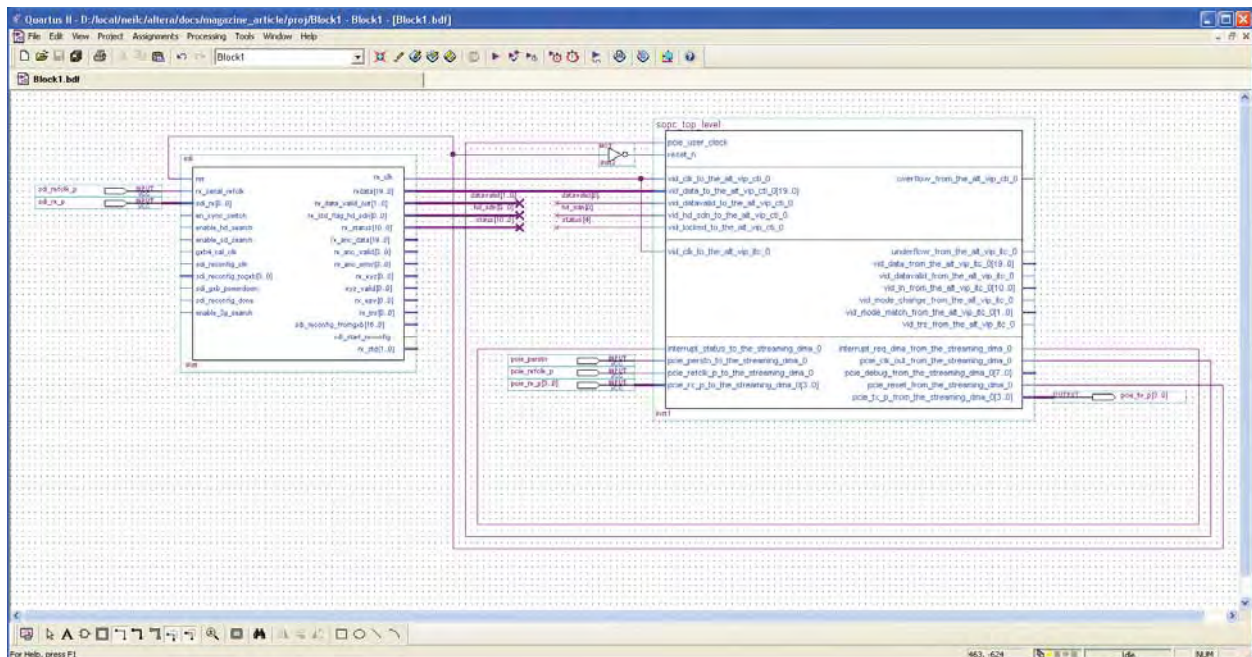
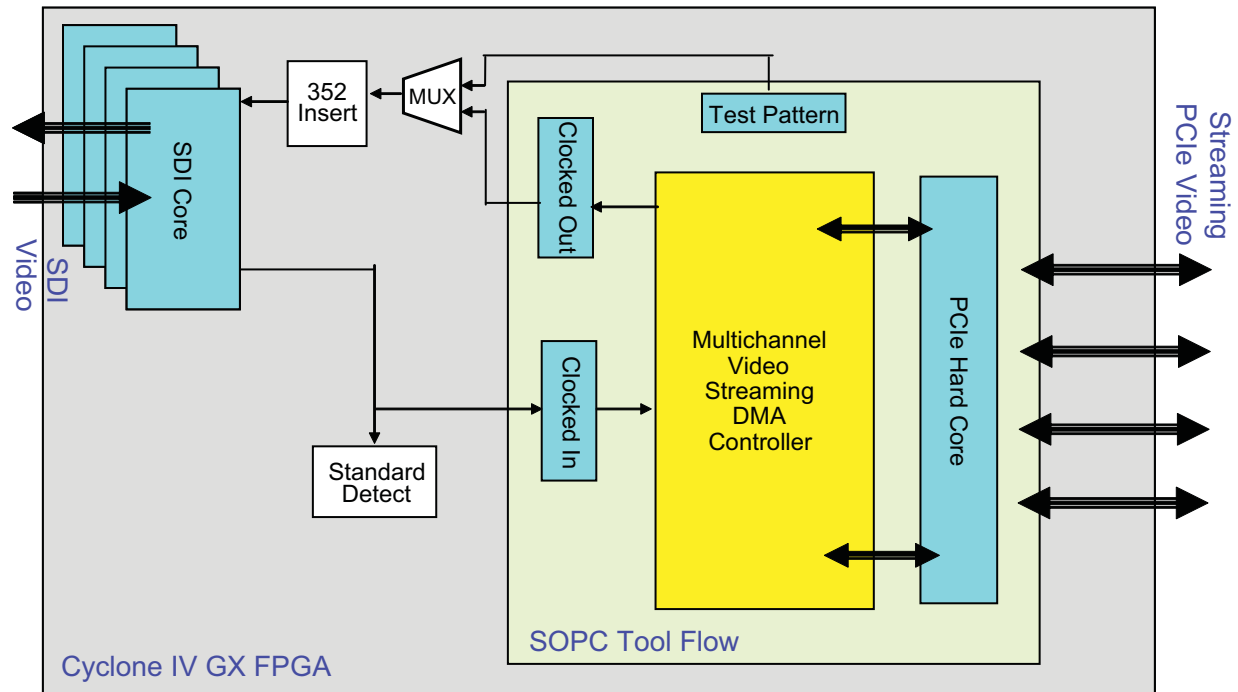


Figure 6. Complete Multichannel Video Streaming on a Chip



Conclusion

The availability of video-specific development boards and their associated SDI daughter cards, IP cores, and user-friendly design tools turn a complex video-streaming system design into a much simpler task for the average engineer. In addition, free video reference designs from Altera can be used as starting points to create video-streaming application projects. Altera constantly adds to and updates its tools and solutions; contact your local Altera sales representative to find out about the latest releases.

Further Information

- 3G-SDI:
www.altera.com/end-markets/broadcast/3g-sdi/bro-3g-sdi.html
- Triple-Rate SDI Reference Design:
www.altera.com/support/refdesigns/sys-sol/broadcast/ref-triple-rate-sdi.html
- SDI-PCIe Bridging Reference Design:
www.altera.com/support/refdesigns/sys-sol/broadcast/ref-sdi-pcie.html
- Terasic SDI-HSMC Daughter Card:
www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=68&No=343
- Contact Altera:
www.altera.com/corporate/contact/con-index.html

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- Tam Do, Senior Technical Marketing Manager, Communication Business Unit, Altera Corporation



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