Boosting System Performance with External Memory Solutions

WP-01134-1.0 White Paper

Altera has designed all of the components of its external memory solutions to work together to achieve the efficient, high-performance outcome that today's applications demand. All pieces of the solution, working together, boost Altera® FPGAs to the outstanding performance level required by all applications.

Introduction

Over 70% of designs on Altera® FPGAs require some type of external memory in the design, but the needs vary depending on the individual application. This white paper addresses all aspects of building external memory solutions with Altera FPGAs, including application needs, memory capabilities of Altera FPGAs, and device and intellectual property (IP) selection. Also discussed is the modular style of the memory components, comprised of Altera's PHY offerings with circuit enhancements and calibration features, and its new controller offering with new features including advanced bank management. In addition, Altera provides a high level of quality assurance in terms of testing, tools, design examples, and documentation.

Application Needs

Memory usage, in individual applications, ranges from high-performance DDR3 to low-power mobile DDR, as shown in Table 1. In the case of the wireline 40/100G application, where performance is key, the DDR3 must run as fast as possible to keep pace with the demands of the network. At the other end of the spectrum, there are portable applications, such as military handheld radios, where power is the most important criteria. These portable applications trade performance for power because they often are in battery-based systems where power is a premium. There are many more examples where the application dictates the type and speed of the memory required.

Table 1. Range of Memory Needs in Applications

Application	Need	Memory Standard
40G/100G	High performance	DDR3, RLDRAM II, QDR II/+
Basestations	Low latency	DDR2/3
Video processing	Increased efficiency	Multiport efficiency, DDR3 @ 533 MHz
Disk array, servers, accelerators	More functions	RDIMM, ONFI, flash, QDR II/+
Low-power/portable	Low power	LPDDR, mobile DDR

Altera has designed its FPGA and IP products to meet the demands of various applications. Altera FPGAs (illustrated in Figure 1) and their value to specific applications include:

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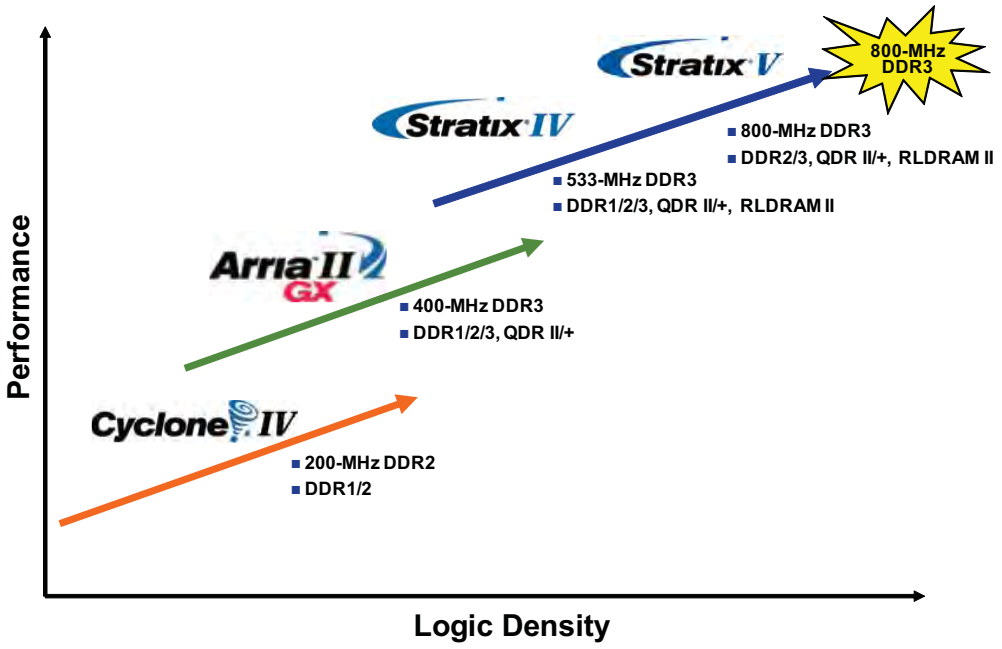
- Stratix® IV and Stratix V FPGAs—Highest performance available up to 800 MHz
- Cyclone® IV FPGAs—Low power and low density
- Arria® II GX FPGAs—Lower power than Stratix IV and Stratix V FPGAs, but higher performance than Cyclone IV FPGAs

Figure 1. Memory Capabilities of Altera FPGAs



Modular Memory Components

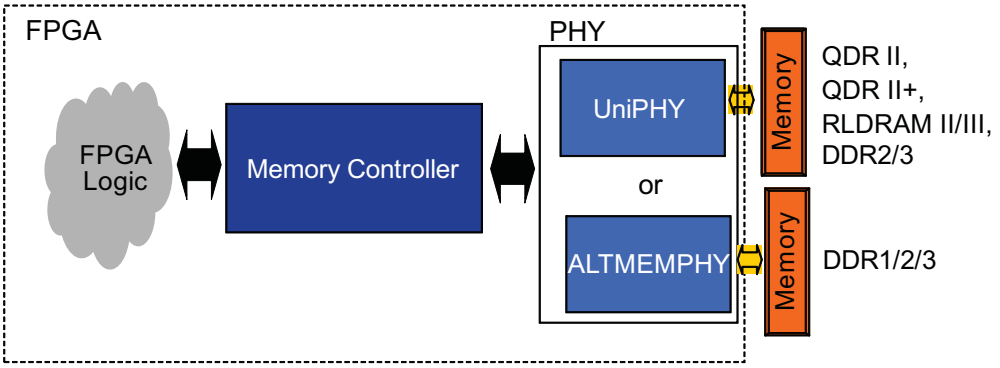
Altera's FPGAs achieve memory performance via external memory IP, which is comprised of a PHY and a controller. Designers can choose the default memory solution listed in Quartus® II software version 10.0, with the optimal PHY and controller IP selected based on the memory requirements (shown in Table 2), or can choose to customize the memory interface.

Table 2. Default PHY and Controller Solutions

FPGA	PHY	Controller
Stratix IV and Stratix IV	UniPHY	HPMCII
Arria II GX	ALTMEMPHY	HPMCII
Cyclone IV	ALTMEMPHY	HPMCII

As stated earlier, the default memory solutions are not the only options. Because Altera's memory solution is modular, designers can build a custom PHY, a custom controller, or both, as desired. Figure 2 shows the modular components that can be mixed and matched to make up the Altera memory solution.

Figure 2. Modular Components in the Altera Memory Solution



Altera's PHY Offerings

Altera has two PHY offerings, ALTMEMPHY, for low-power applications, and UniPHY, for high-performance applications where UniPHY provides half the latency of ALTMEMPHY. Some new features have been added to UniPHY to support the needs of high-performance applications, including PLL and DLL sharing, support for QDR II/II+ and RLDRAM II, and a new smart-calibration algorithm. In addition to the new features, UniPHY has been architected to reduce the latency through the PHY.

Stratix V Circuit Enhancements

As part of Altera's focus on continually improving memory performance and lowering latency, the new Stratix V FPGAs have significant circuit and PHY enhancements. Because of these advancements, Stratix V FPGAs have reached the goals of higher performance and lower latency on memory interfaces. All of the critical circuits in the read/write paths have been hardened to guarantee timing closure at higher frequencies. The hard FIFO buffer in the I/O blocks enables the new UniPHY to use half the PHY latency as compared to Stratix IV FPGAs.

For example, at 400 MHz, the ALTMEMPHY read latency is 23 cycles, while the UniPHY Stratix V FPGA PHY latency is expected to be 11 cycles. Other features, like duty cycle correction, advanced calibration algorithms, and voltage and temperature (VT)-compensated deskew delays, increase the operating margin for high data rates and high system reliability. Stratix V FPGAs not only increase the memory interface performance, but also make it easier to implement.

Calibration Features

As well as the new features in UniPHY and the enhancements made to Stratix V FPGAs that streamline the memory for high performance and low latency, Altera PHY IP has built-in calibration features that enable designers to maintain desired performance. These calibration features are supported on both ALTMEMPHY and UniPHY and in all Altera FPGAs.

There are three types of calibrations available in the Altera memory IP, each of which performs a key function to maintain external memory performance:

- Capture margin from memory to device—The calibration sequencer removes the skew across the DQ group to get the best capture window.
- From memory domain to system domain via resync margin via calibration—Once the removal of the skew is complete and the sequencer has done the best job of capturing the data from the memory domain, it must be transferred to the system domain. In the resync stage, the auto-calibration sequencer automatically sets the PLL phase to the best resync margin possible using the resync calibration.
- Maintain the margin over time with VT compensation—This calibration maintains the established margins over variations of VT. The VT compensation performs the function of maintaining the robust margins over varying power, voltage and temperature (PVT) conditions.

The calibration techniques are transparent to the designer because they are integrated into the PHY IP and perform their functions with no required designer involvement. These three techniques allow Altera devices to achieve and maintain high performance.

Altera's Controller Offering

The second part of the memory solution is the controller. Based on the High-Performance Memory Controller (HPMC), Altera's new High-Performance Memory Controller II (HPMCII) includes new features (Table 3) that enable Altera devices to achieve greater efficiency when processing data to and from memory, thus increasing the overall performance of the interface.

Table 3. Features in Altera's Controllers

Features	HPMCII	HPMC
ECC with sub-word write	✔	✔
Power management	✔	✔
5-cycle controller latency (6 with ECC)	✔	✔
Support for 800-MHz DDR3 memory	✔	
Advanced bank management with command look-ahead	✔	
Flexible system interface	✔	
Run-time programmable	✔	

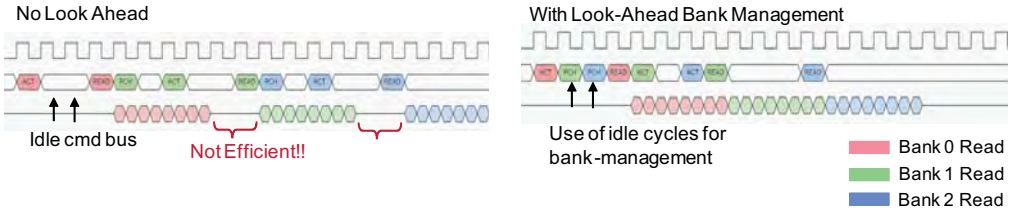
Advanced Bank Management with Command Look-Ahead Feature

The controller's efficiency features are what enable Altera FPGAs to achieve their improved performance. In particular, the advanced bank management with command look-ahead feature enables the HPMCII to achieve up to 5X higher efficiency compared to the HPMC. This efficiency feature is a key differentiator for all Altera FPGAs, enabling them to achieve maximum performance.

The advanced bank management feature enables Altera FPGAs to utilize the idle command bus more efficiently, which reduces the idle times on the bus. Rather than waiting for the read or write command to be fully issued before the bus is activated by the arrival of the entire packet (Figure 3, left), the advanced bank management feature performs a pre-charge of the link does and looks ahead to anticipate which data

packets will need to be fetched or where the data needs to be placed (Figure 3, right). This means that once the data arrives, the bus and the memory are ready to perform the transaction, rather than just starting bus initialization. This feature enables the application running in the FPGA to run more smoothly and achieve optimal performance.

Figure 3. Advanced Bank Management Feature



Quality Assurance

Thorough testing, easy-to-use tools, example designs, drivers, and test benches, and improved and expanded documentation are all part of Altera's focus on improving the designer's experience, reducing design time, and increasing design productivity with external memory interfaces.

Testing

A commitment to quality is important for external memory IP, because designers expect it to work properly the first time. Altera performs extensive testing to make sure that these expectations are met. In addition to all the performance, efficiency, and latency enhancements in the new PHY and controller, Altera also focuses on ensuring that external memory solutions are reliable and easy to use. This is done with the help of an extensive test verification environment that has been assembled to test the devices in conjunction with the memory IP. Compliance to memory functionality is performed with fictional hardware tests, which involve testing with both actual memory devices and simulated devices. Design flow testing ensures that the tool-created designs perform as expected, and that the PHY meets the designer's expectations and reliably closes timing.

Tools

Besides testing to ensure that the device and IP work reliably for external memory interconnection, Altera offers tools that make designing external memory interfaces in Altera FPGAs easy. These easy-to-use tools include:

- Memory IP—Both the PHY and controller IP are available in clear-text RTL, which enables the designer to modify the design if necessary. There is no back and forth with the factory for permission to view the clear text, it just comes with the IP.
- Memory IP interfaces—The PHY uses an Altera PHY Interface (AFI) for the PHY-to-controller connection and an Avalon® Memory-Mapped (Avalon-MM) interface for the controller-to-fabric connection.
- Timing and pin constraints—Convenient timing and pin constraints are available in the tools and documentation.

Examples

Altera offers various example designs, drivers, and a test bench to provide a starting point for designers:

- Example designs—Design-parameterizable examples include the PHY, the controller, and a driver.
- Example drivers—Example drivers include a parameterizable traffic generator.
- Example test bench—The example test bench integrates the memory model with the example design and provides a base level of functional verification.

Documentation

Altera has redesigned the External Memory Interface Handbook and IP documentation so that it is very easy to access. The documentation flow is set up with the designer in mind, and the data in each chapter aligns with the design steps that a designer follows. So, as the designer progresses through the handbook, the information becomes more specific to the design. The information for all devices is now in a central location, following a more logical flow to enhance productivity.

In addition to the re-architected handbook, Altera provides many system-level reference designs to give designers a head start on their designs. For example, AN 431: PCI Express to External Memory Reference Design demonstrates how to build memory solutions with Altera's IP and connect it to other IP such as the DDR3 to PCI Express interface on the Stratix IV GX FPGA.

Conclusion

To achieve high performance at the low latency solution required for 800-MHz DDR3 connectivity, IP, hardware, test verification, and documentation must all work together. Altera has designed all of the components of its external memory solutions to work together to achieve the efficient, easy-to-use, high-performance outcome that external memory designers demand. All pieces of the solution, working together, get Altera FPGAs to the outstanding performance level required by all applications.

Further Information

- Stratix V FPGAs: Built for Bandwidth:
  www.altera.com/products/devices/stratix-fpgas/stratix-v/stxv-index.jsp
- Literature: Stratix V Devices:
  www.altera.com/products/devices/stratix-fpgas/stratix-v/literature/stv-literature.jsp
- Altera's External Memory Solutions Center:
  www.altera.com/technology/memory/mem-index.jsp
- Webcast: "Achieving 800-MHz DDR3 Performance With Advanced Silicon and Memory IP"
  www.altera.com/education/webcasts/all/wc-2010-800mhz-adv-silicon-memory-ip.html
- High-Performance Memory Controller II SDRAM MegaCore® Function:
  www.altera.com/products/ip/iup/memory/m-alt-high-perf-mem-controller-ii.html
- Literature: External Memory Interfaces:
  www.altera.com/literature/lit-external-memory-interface.jsp
- *AN 431: PCI Express to External Memory Reference Design*:
  www.altera.com/literature/an/an431.pdf

Acknowledgements

- Bryce Mackin, Manager, Product Marketing, Altera Corporation

Document Revision History

Table 4 shows the revision history for this document.

Table 4. Document Revision History

Date	Version	Changes
June 2010	1.0	Initial release.