

IPTV's Key Broadcast Building Blocks

Introduction

Telcos, in pursuit of the triple play (voice, video, and data), are investing heavily to compete with the cable companies in providing quality video content to the consumer. However, most telco infrastructures do not currently have the bandwidth to support high-quality video distribution. The telcos are updating their Internet protocol (IP) networks and using new encoding schemes such as MPEG4-Part 10 (also called H.264-AVC) to deliver video content to the consumer.

This creates a huge opportunity for supplying telcos with updated equipment including the latest encoders and decoders. This paper will investigate the technology that is fueling this new Internet protocol television (IPTV) infrastructure. The first portion will be looking at the video encoding method and the second portion will focus on the video-over-IP network design that is being used for IPTV.

IPTV

The telcos are on the offensive to gain a big piece of the video market share from the cable TV providers. Cable multiple service operators (MSOs) have made great progress in delivering a "triple play" of voice, video, and data services to the consumer in the last few years. Now the telcos are responding in a big way to provide the same triple play by offering not only voice and data, but also high-quality digital TV video via a new technology called IPTV. IPTV is an emerging technology that allows consumers to watch high-quality digital TV over the Internet via an IPTV set-top box or a PC. The traditional cable companies use a RF signal to carry the digital video by means of QAM.

Technology advancements have made it possible for telcos to bring the same quality of video via the Internet. The key building blocks on the transmission side are advanced video encoding and video over IP. Advanced video encoding is the most critical building block. The availability of high-definition (HD) content along with standard definition (SD) content have created a challenge for the telcos, since telcos still rely on bandwidth-limited twisted copper pair of wires and usually do not have the luxury of cable's broadband capability. A typical HD channel requires 20 Mbps and a SD channel requires 4 Mbps. Therefore, a bandwidth-efficient video transport mechanism is needed. The H.264 format of MPEG4 Part 10 and Microsoft's VC-1 encoder can offer 2.5 to 3 times more bandwidth-efficient improvement over the popular MPEG2 encoding. Most broadcasters are adapting the H.264 standard rather than the VC-1 standard. The other building block of IPTV transmission is video over IP, which maps or bridges the encoded video data onto the Internet for delivery.

H.264 Encoder

The H.264 is also known as MPEG-4 ISO/IEC14496-10 or MPEG-4/AVC. This standard was co-developed by a JVT group composed by MPEG-ISO/IEC members and VCEG-ITU-T members. Three profiles (main, baseline, and high) have been defined, each with several levels. The main profile is required for broadcast video quality, while the baseline profile is typically used for mobile and video conferencing applications. The H.264 encoder system block diagram (Figure 1) includes two dataflow paths, a "forward" path and a "reconstruction" or feedback path.

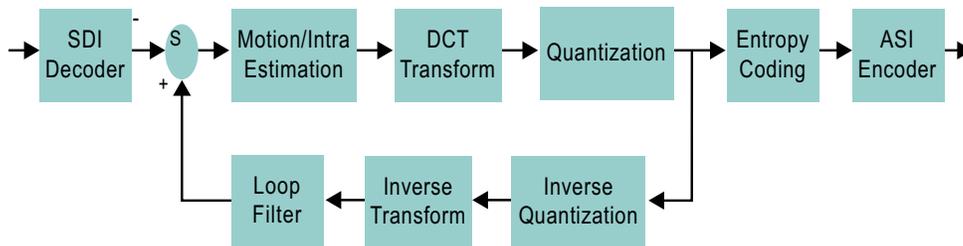


Figure 1. H.264 Encoder Block Diagram

H.264 encoding is ten times more complex than the MPEG2 encoding. For the motion estimation and compensation section, H.264 employs blocks of different sizes and shapes, multiple reference frame selection, and multiple bi-directional mode selection. For the transform section, H.264 uses an integer-based transform that roughly approximates the discrete cosine transform (DCT) used in previous MPEG standards, but does not have the mismatch problem in the inverse transform. Entropy coding can be performed using either a combination of a single universal variable-length codes (UVLC) table with context adaptive variable-length codes (CAVLC) for the transform coefficients, or using context-based adaptive binary arithmetic coding (CABAC). The H.264 design is very complex, computing-hungry, and requires parallel processing. If a general-purpose processor is used, it will be limited by its internal architecture (i.e., if it has eight internal multipliers, it can perform eight multiplications per cycle). A programmable logic device (PLD) is flexible and highly scalable: if an algorithm needs 100 multiplications per cycle, then the PLD can be programmed to perform the required task. Figure 2 shows a single-chip main profile H.264 encoder PLD implementation using an Altera® Stratix® II device.

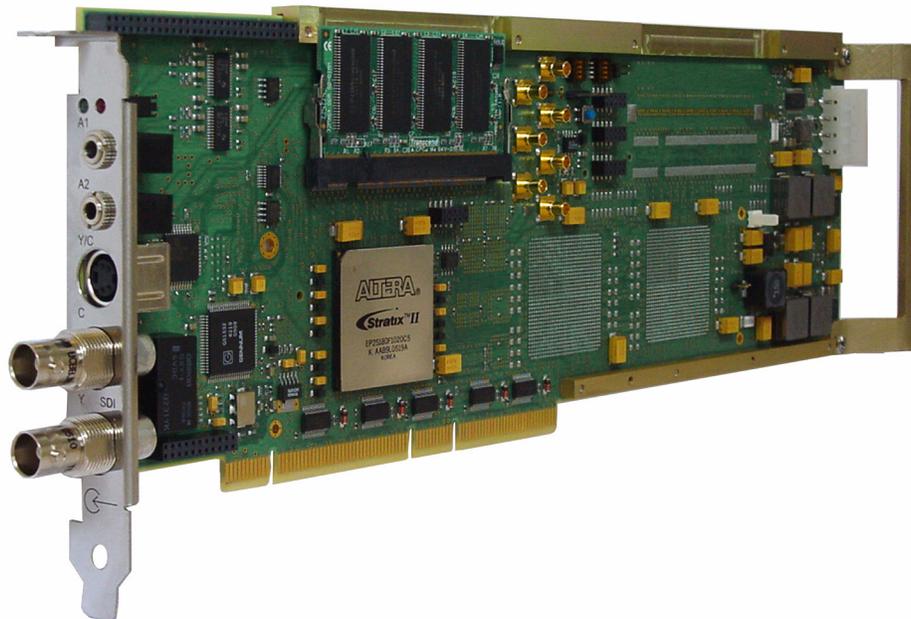


Figure 2. Single Chip H.264 Encoder

Video Over IP

Video over IP is the transmission of encoded video transport stream (TS) data over IP-based networks. It bridges between one or more encoded video streams and IP packets carried over 100 Mbps or 1 Gbps Ethernet. Video over IP accepts TS data and encapsulates it for transmission over Ethernet. Various standards define video over IP: real-time transport protocol (RTP), RTP payload format for MPEG video, UDP/IP, Pro-MPEG code of Practice #3, and DVB-IPI. The TS input to video over IP is either a DVB-ASI or uncompressed SDI video data that will be mapped onto the Ethernet protocol layer. Figure 3 shows a video-over-IP reference design block diagram that receives a DVB-ASI TS and then converts the TS to IP. The design includes the following main blocks: TS input logic, frame buffer, queue system, Ethernet-receive DMA, encapsulator, transmit channel information, receive channel information, timestamp, media access control (MAC) interface, and host processor interface.

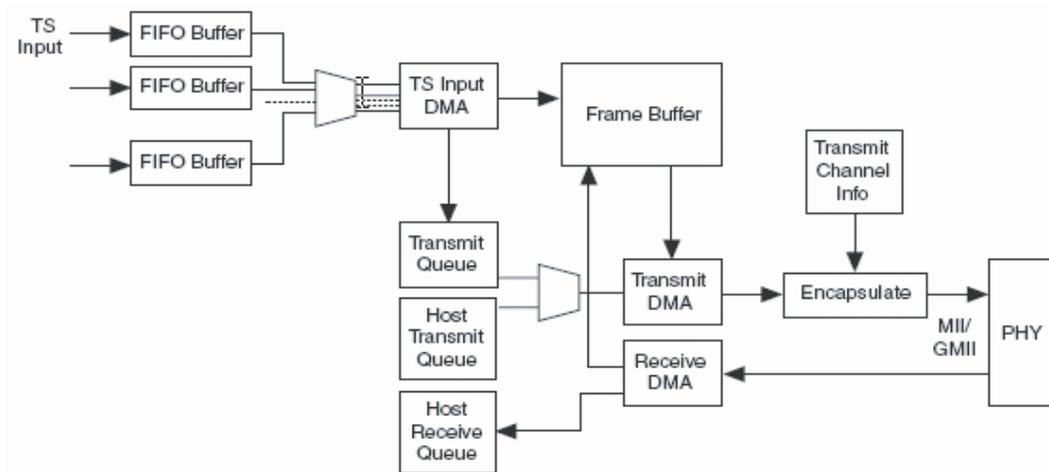


Figure 3. Video-Over-IP Reference Design Block Diagram

Conclusion

In summary, in order to provide quality video over IP, the latest H.264 video encoding technology is used to conserve bandwidth for delivery. Figure 4 shows the overall IPTV transmission system block diagram. The video content can be either SD or HD, uncompressed video, or previous MPEG2 TS. All these formats will be converted to H.264 video format before transmitting. All the key pieces can be implemented efficiently using PLDs for system upgradeability and flexibility.

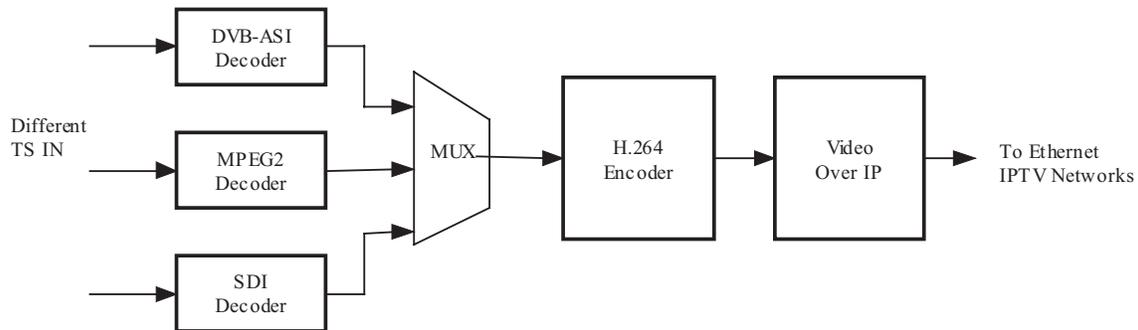
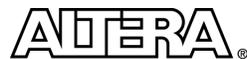


Figure 4. IPTV Core Block Diagram

Further Information

- Specification details of QAM can be obtained from the International Telecommunication Union (ITU) J.83 Recommendation:
<http://www.itu.int/rec/recommendation.asp?type=items&lang=E&parent=T-REC-J.83-199704-I>



101 Innovation Drive
 San Jose, CA 95134
 (408) 544-7000
<http://www.altera.com>

Copyright © 2006 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.